

N-channel 800 V, 1.3 Ω typ., 4.5 A MDmesh™ K5 Power MOSFETs in TO-220FP and I²PAKFP packages

Datasheet - production data

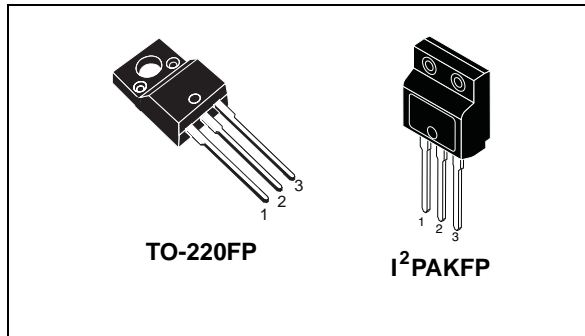
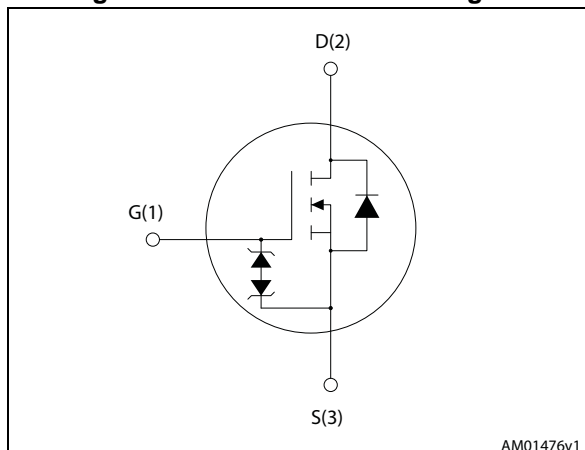


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STF6N80K5	800 V	1.6 Ω	4.5 A	25 W
STF16N80K5				

- Industry's lowest RDS(on)
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF6N80K5	6N80K5	TO-220FP	Tube
STF16N80K5		I ² PAKFP	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	4.5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	2.8	A
I_{DM} ⁽²⁾	Drain current (pulsed)	18	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	25	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	84	mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$)	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 4.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, peak $V_{DS} \leq V_{(BR)DSS}$
4. $V_{DS} \leq 640\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	62.5	

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 800 V			1	μA
		V _{DS} = 800 V, T _j = 125 °C			50	μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2 A		1.3	1.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	270	-	pF
C _{oss}	Output capacitance		-	25	-	pF
C _{rss}	Reverse transfer capacitance		-	0.7	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0	-	38	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	16	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0	-	7.5	-	Ω
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 4.5 A V _{GS} = 10 V	-	13	-	nC
Q _{gs}	Gate-source charge		-	2.1	-	nC
Q _{gd}	Gate-drain charge		-	9.6	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 2.25\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$	-	16	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	28.5	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.5\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.5\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$,	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.2		μC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.5\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$	-	450		ns
Q_{rr}	Reverse recovery charge		-	3.15		μC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area

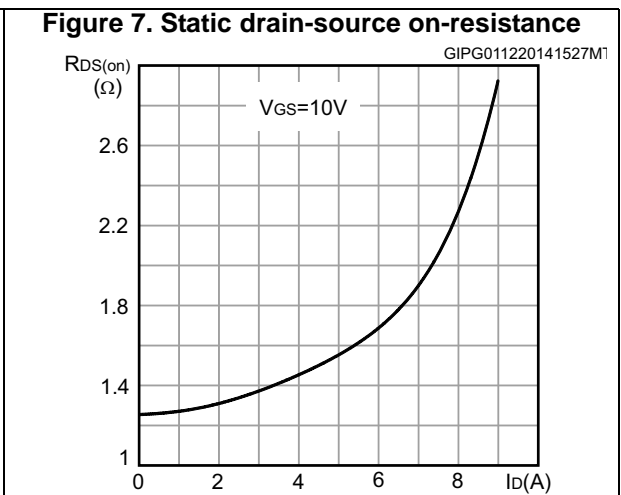
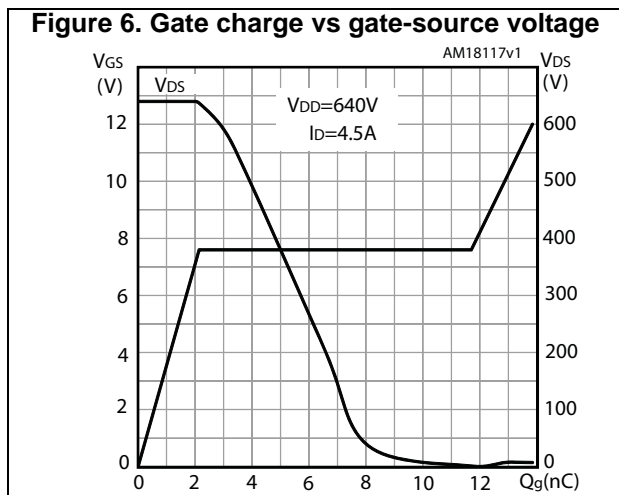
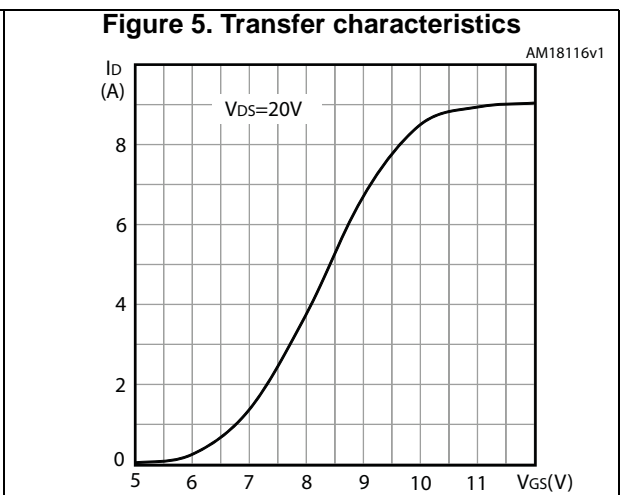
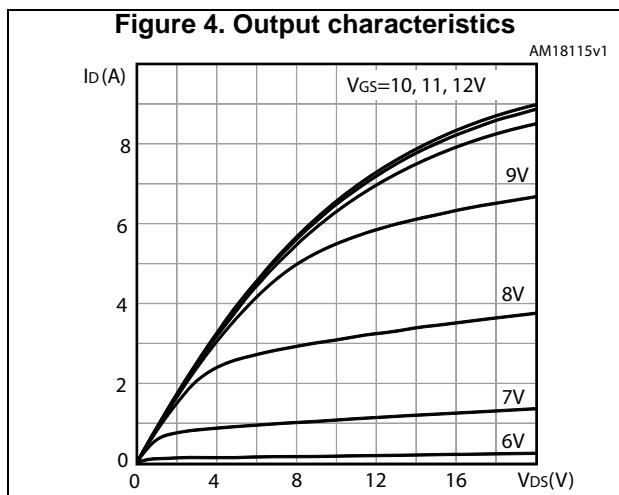
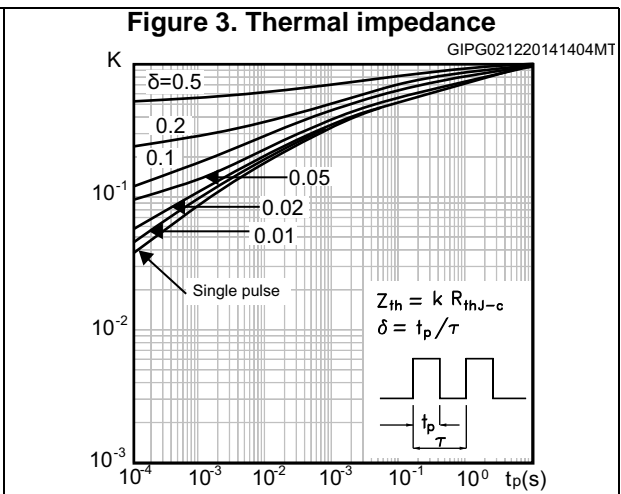
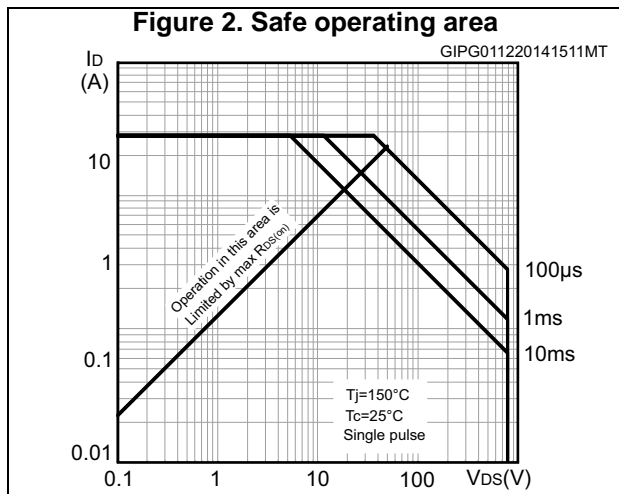
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

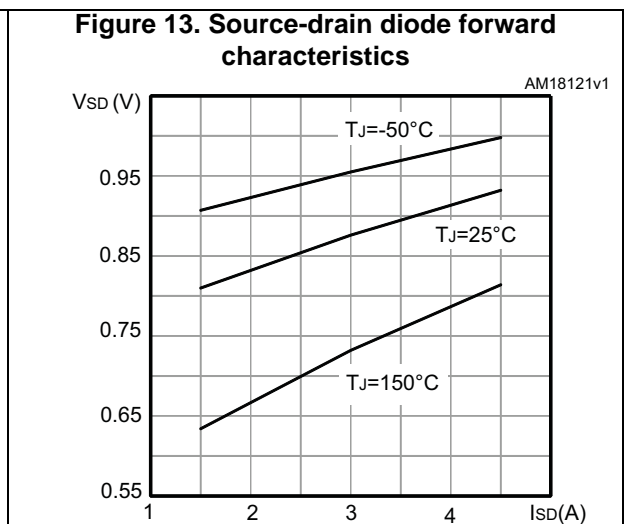
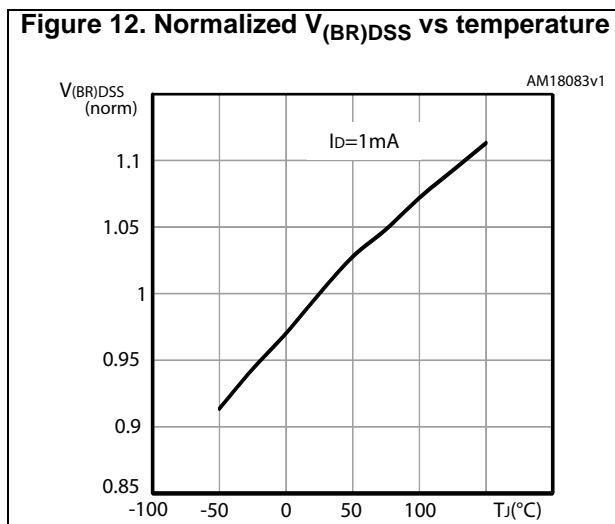
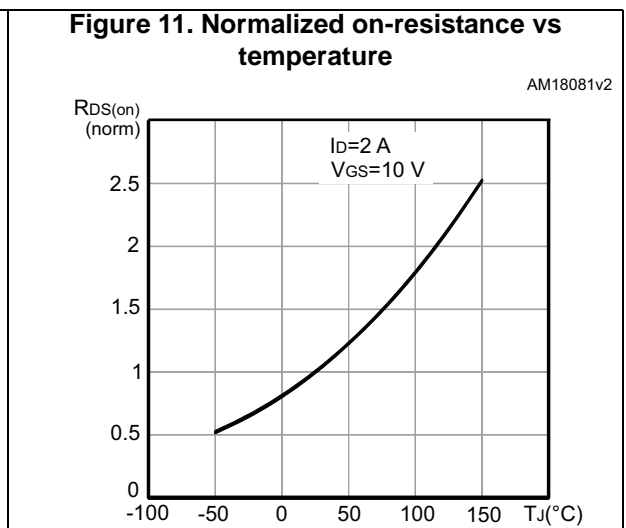
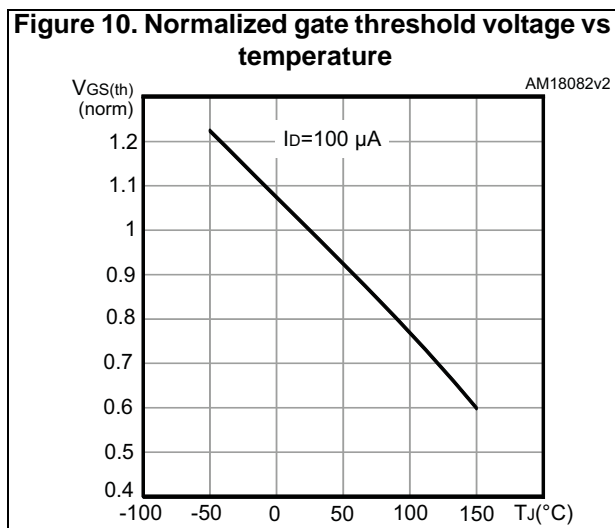
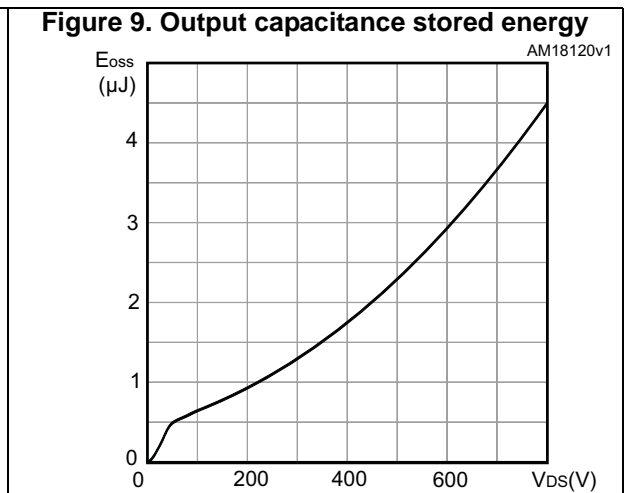
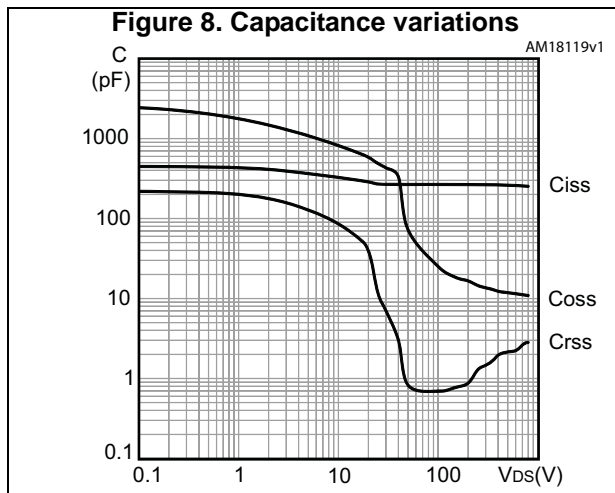
Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

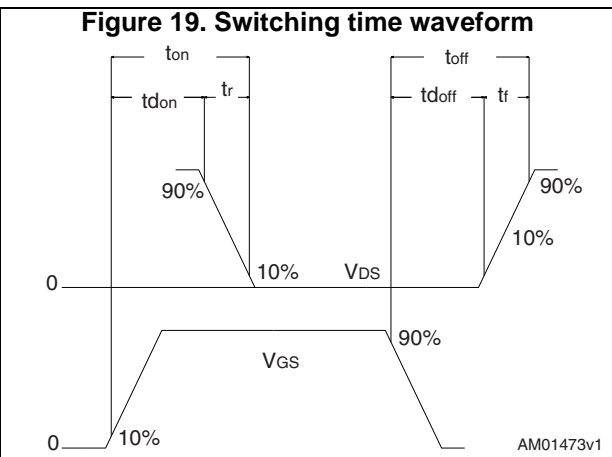
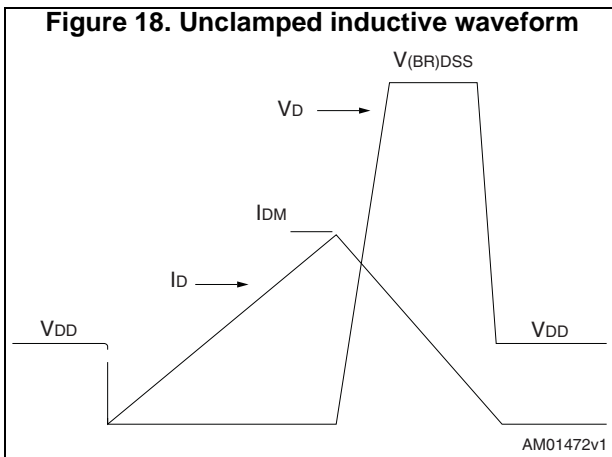
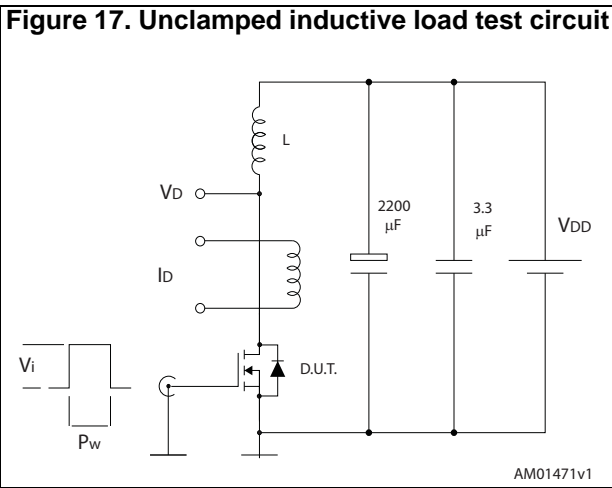
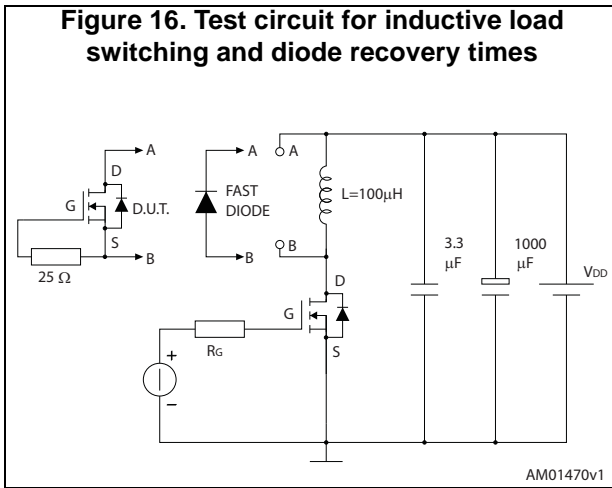
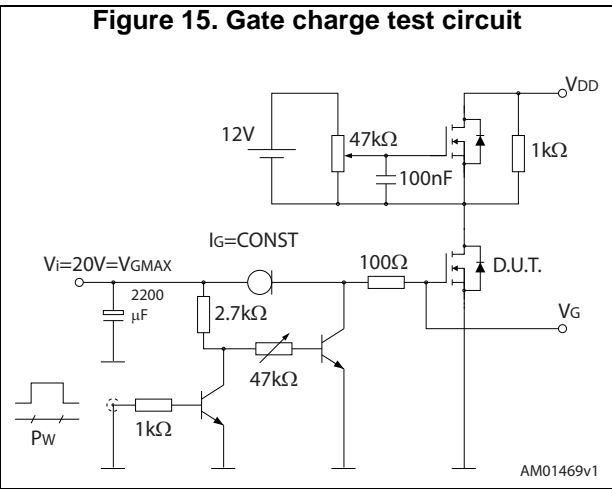
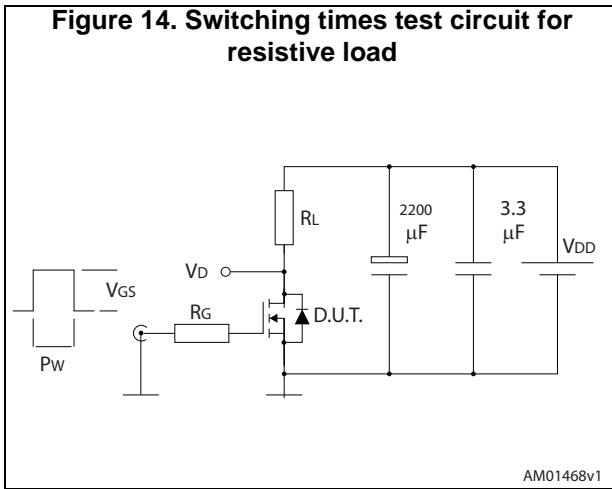
The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)





3 Test circuits

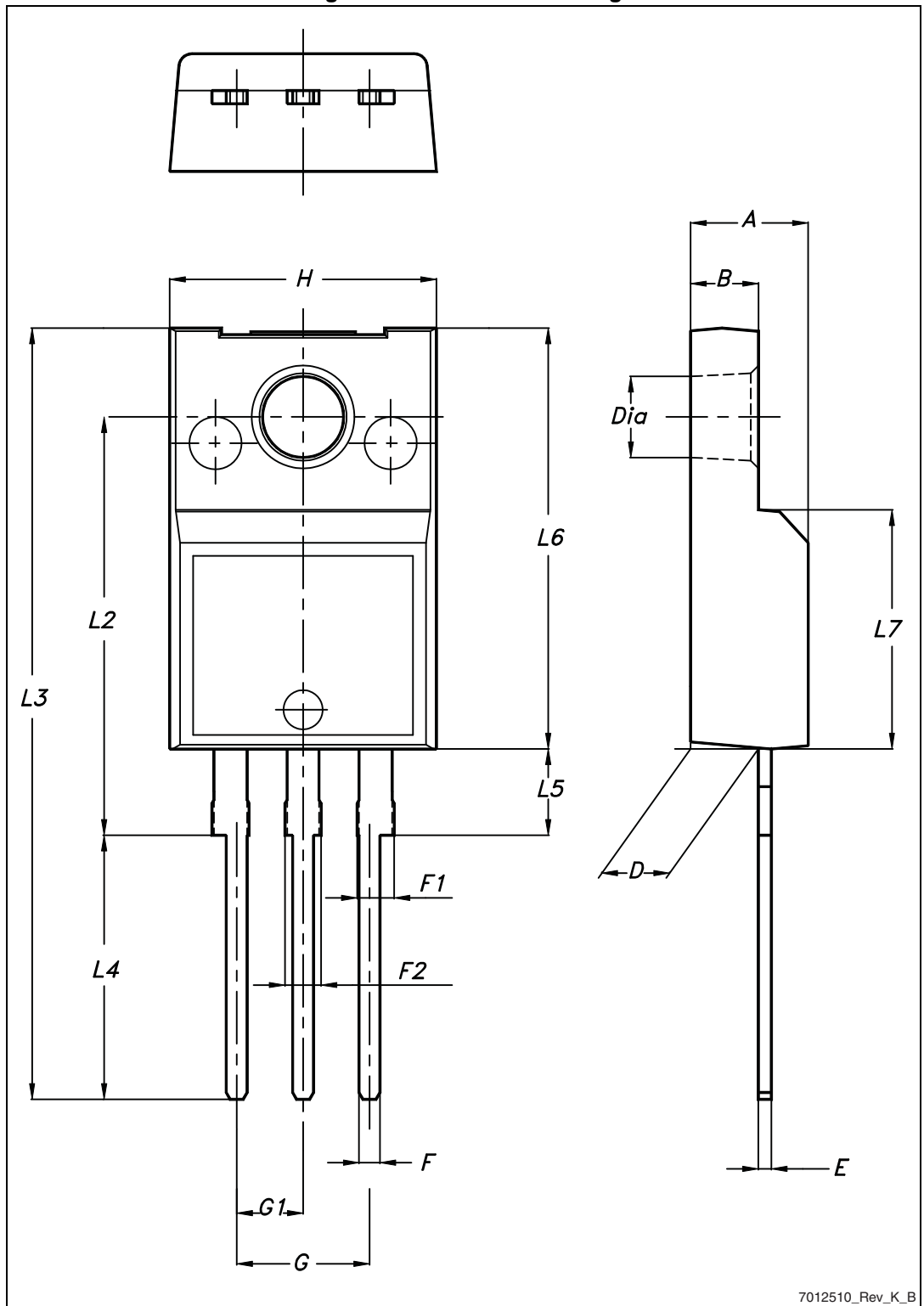


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220FP, STF6N80K5

Figure 20. TO-220FP drawing



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAKFP (TO-281), STF16N80K5

Figure 21. I²PAKFP (TO-281) drawing

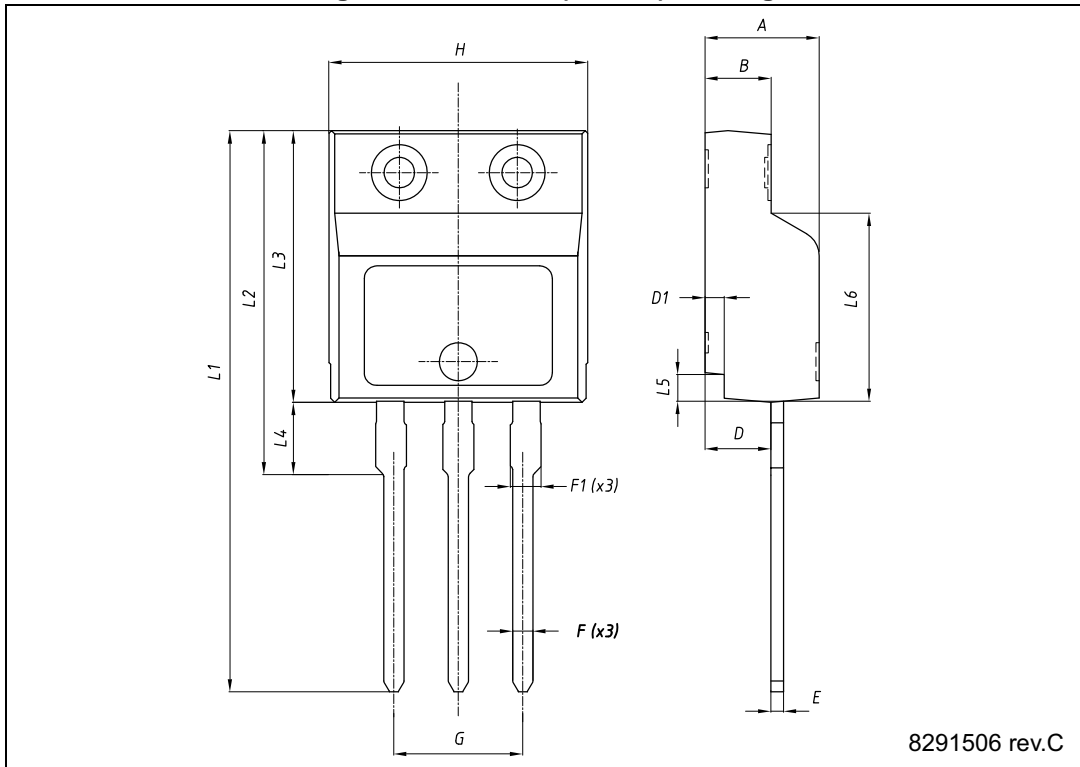


Table 10. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
28-May-2013	1	First release.
05-Mar-2014	2	<ul style="list-style-type: none"> – Datasheet status promoted from preliminary data to production data – Added: I²PAKFP package – Modified: E_{AS} value in Table 2 – Added: MOSFET dv/dt ruggedness test condition and note 4 in Table 2 – Modified: R_G value in Table 5 – Modified: the entire typical values in Table 5, 6 and 7 – Added: Section 2.1: Electrical characteristics (curves) – Minor text changes
05-Dec-2014	3	<p>Updated title, features and description in cover page.</p> <p>Updated Section 2.1: Electrical characteristics (curves) and Section 4: Package mechanical data.</p> <p>Minor text changes.</p>

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