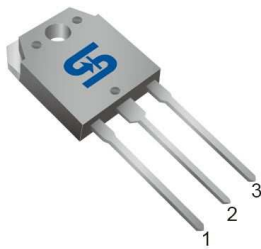


TO-3PN

Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
500	0.3 @ $V_{GS}=10V$	20

General Description

The TSM20N50CN N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, electronic lamp ballast based on half bridge.

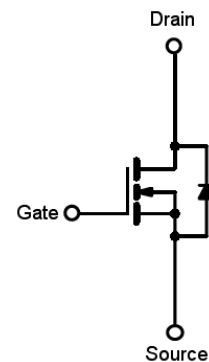
Features

- Low $R_{DS(ON)}$ 0.3 Ω (Max.)
- Low gate charge typical @ 54nC (Typ.)
- Improve dv/dt capability

Ordering Information

Part No.	Package	Packing
TSM20N50CN C0	TO-3PN	30pcs / Tube

Block Diagram


N-Channel MOSFET

Absolute Maximum Rating ($T_a = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ($T_c=25^\circ\text{C}$)	I_D	20	A
Pulsed Drain Current *	I_{DM}	80	A
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Single Pulse Avalanche Energy (Note 2)	E_{AS}	1088	mJ
Avalanche Current (Repetitive) (Note 1)	I_{AR}	20	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	31.2	mJ
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to +150	$^\circ\text{C}$

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R\theta_{JC}$	0.4	$^{\circ}\text{C/W}$
Thermal Resistance - Junction to Ambient	$R\theta_{JA}$	62.5	$^{\circ}\text{C/W}$

Notes: Surface mounted on FR4 board $t \leq 10\text{sec}$

Electrical Specifications ($T_a = 25^{\circ}\text{C}$ unless otherwise noted)

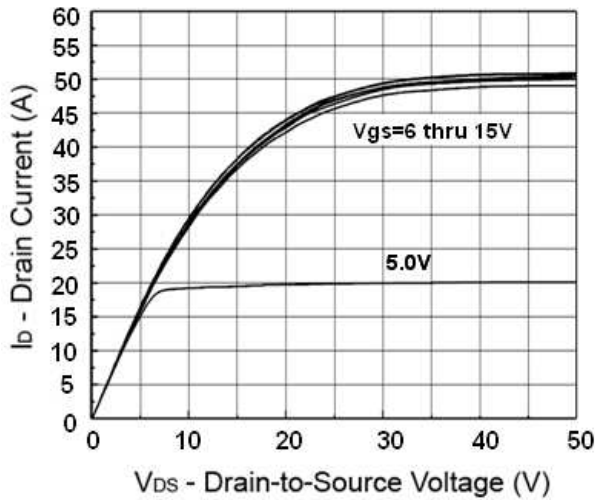
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	$R_{DS(ON)}$	--	0.25	0.3	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.0	--	4.0	V
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Forward Transconductance	$V_{DS} = 30V, I_D = 10A$	g_{fs}	--	11	--	S
Diode Forward Voltage	$I_S = 20A, V_{GS} = 0V$	V_{SD}	--	--	1.5	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 400V, I_D = 20A,$ $V_{GS} = 10V$	Q_g	--	54	--	nC
Gate-Source Charge		Q_{gs}	--	15	--	
Gate-Drain Charge		Q_{gd}	--	12.5	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	3094	--	pF
Output Capacitance		C_{oss}	--	296	--	
Reverse Transfer Capacitance		C_{rss}	--	9.2	--	
Switching ^c						
Turn-On Delay Time	$V_{DD} = 250V, I_D = 20A,$ $R_G = 25\Omega$	$t_{d(on)}$	--	78	--	nS
Turn-On Rise Time		t_r	--	72	--	
Turn-Off Delay Time		$t_{d(off)}$	--	184	--	
Turn-Off Fall Time		t_f	--	68	--	
Reverse Recovery Time	$V_{GS} = 0V, I_S = 20A,$	t_{fr}	--	426	--	nS
Reverse Recovery Charge	$di_F/dt = 100A/\mu s$	Q_{fr}	--	6	--	μC

Notes:

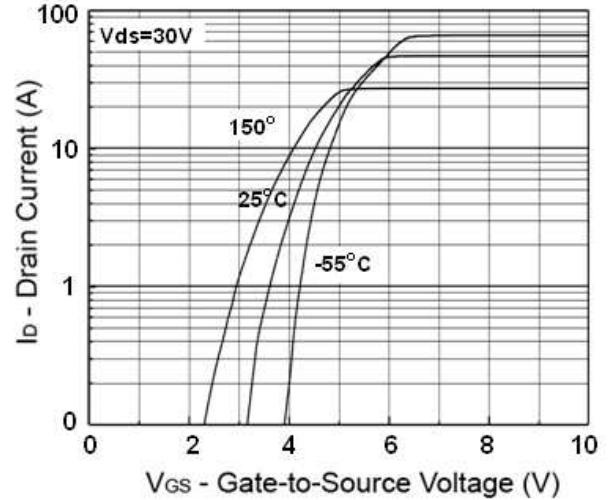
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. $V_{DD} = 50\text{V}, I_{AS} = 20\text{A}, L = 4.9\text{mH}, R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
3. $I_{SD} \leq 20\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{dd} \leq BV_{DS}$, Starting $T_J = 25^{\circ}\text{C}$
4. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
5. b For design reference only, not subject to production testing.
6. c Switching time is essentially independent of operating temperature.

Electrical Characteristics Curve (Tc = 25°C, unless otherwise noted)

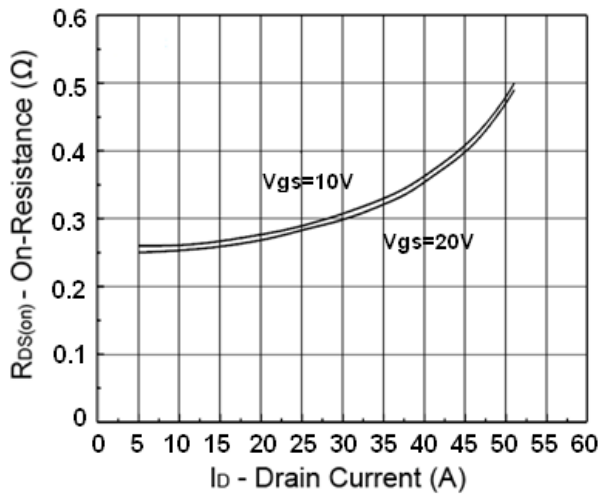
Output Characteristics



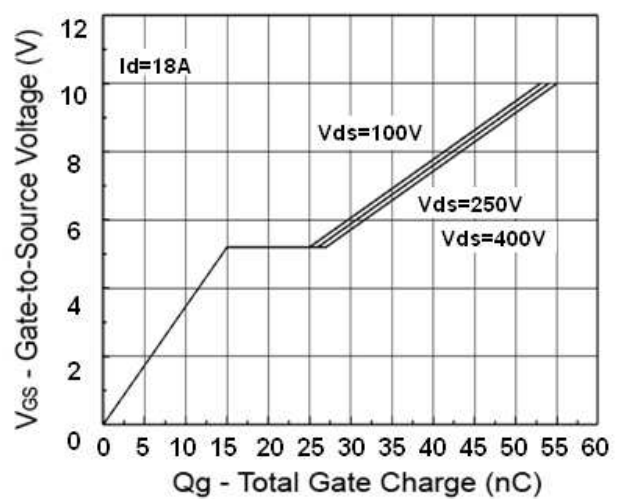
Transfer Characteristics



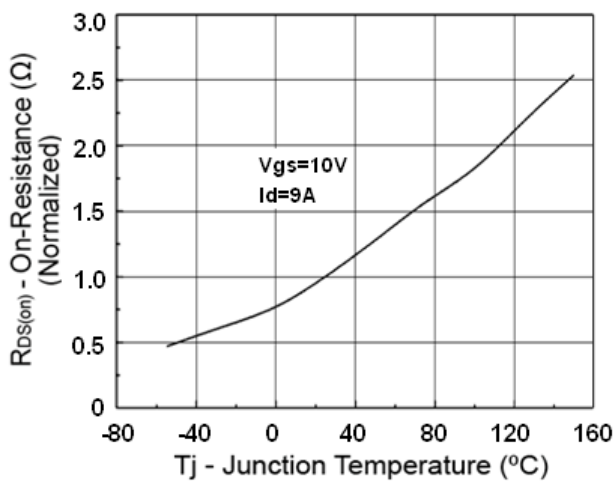
On-Resistance vs. Drain Current



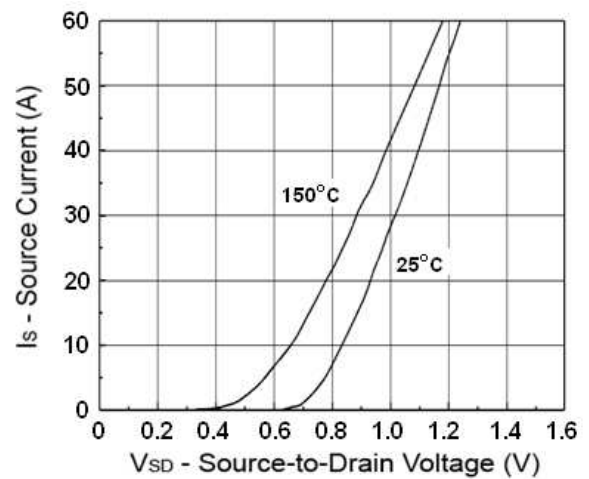
Gate Charge



On-Resistance vs. Junction Temperature

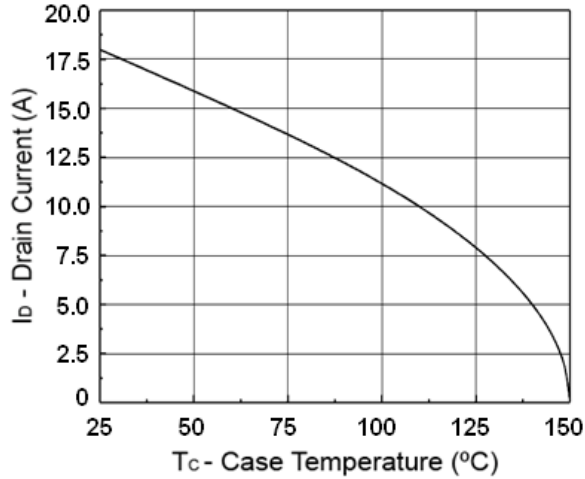


Source-Drain Diode Forward Voltage

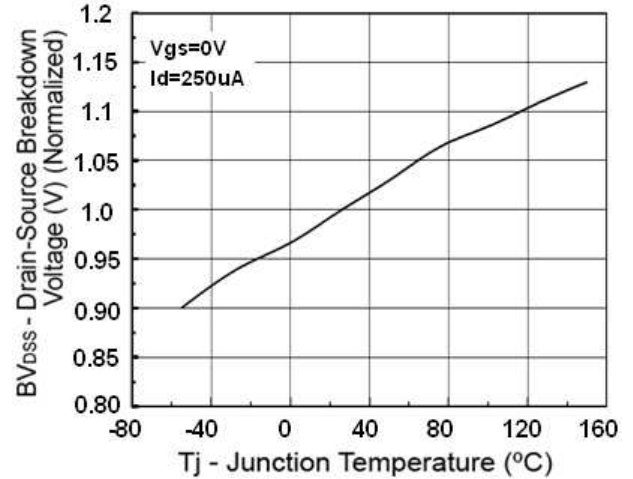


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

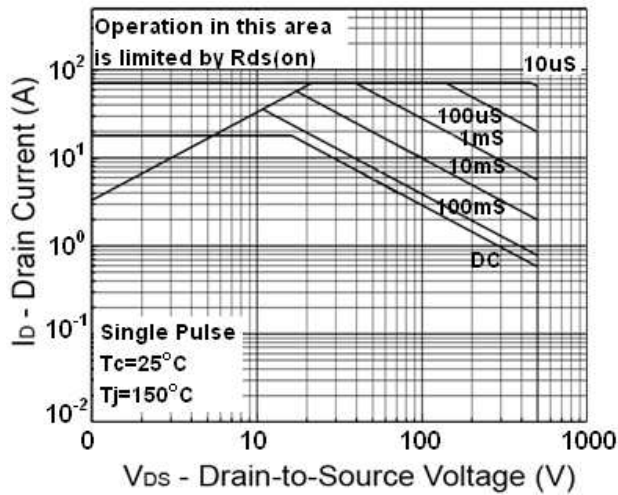
Drain Current vs. Case Temperature



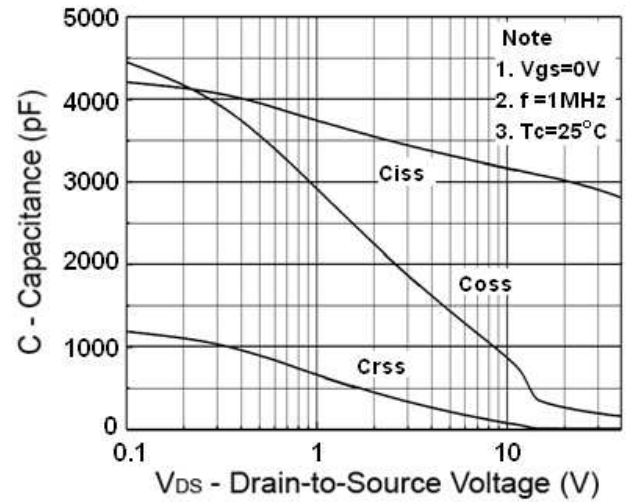
BV_{DSS} vs. Junction Temperature



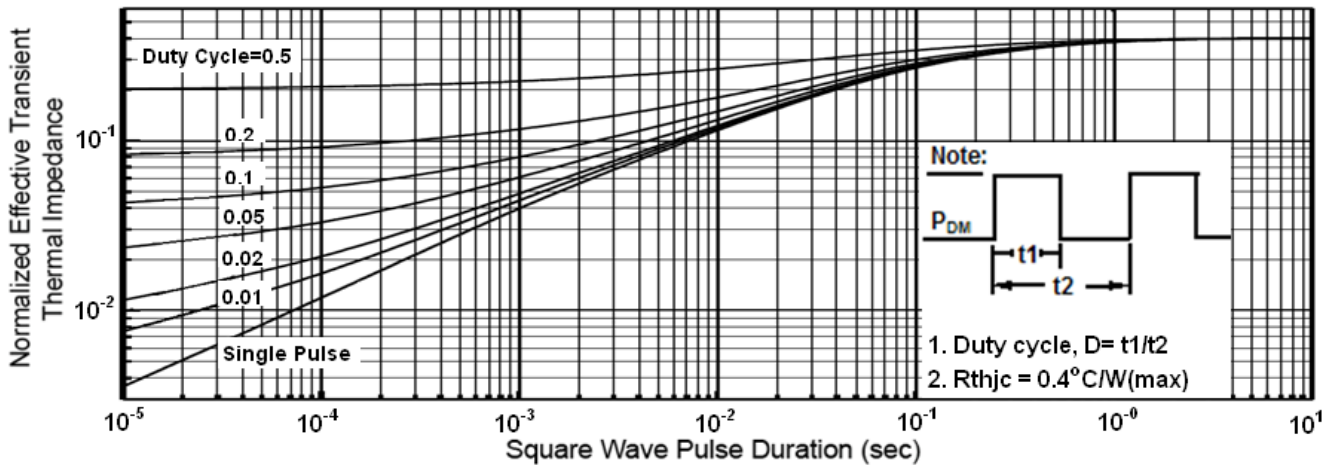
Maximum Safe Operating Area



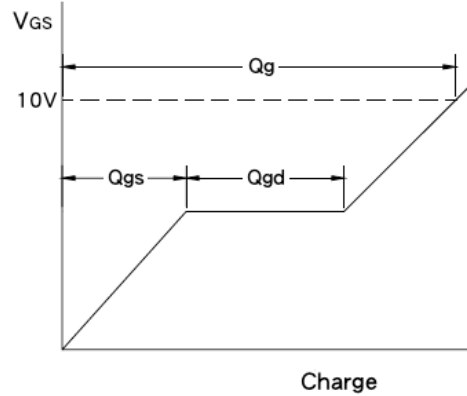
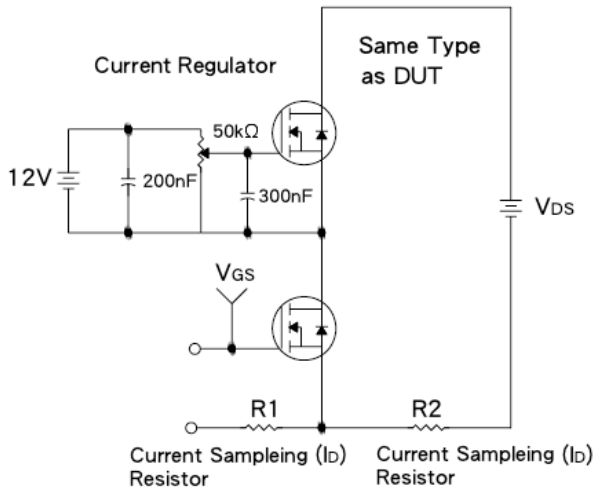
Capacitance vs. Drain-Source Voltage



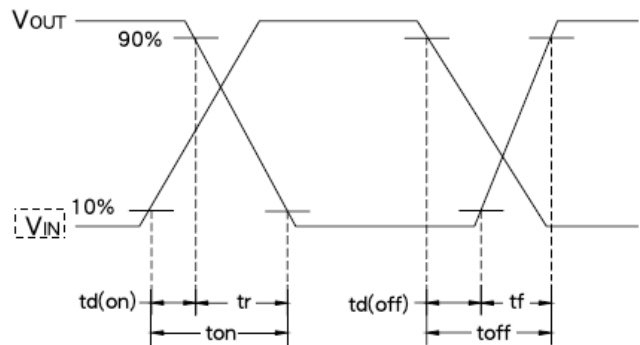
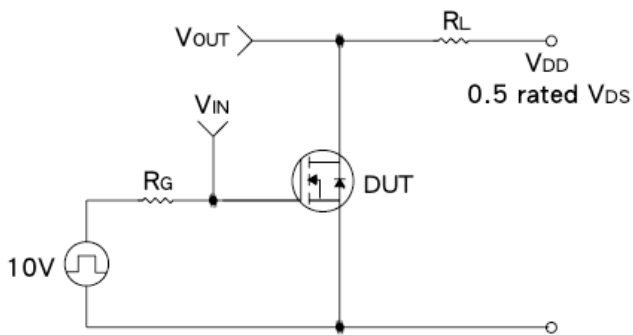
Normalized Thermal Transient Impedance, Junction-to-Ambient



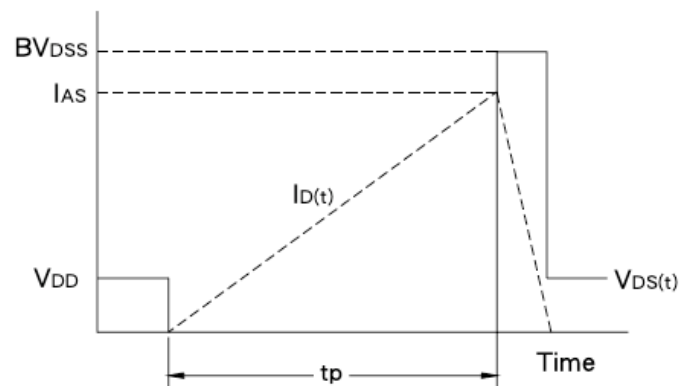
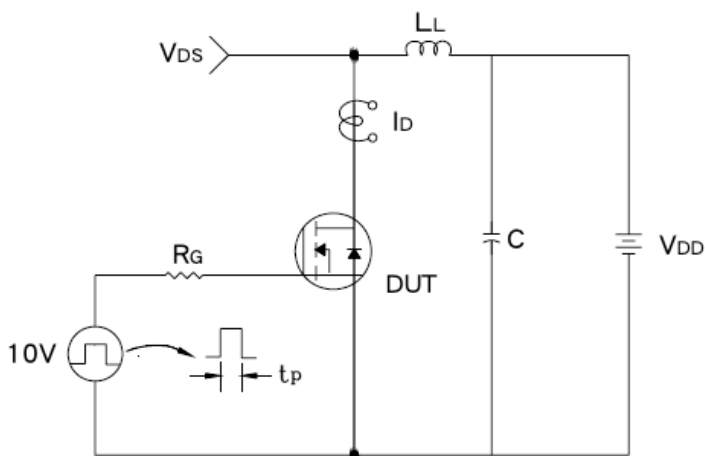
Gate Charge Test Circuit & Waveform



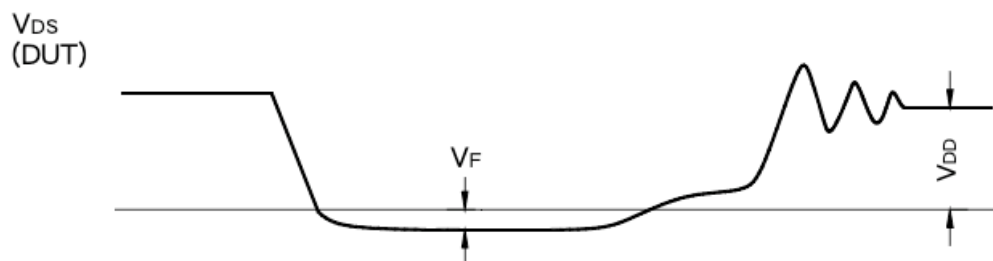
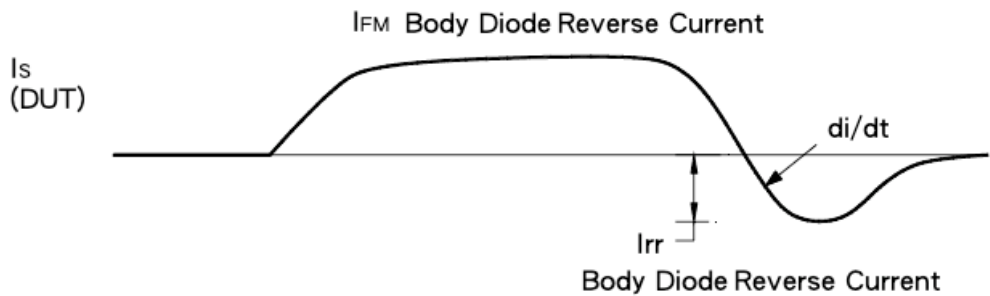
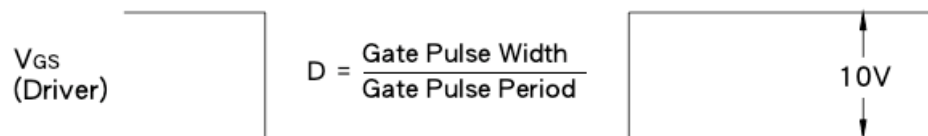
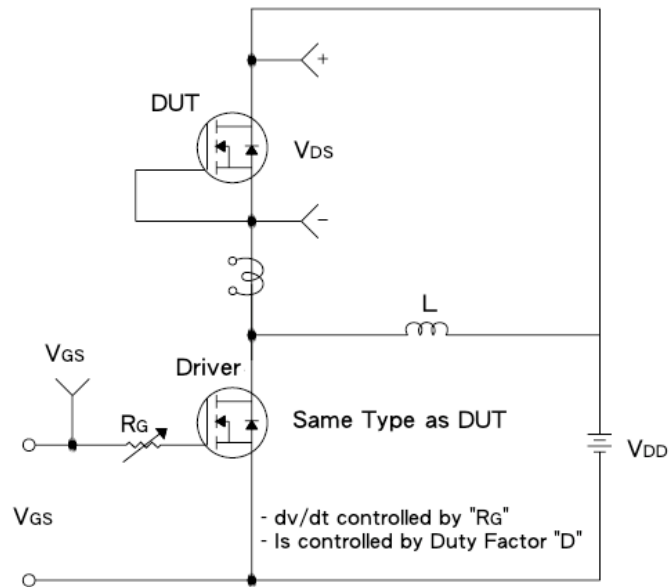
Resistive Switching Test Circuit & Waveform



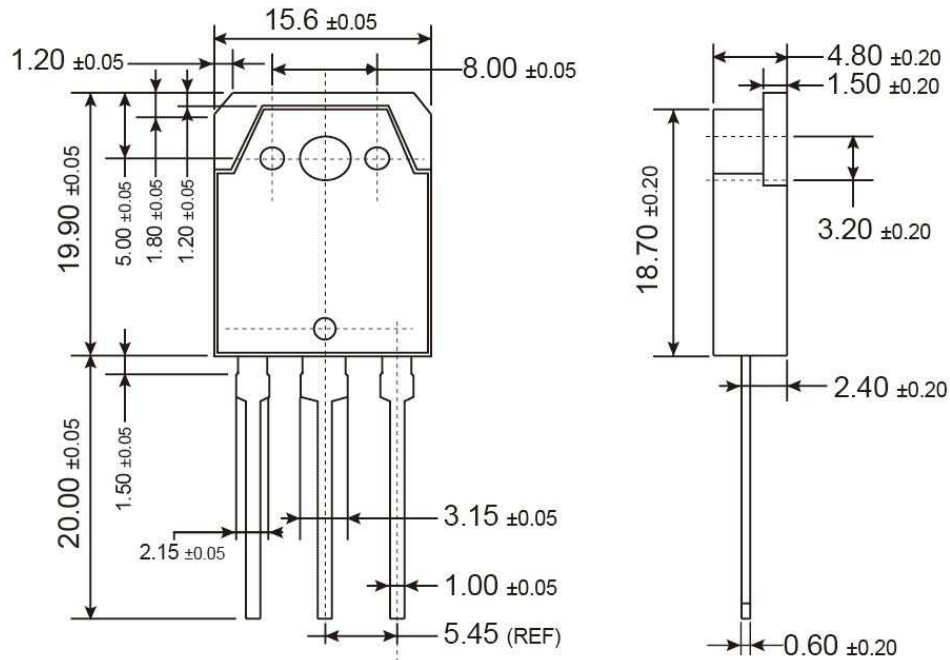
E_{AS} Test Circuit & Waveform



Diode Reverse Recovery Time Test Circuit & Waveform



TO-3PN Mechanical Drawing



Unit: Millimeters

TSM20N50CN

500V N-Channel Power MOSFET

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