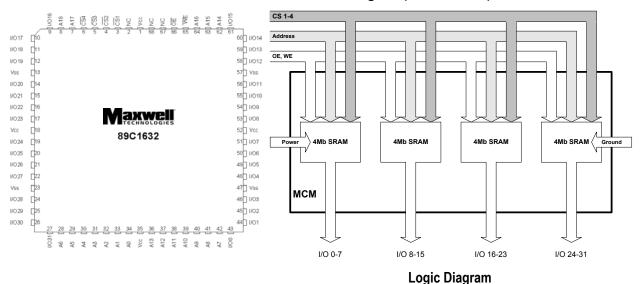


89C1632 16 Megabit (512K x 32-Bit) MCM SRAM

16 Megabit (512k x 32-bit) SRAM MCM



FEATURES:

- Four 512k x 8 SRAM architecture
- Rad-Pak® technology hardens against natural space radiation technology
- · Total dose hardness:
 - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
 - SEL > 68 MeV/mg/cm²
 - SEU threshold = 3 MeV/mg/cm²
 - SEU saturated cross section: 6E-9 cm²/bit
- · Package: 68-pin quad flat package
- · Fast access time: 20, 25 and 30 ns
- Completely static memory no clock or timing strobe required
- Internal bypass capacitor
- High-speed silicon-gate CMOS technology
- 5V or 3V ± 10% power supply
- Equal address and chip enable access times
- Three-state outputs
- · All inputs and outputs are TTL compatible

Description:

Maxwell Technologies' 89C1632 high-performance 16 Megabit Multi-Chip Module (MCM) Static Random Access Memory features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The four 4-Megabyte SRAM die and bypass capacitors are incorporated into a high-reliable hermetic quad flat-pack ceramic package. With high-performance silicon-gate CMOS technology, the 89C1632 reduces power consumption and eliminates the need for external clocks or timing strobes. It is equipped with output enable (OE) and four byte enable (CS1 - CS4) inputs to allow greater system flexibility. When OE input is high, the output is forced to high impedance.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. In a GEO orbit, RAD-PAK provides true greater than 100 krad (Si) total radiation dose tolerance, dependent upon space mission. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or a space mission. This product is available in Class H or Class K packaging and screening.

TABLE 1. PINOUT DESCRIPTION

Pin	Symbol	Description
34-28, 42-36, 62-64, 7, 8	A0-A18	Address Enable
65	WE	WriteEnable
66	ŌĒ	Output Enable
3-6	CS1 - CS4	Chip Enable
43-46, 48-56, 58-61, 9-12, 14-17, 19-22, 24-27	1/00-1/031	Data Input/Output
2, 67, 68	NC	No Connection
1, 18, 35, 52	V _{CC}	+5V Power Supply
13, 23, 47, 57	V _{SS}	Ground

TABLE 2. 89C1632 ABSOLUTE MAXIMUM RATINGS

(Voltage referenced to $V_{SS} = 0V$)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage Relative to V _{SS}	V _{CC}	-0.5	+7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V_{IN}, V_{OUT}	-0.5	V _{CC} +0.5	V
Power Dissipation	P_{D}		4.0	W
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _S	-65	+150	°C

Table 3. 89C1632 Recommended Operating Conditions

(V_{CC} = 5.0 \pm 10%, T_A = -55 to +125 °C, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Supply Voltage, (Operating Voltage Range)	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.5 ⁽¹⁾	V
Input Low Voltage	V _{IL}	-0.5 (2)	0.8	V

^{1.} V_{IH} (max) = V_{CC} + 2V ac (pulse width \leq 10ns) for I \leq 80 mA.

^{2.} V_{IL} (min) = -2.0V ac; (pulse width \leq 20 ns) for I \leq 80 mA.

TABLE 4. 89C1632 CAPACITANCE

 $(f = 1.0 \text{ MHz}, dV = 3.0V, T_A = 25 ^{\circ}C)$

PARAMETER	Symbol	Test Conditions	Max	Units
Input Capacitance ¹	C _{IN}	V _{IN} = 0 V	7 28 7	pF
Input / Output Capacitance ¹	C _{OUT}	V _{I/O} = 0 V	8	pF

^{1.} Guaranteed by design.

Table 5. 89C1632 DC Electrical Characteristics

 $(V_{CC} = 5.0 \pm 10\%, T_A = -55 \text{ to } +125 ^{\circ}\text{C}, \text{ unless otherwise noted})$

Parameter	Symbol	TEST CONDITIONS	Min	Түр	Max	Units
Input Leakage Current	I _{LI}	$V_{IN} = 0$ to V_{CC}	-8.0		+8.0	uA
Output Leakage Current	I _{LO}	$\overline{\text{CS}} = V_{\text{IH}}, V_{\text{OUT}} = V_{\text{SS}} \text{ to } V_{\text{CC}}$	-8.0		+8.0	uA
Average Operating Current Cycle Time:	I _{cc}	Min. Cycle, 100% Duty, $\overline{\text{CS}} = \text{V}_{\text{IL}}, \text{I}_{\text{OUT}}$ = 0 mA				mA
20 ns		$V_{IN} = V_{IH}$ or V_{II}			800	
25 ns					760	
30 ns					720	
Standby Power Supply Current	I _{SB}	CS= V _{IH} , cycle time ≥ 25ns			240	mA
CMOS Standby Power Supply Current	I _{SB1}	$\overline{\text{CS}}$ ≥ V _{CC} - 0.2V, f = 0 MHz, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} < 0.2V			60	mA
Output Low Voltage	V _{OL}	I _{OL} = + 8.0 mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4			V

TABLE 6. 89C1632 AC OPERATING CONDITIONS AND CHARACTERISTICS

 $(V_{CC} = 5.0 \pm 10\%, T_A = -55 \text{ to } +125 ^{\circ}\text{C}, \text{ unless otherwise noted})$

Parameter	Min	Түр	Max	Units
Input Pulse Level	0.0		3.0	V
Output Timing Measurement Reference Level			1.5	V
Input Rise/Fall Time			3.0	ns
Input Timing Measurement Reference Level			1.5	V

TABLE 7. 89C1632 READ CYCLE

(V_{CC} = $5.0 \pm 10\%$, T_A = -55 to +125 °C, unless otherwise noted)

Parameter	Symbol	Min	Түр	Max	Units
Read Cycle Time -20 -25 -30	t _{RC}	20 25 30	 	 	ns
Address Access Time -20 -25 -30	t _{AA}	 	 	20 25 30	ns
Chip Select to Output -20 -25 -30	t _{co}	 	 	20 25 30	ns
Output Enable to Output -20 -25 -30	t _{OE}	 	 	10 12 14	ns
Output Enable to Low-Z Output -20 -25 -30	^t o.z	 	0 0 0	 	ns
Chip Enable to Low-Z Output -20 -25 -30	t _{LZ}	 	3 3 3	 	ns
Output Disable to High-Z Output -20 -25 -30	t _{OHZ}	 	5 6 8	 	ns
Chip Disable to High-Z Output -20 -25 -30	t _{HZ}	 	5 6 8	 	ns
Output Hold from Address Change -20 -25 -30	t _{OH}	3 3 3	 	 	ns

TABLE 8. 89C1632 FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O PIN	SUPPLY CURRENT
Н	X ¹	X ¹	Not Select	High-Z	I _{SB} , I _{SB1}

TABLE 8. 89C1632 FUNCTIONAL DESCRIPTION

CS	WE	ŌĒ	Mode	I/O PIN	SUPPLY CURRENT
L	Н	Н	Output Disable	High-Z	I _{cc}
L	Н	L	Read	D _{OUT}	I _{cc}
L	L	X ¹	Write	D _{IN}	I _{cc}

^{1.} X = don't care.

TABLE 9. 89C1632 WRITE CYCLE

(V_{CC} = 5.0 \pm 10%, T_A = -55 to +125 °C, unless otherwise noted)

PARAMETER	Symbol	Min	Түр	Max	Units
Write Cycle Time -20 -25 -30	t _{wc}	20 25 30			ns
Chip Select to End of Write -20 -25 -30	t _{CW}	14 17 20		 	ns
Address Set-up Time -20 -25 -30	t _{AS}	0 0 0		 	ns
Address Valid to End of Write -20 -25 -30	t _{AW}	14 17 20		 	ns
Write Pulse Width (OE High) -20 -25 -30	t _{WP}	14 17 20		 	ns
Write Pulse Width (OE Low) -20 -25 -30	t _{WP1}	20 25 30		 	ns
Write Recovery Time -20 -25 -30	t _{WR}	0 0 0		 	ns
Write to Output High-Z -20 -25 -30	t _{wHZ}	 	5 7 9	 	ns

TABLE 9. 89C1632 WRITE CYCLE

(V_{CC} = 5.0 \pm 10%, T_A = -55 to +125 °C, unless otherwise noted)

Parameter	Symbol	Min	Түр	Max	Units
Data to Write Time Overlap -25 -30	t _{DW}	10 12 14		 	ns
Data Hold from Write Time -20 -25 -30	t _{DH}	0 0 0		 	ns
End Write to Output Low-Z -20 -25 -30	t _{ow}	 	3 3 3	 	ns

FIGURE 1. AC TEST LOADS

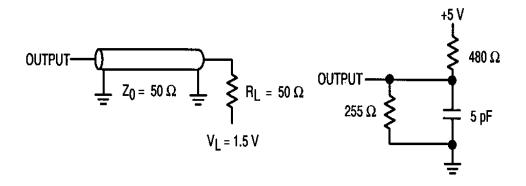


Figure 1A

Figure 1B

FIGURE 2. TIMING WAVEFORM OF READ CYCLE (1) (ADDRESS CONTROLLED)

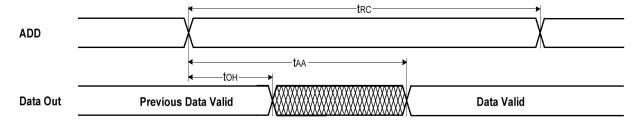
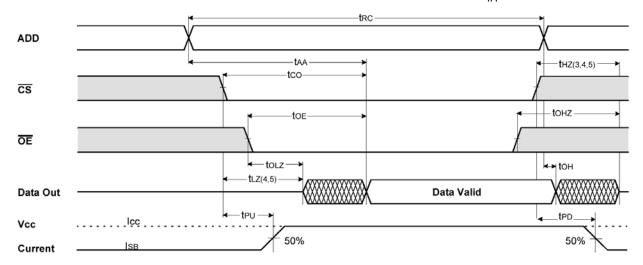


FIGURE 3. TIMING WAVEFORM OF READ CYCLE (2) (WE = VIH)



- 1. WE is high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.

16 Megabit (512K x 32-Bit) MCM SRAM

- 3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OI} levels.
- At any given temperature and voltage conditions, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device.
- 5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with $\overline{CS} = V_{II}$.
- 7. Address valid prior to coincident with $\overline{\text{CS}}$ transition low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

FIGURE 4. TIMING WAVEFORM OF WRITE CYCLE (1) (OE CLOCK)

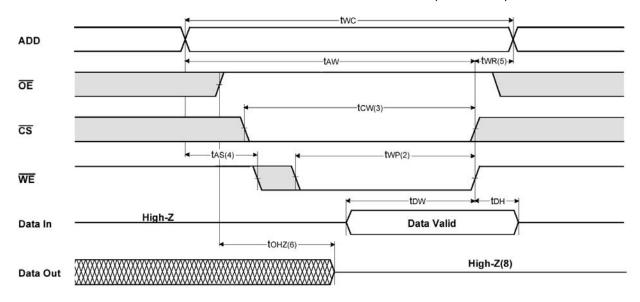


FIGURE 5. TIMING WAVEFORM OF WRITE CYCLE (2) (OE LOW FIIXED)

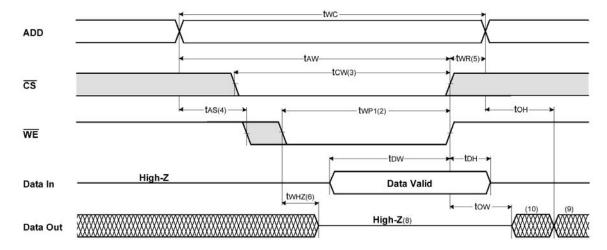
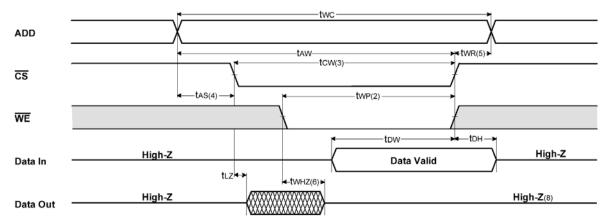


FIGURE 6. TIMING WAVEFORM OF WRITE CYCLE (3) (CS CONTROLLED)



- 1. All write cycle timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- 3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
- 4. t_{AS} is measured from the address valid to the beginning of write.
- 5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
- 6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization of elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CS}}$ foes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. D_{OUT} is the read data of the new address.
- 10.When $\overline{\text{CS}}$ is low, I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FIGURE 7. SRAM HEAVY ION CROSS SECTION

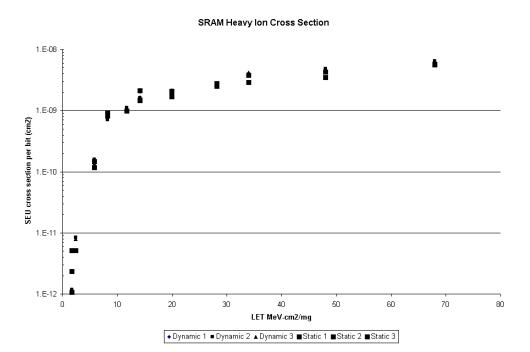
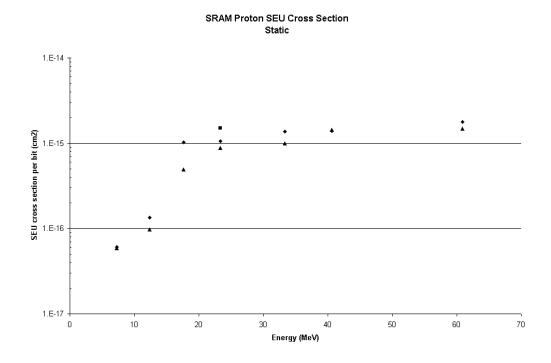
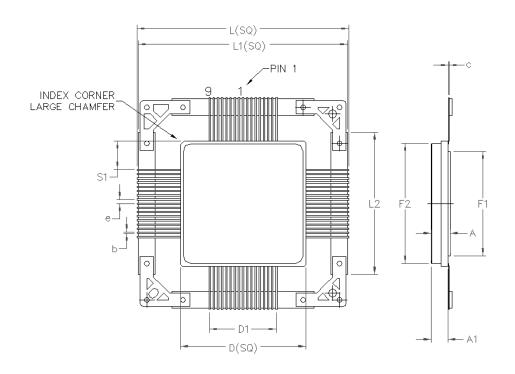


FIGURE 8. SRAM PROTON SEU CROSS SECTION STATIC



10



68 PIN RAD-PAK® QUAD FLAT PACKAGE

Symbol		DIMENSION			
	Min	Nом	Max		
A	0.206	0.225	0.244		
b	0.015	0.017	0.018		
С	0.008	0.009	0.12		
D	1.479	1.494	1.509		
D1	0.800				
е	0.050 BSC				
S1		0.339			
F1	1.239	1.244	1.249		
F2	1.429	1.434	1.439		
L	2.485	2.510	2.545		
L1	2.485	2.500	2.505		
L2	1.690	1.700	1.710		
A1	0.180	0.195	0.210		
N	68				

Q68-04 Note: All dimensions in inches

All data sheets are subject to change without notice

89C1632

16 Megabit (512K x 32-Bit) MCM SRAM

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

16 Megabit (512K x 32-Bit) MCM SRAM

Product Ordering Options

