FAIRCHILD SEMICONDUCTOR®

March 2013

FCD5N60

N-Channel SuperFET® MOSFET

600 V, 4.6 A, 950 mΩ

Features

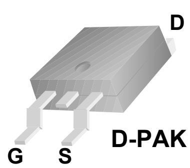
- 650V @T_J = 150°C
- Typ. $R_{DS(on)}$ = 810 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 16 nC)
- Low Effective Output Capacitance (Typ. C_{oss}.eff = 32 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

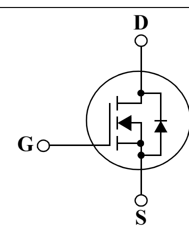
- LCD/LED TV and Monitor
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



D-PAK



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FCD5N60	Unit
V_{DSS}	Drain to Source Voltage		600	V
I_D	Drain Current	-Continuous (T_C = 25°C)	4.6	A
		-Continuous (T_C = 100°C)	2.9	
I_{DM}	Drain Current	- Pulsed (Note 1)	13.8	A
V_{GSS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		159	mJ
I_{AR}	Avalanche Current (Note 1)		4.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		5.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	54	W
		- Derate above 25°C	0.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCD5N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	83	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD5N60	FCD5N60TM	D-PAK	380mm	16m	2500
FCD5N60	FCD5N60TF	D-PAK	380mm	16m	2000

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_C = 25^{o}C	600	-	-	V
		V_{GS} = 0 V, I_D = 250 μA, T_C = 150^{o}C	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25^{o}C	-	0.6	-	V/^{o}C
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 4.6 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, T_C = 125^{o}C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.3 A	-	0.81	0.95	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 2.3 A (Note 4)	-	3.8	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	-	470	600	pF
C_{oss}	Output Capacitance		-	250	320	pF
C_{rss}	Reverse Transfer Capacitance		-	22	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1.0 MHz	-	12	-	pF
C_{oss}eff.	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	32	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 4.6 A, R_G = 25 Ω (Note 4, 5)	-	12	30	ns
t_r	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	47	95	ns
t_f	Turn-Off Fall Time		-	22	55	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 480 V, I_D = 4.6 A, V_{GS} = 10 V (Note 4, 5)	-	16	-	nC
Q_{gs}	Gate to Source Gate Charge		-	2.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.8	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4.6 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4.6 A, dI_F/dt = 100 A/μs (Note 4)	-	295	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.7	-	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 2.3 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

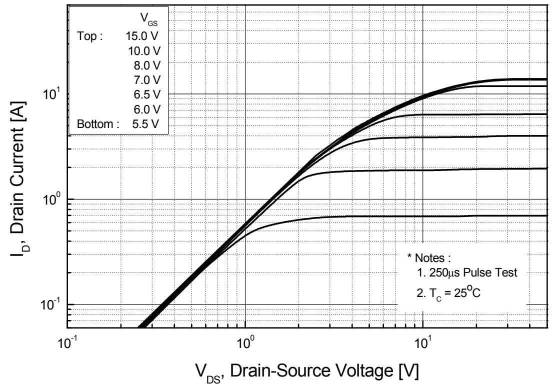


Figure 2. Transfer Characteristics

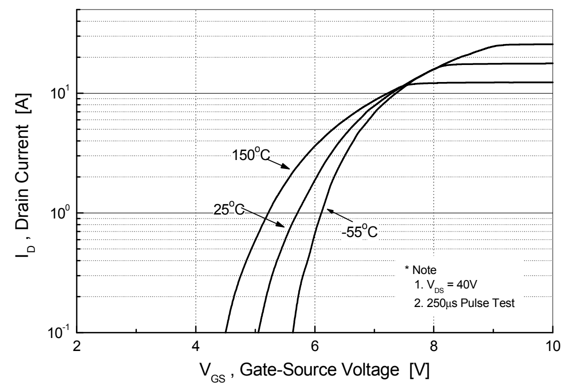


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

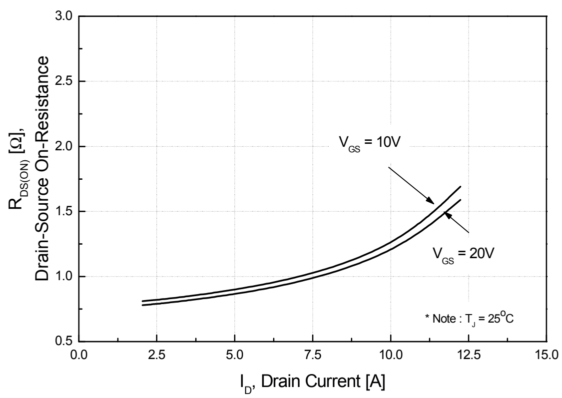


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

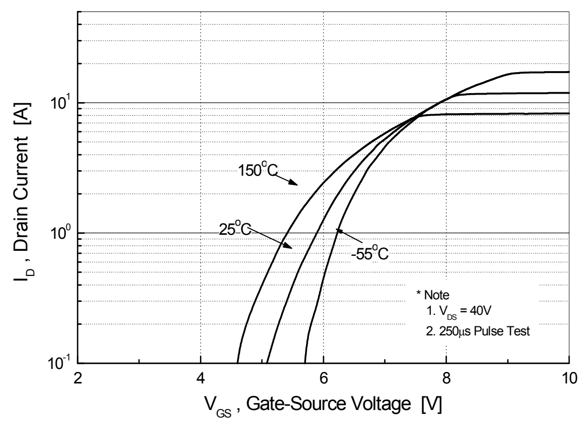


Figure 5. Capacitance Characteristics

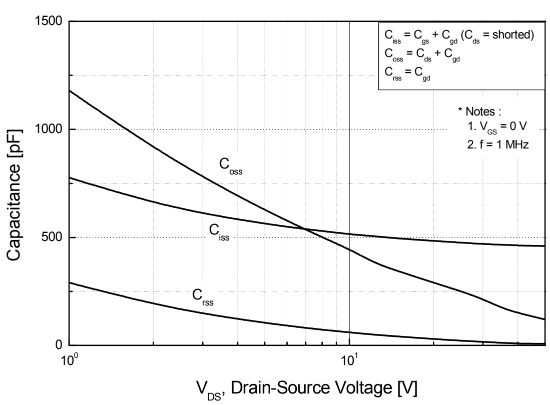
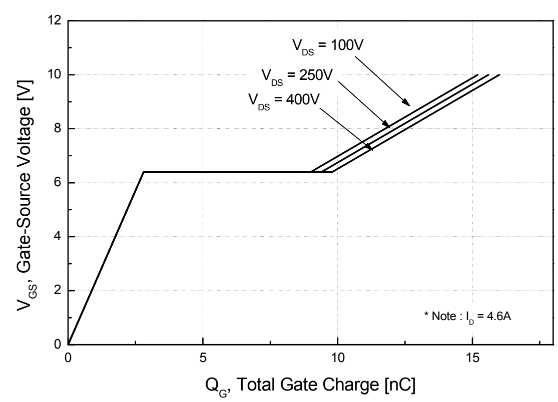


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

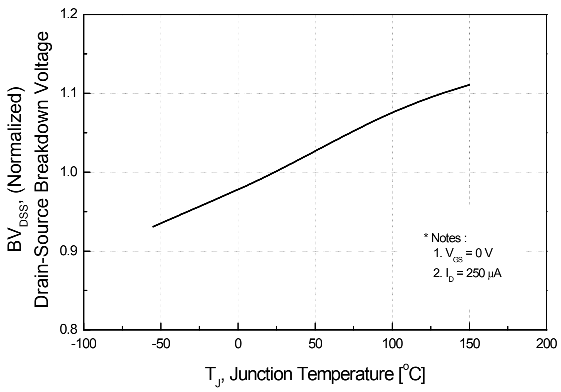


Figure 8. On-Resistance Variation vs. Temperature

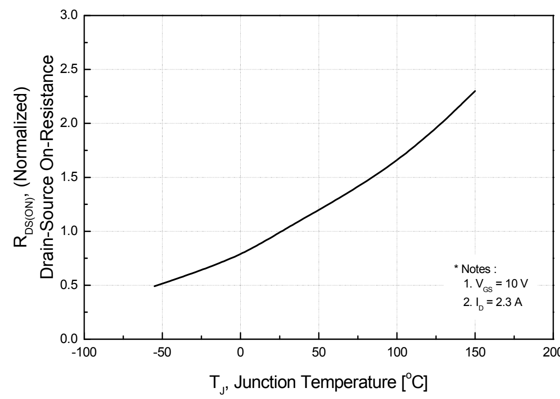


Figure 9. Maximum Safe Operating Area

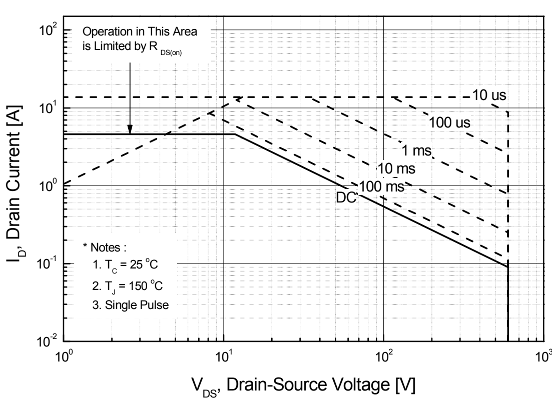


Figure 10. Maximum Drain Current vs. Case Temperature

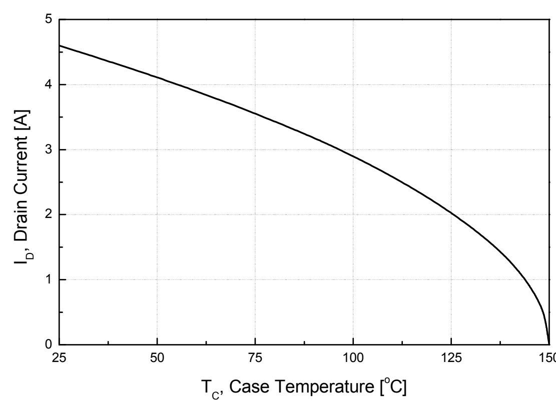
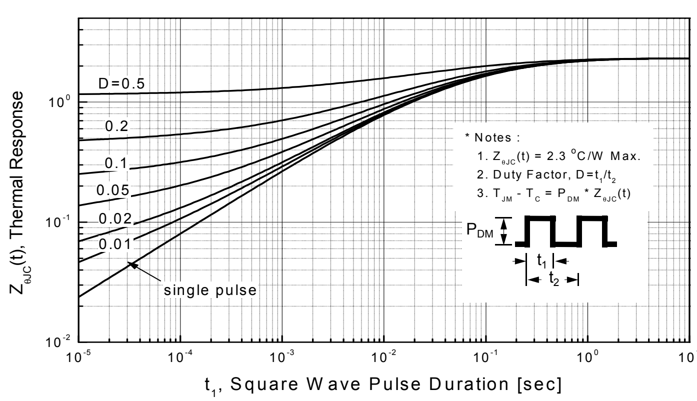
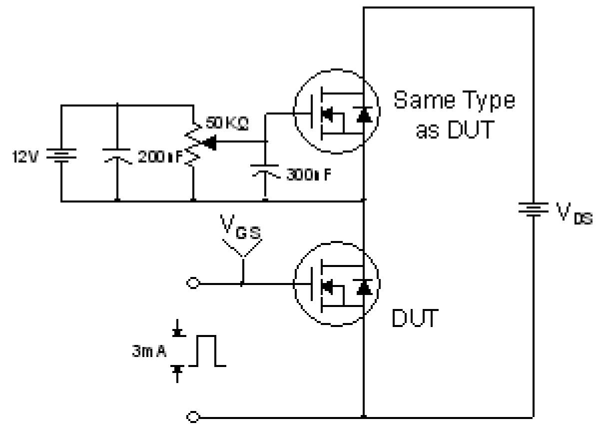
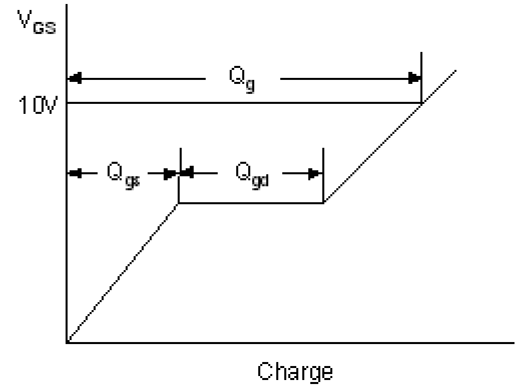


Figure 11. Transient Thermal Response Curve

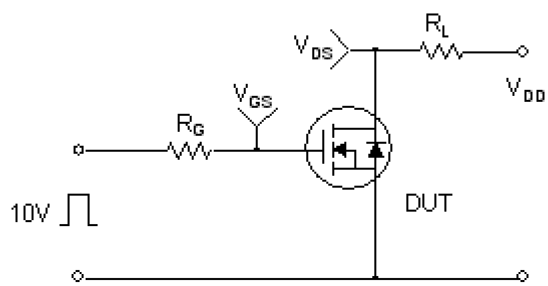


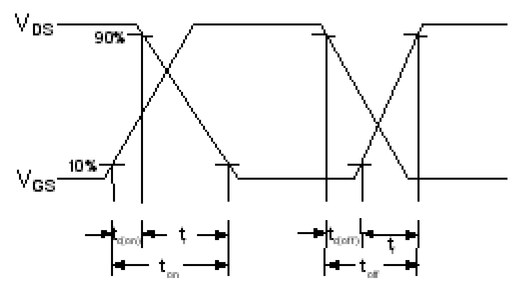
Gate Charge Test Circuit & Waveform



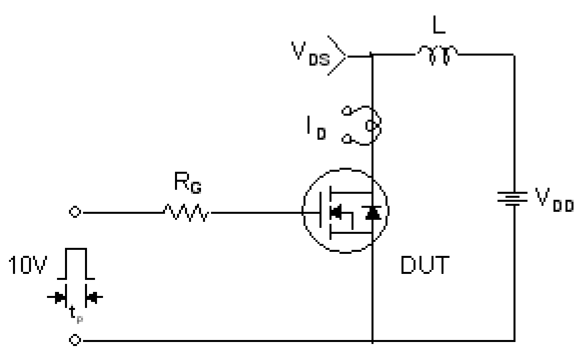


Resistive Switching Test Circuit & Waveforms

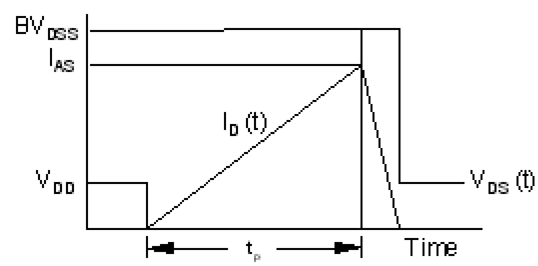




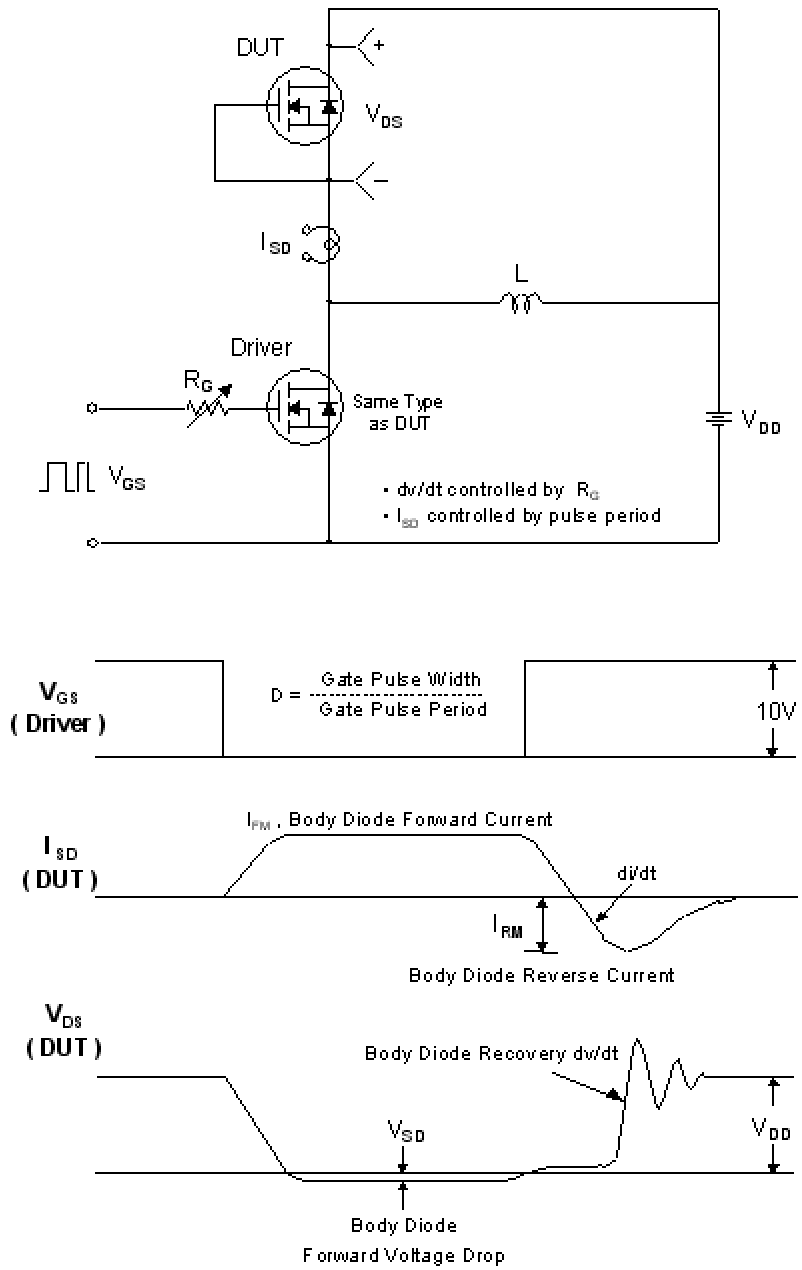
Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

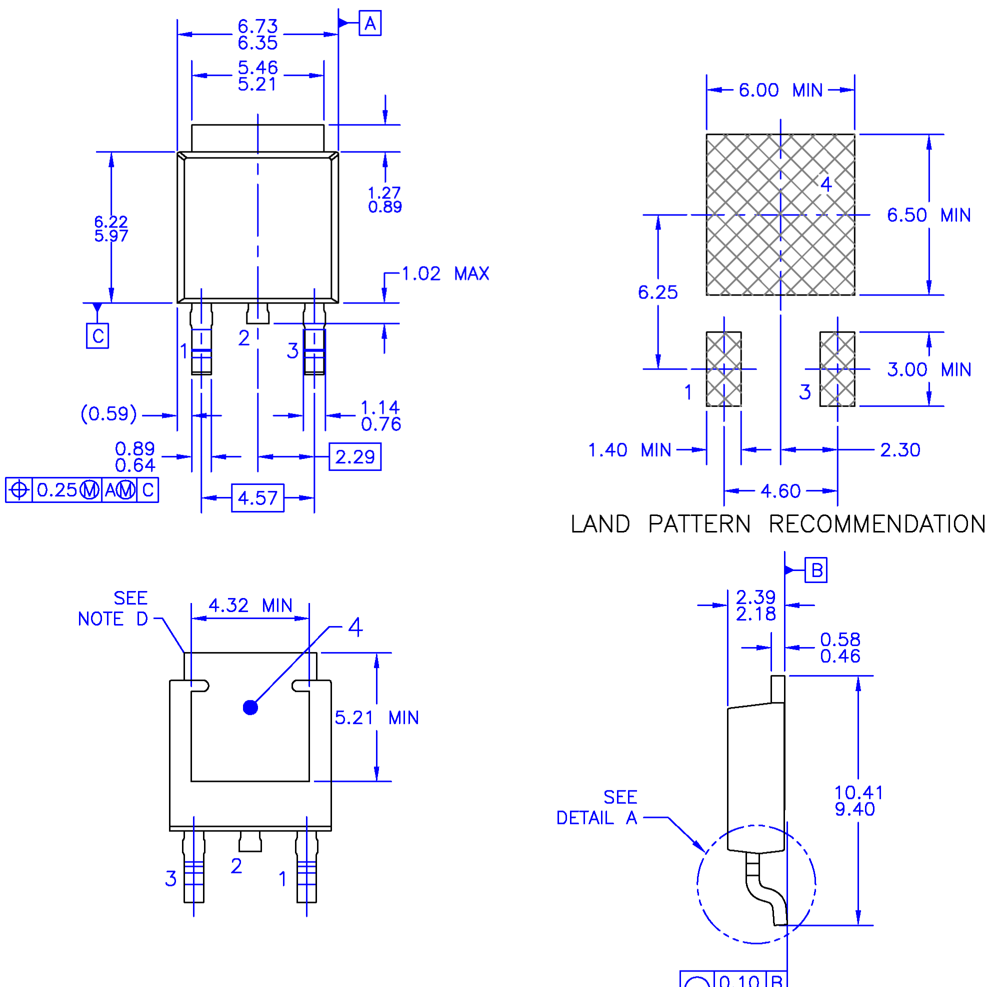


Peak Diode Recovery dv/dt Test Circuit & Waveforms

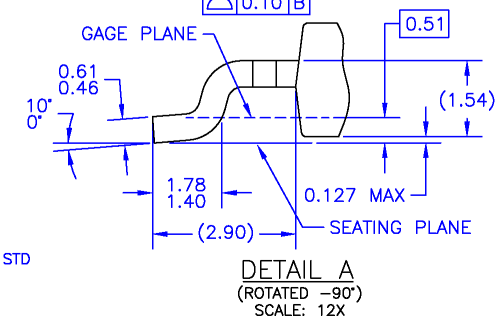


Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO–252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238–3N.
- H) DRAWING NUMBER AND REVISION: MKT–TO252A03REV8



Dimensions in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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