

**40V COMPLEMENTARY DUAL ENHANCEMENT MODE MOSFET**

**Product Summary**

Device	V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> Max	I <sub>D</sub> T <sub>A</sub> = +25°C
Q1	40V	28mΩ @ V <sub>GS</sub> = 10V	7.2A
		49mΩ @ V <sub>GS</sub> = 4.5V	5.4A
Q2	-40V	50mΩ @ V <sub>GS</sub> = -10V	-5.2A
		79mΩ @ V <sub>GS</sub> = -4.5V	-4.7A

**Description**

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.


**Applications**

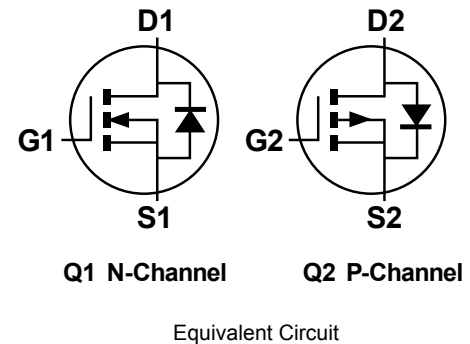
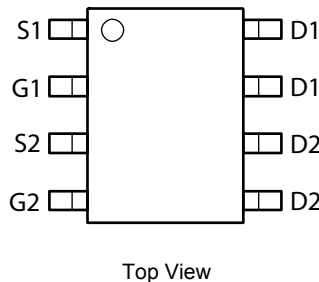
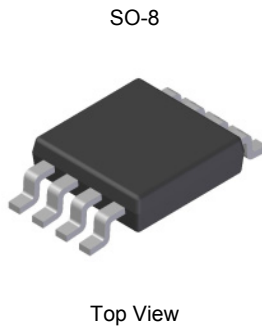
- Motor Control
- Backlighting
- DC-DC Converters
- Power Management Functions

**Features and Benefits**

- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.074 grams (approximate)

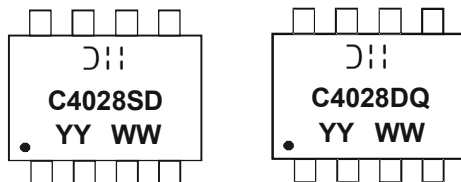


**Ordering Information** (Note 4)

Part Number	Compliance	Case	Packaging
DMC4028SSD-13	Standard	SO-8	2500 / Tape & Reel
DMC4028SSDQ-13	Automotive	SO-8	2500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



Dii = Manufacturer's Marking  
 C4028SD = Product Type Marking Code for DMC4028SSD-13  
 C4028DQ = Product Type Marking Code for DMC4028SSDQ-13  
 YYWW = Date Code Marking  
 YY = Year (ex: 09 = 2009)  
 WW = Week (01 - 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

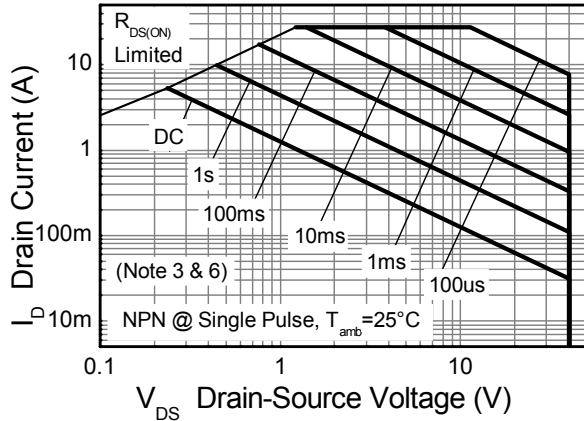
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage		V <sub>DSS</sub>	40	-40	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	±20	V
Continuous Drain Current	V <sub>GS</sub> = 10V	(Notes 7 & 9)	7.2	5.2	A
		T <sub>A</sub> = 70°C (Notes 7 & 9)	5.5	4.2	
		(Notes 6 & 9)	5.4	4	
		(Notes 6 & 10)	6.5	4.8	
Pulsed Drain Current	V <sub>GS</sub> = 10V	I <sub>DM</sub>	27.3	20.4	A
Continuous Source Current (Body diode)		I <sub>S</sub>	3.35	3.15	A
Pulsed Source Current (Body diode)		I <sub>SM</sub>	27.3	20.4	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

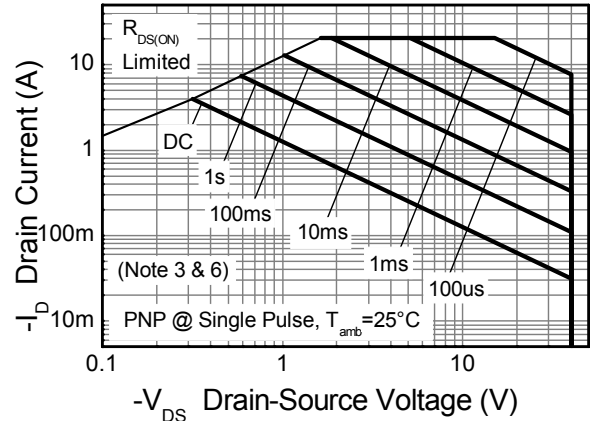
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 6 & 9)	P <sub>D</sub>	1.25		W mW/°C
			10		
	(Notes 6 & 10)		1.8		
			14.3		
Thermal Resistance, Junction to Ambient	(Notes 6 & 9)	R <sub>θJA</sub>	2.16		°C/W
	(Notes 6 & 10)		17.2		
	(Notes 7 & 9)		100		
Thermal Resistance, Junction to Lead	(Notes 6 & 10)	R <sub>θJL</sub>	70		°C/W
	(Notes 7 & 9)		58		
Thermal Resistance, Junction to Lead		(Notes 9 & 11)	53	53	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150		°C

- Notes:
5. AEC-Q101 V<sub>GS</sub> maximum is ±16V.
  6. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  7. Same as note (5), except the device is measured at t ≤ 10 sec.
  8. Same as note (5), except the device is pulsed with D= 0.02 and pulse width 300 μs. The pulse current is limited by the maximum junction temperature.
  9. For a dual device with one active die.
  10. For a device with two active die running at equal power.
  11. Thermal resistance from junction to solder-point (at the end of the drain lead).

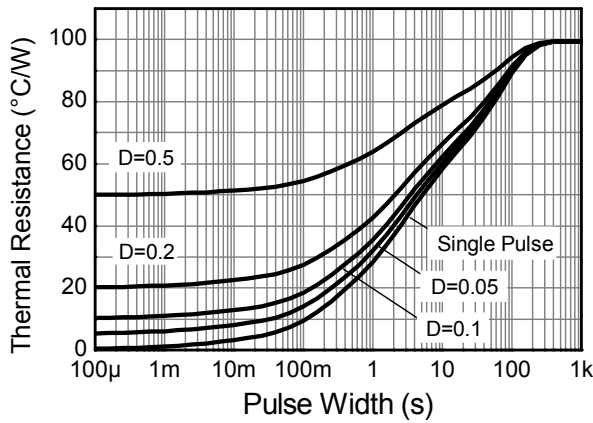
**Thermal Characteristics**



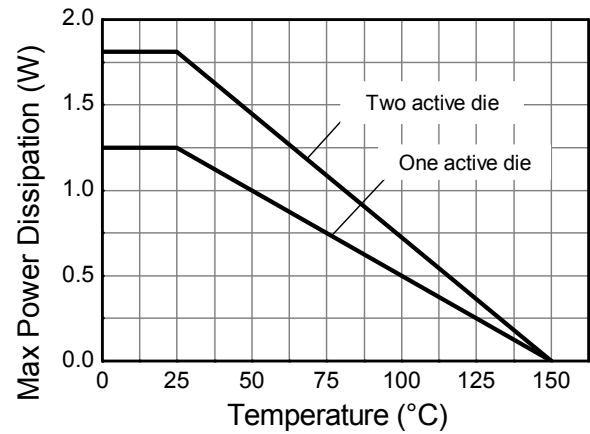
**N-channel Safe Operating Area**



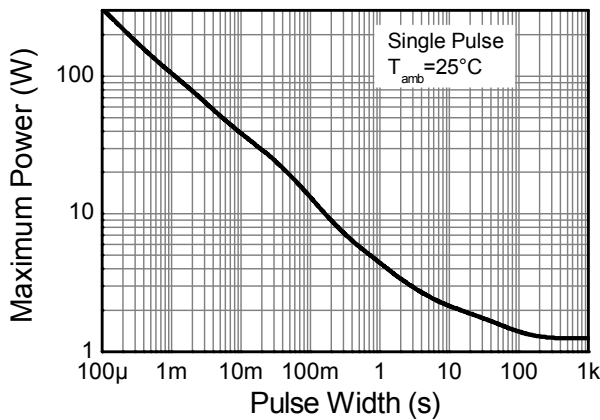
**P-channel Safe Operating Area**



**Transient Thermal Impedance**



**Derating Curve**



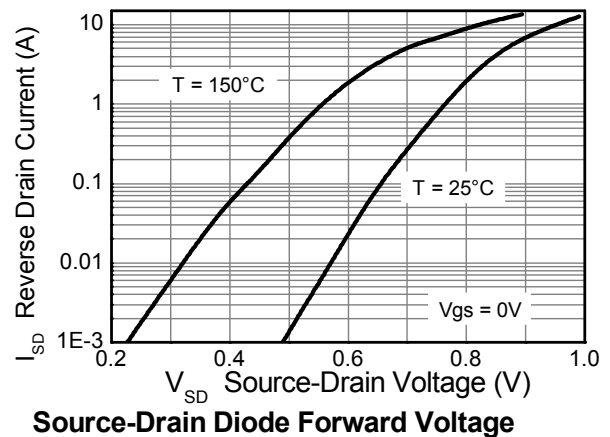
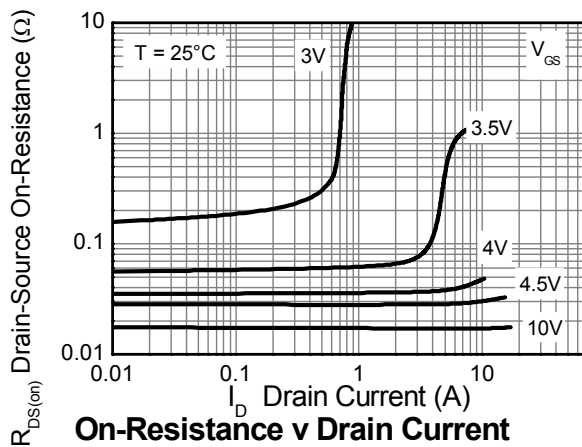
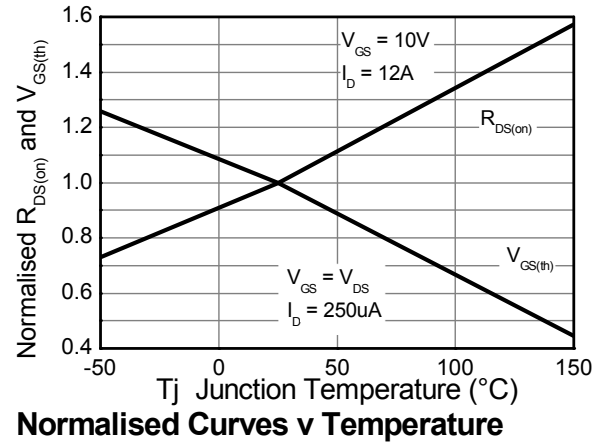
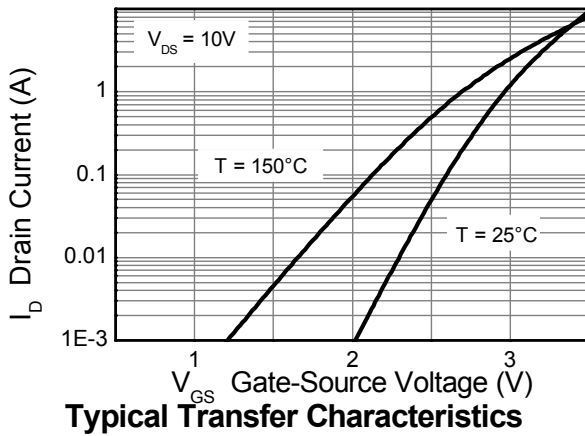
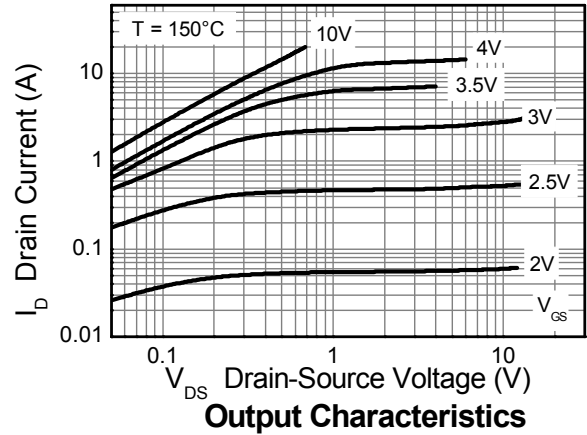
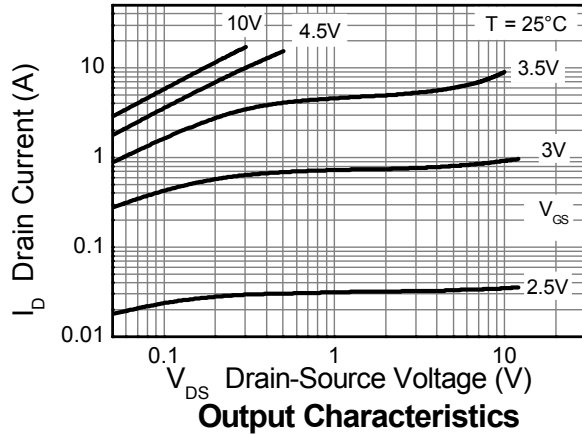
**Pulse Power Dissipation**

**Electrical Characteristics – Q1 N-Channel** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

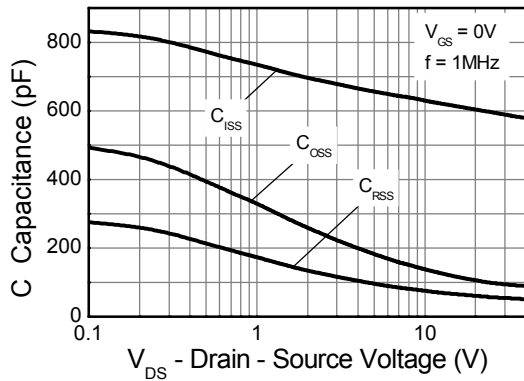
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	40	—	—	V	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	0.5	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.0	—	3.0	V	I <sub>D</sub> = 250μA, V <sub>DS</sub> = V <sub>GS</sub>
Static Drain-Source On-Resistance (Note 12)	R <sub>DS(on)</sub>	—	0.018	0.028	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A
			0.033	0.049		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A
Forward Transconductance (Notes 12 & 13)	g <sub>fs</sub>	—	22.8	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 6A
Diode Forward Voltage (Note 12)	V <sub>SD</sub>	—	0.845	1.1	V	I <sub>S</sub> = 6A, V <sub>GS</sub> = 0V
Reverse recovery time (Note 13)	t <sub>rr</sub>	—	135	—	ns	I <sub>S</sub> = 6A, di/dt = 100A/μs
Reverse recovery charge (Note 13)	Q <sub>rr</sub>	—	799	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 13)</b>						
Input Capacitance	C <sub>iSS</sub>	—	604	—	pF	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	106	—	pF	
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	59.6	—	pF	
Total Gate Charge (Note 14)	Q <sub>g</sub>	—	6.5	—	nC	V <sub>GS</sub> = 4.5V
Total Gate Charge (Note 14)	Q <sub>g</sub>	—	12.9	—	nC	V <sub>GS</sub> = 10V
Gate-Source Charge (Note 14)	Q <sub>gs</sub>	—	2.3	—	nC	
Gate-Drain Charge (Note 14)	Q <sub>gd</sub>	—	3.6	—	nC	
Turn-On Delay Time (Note 14)	t <sub>D(on)</sub>	—	4.2	—	ns	V <sub>DD</sub> = 20V, V <sub>GS</sub> = 10V I <sub>D</sub> = 6A, R <sub>G</sub> ≅ 6.0Ω
Turn-On Rise Time (Note 14)	t <sub>r</sub>	—	12.4	—	ns	
Turn-Off Delay Time (Note 14)	t <sub>D(off)</sub>	—	13.8	—	ns	
Turn-Off Fall Time (Note 14)	t <sub>f</sub>	—	10.7	—	ns	

- Notes:
- 12. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
  - 13. For design aid only, not subject to production testing.
  - 14. Switching characteristics are independent of operating junction temperatures.

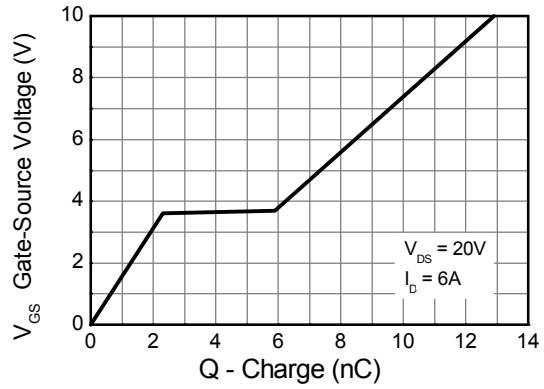
**Typical Characteristics – Q1 N-Channel**



**Typical Characteristics – Q1 N-Channel - (cont.)**

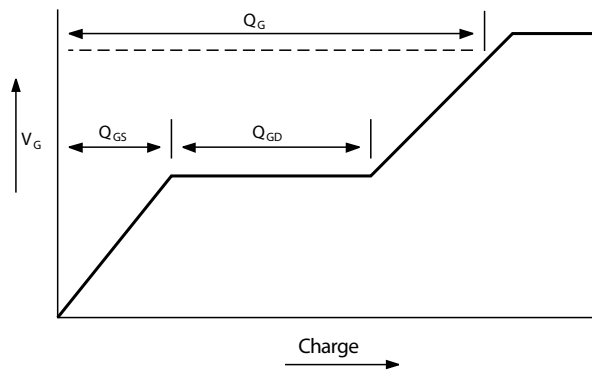


**Capacitance v Drain-Source Voltage**

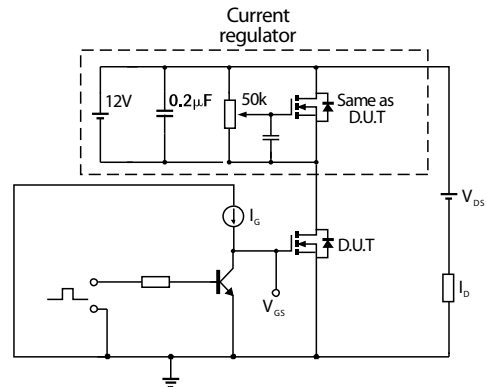


**Gate-Source Voltage v Gate Charge**

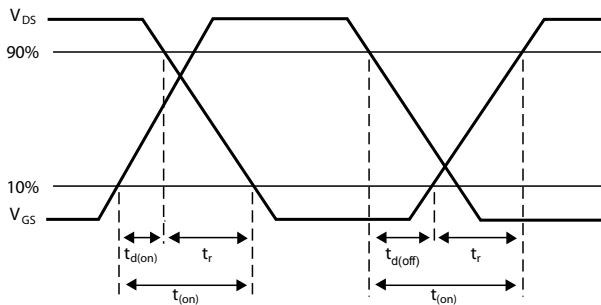
**Test Circuits – Q1 N-Channel**



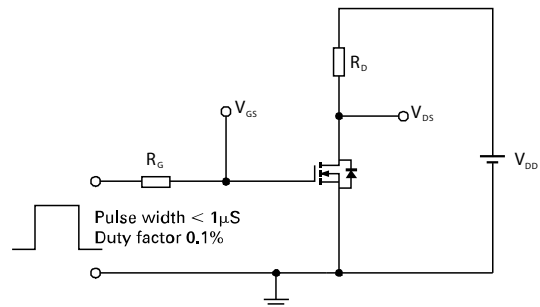
**Basic gate charge waveform**



**Gate charge test circuit**



**Switching time waveforms**



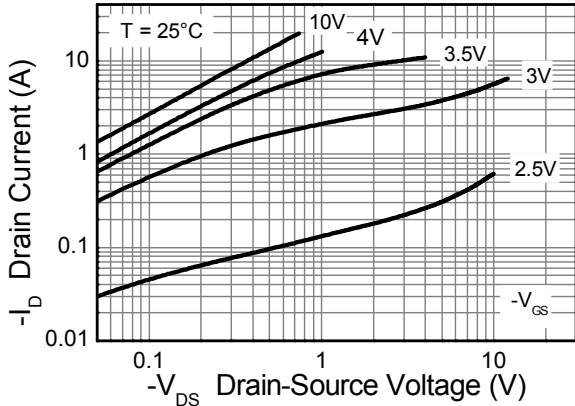
**Switching time test circuit**

**Electrical Characteristics – Q2 P-Channel** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

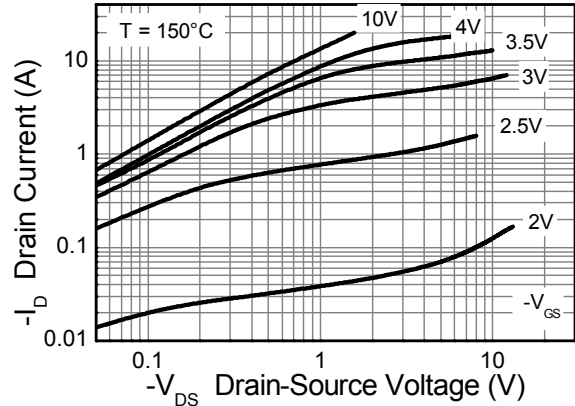
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	—	—	V	$I_D = -250 \mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-0.5	$\mu\text{A}$	$V_{DS} = -40\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-3.0	V	$I_D = -250 \mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 12)	$R_{DS(on)}$	—	0.039	0.050	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -6\text{A}$
			0.060	0.079		$V_{GS} = -4.5\text{V}$ , $I_D = -5\text{A}$
Forward Transconductance (Notes 12 & 13)	$g_{fs}$	—	16.6	—	S	$V_{DS} = -15\text{V}$ , $I_D = -6\text{A}$
Diode Forward Voltage (Note 13)	$V_{SD}$	—	-0.865	-1.1	V	$I_S = -6\text{A}$ , $V_{GS} = 0\text{V}$
Reverse Recovery Time (Note 13)	$t_{rr}$	—	138	—	ns	$I_S = -6\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge (Note 13)	$Q_{rr}$	—	841	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 13)</b>						
Input Capacitance	$C_{iss}$	—	674	—	pF	$V_{DS} = -20\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	115	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	67.7	—	pF	
Total Gate Charge (Note 14)	$Q_g$	—	7.0	—	nC	$V_{GS} = -4.5\text{V}$
Total Gate Charge (Note 14)	$Q_g$	—	14	—	nC	$V_{GS} = -10\text{V}$
Gate-Source Charge (Note 14)	$Q_{gs}$	—	2.2	—	nC	
Gate-Drain Charge (Note 14)	$Q_{gd}$	—	3.7	—	nC	
Turn-On Delay Time (Note 14)	$t_{D(on)}$	—	2.3	—	ns	$V_{DD} = -20\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -6\text{A}$ , $R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 14)	$t_r$	—	14.1	—	ns	
Turn-Off Delay Time (Note 14)	$t_{D(off)}$	—	25.1	—	ns	
Turn-Off Fall Time (Note 14)	$t_f$	—	14.3	—	ns	

- Notes:
- 12. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
  - 13. For design aid only, not subject to production testing.
  - 14. Switching characteristics are independent of operating junction temperatures.

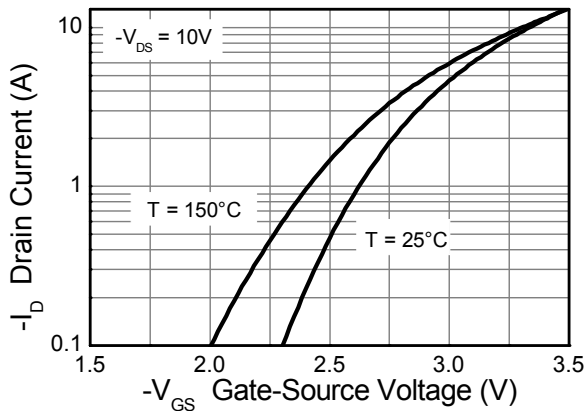
**Typical Characteristics – Q2 P-Channel**



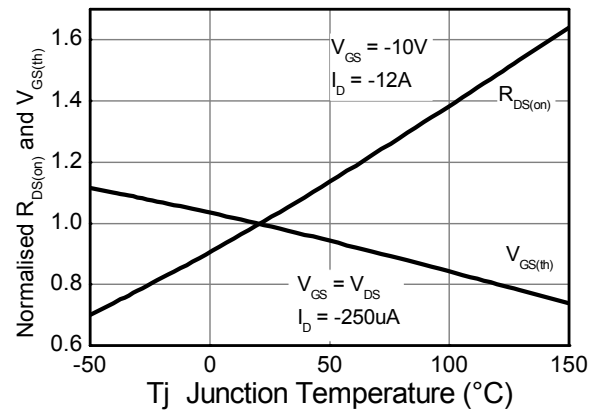
**Output Characteristics**



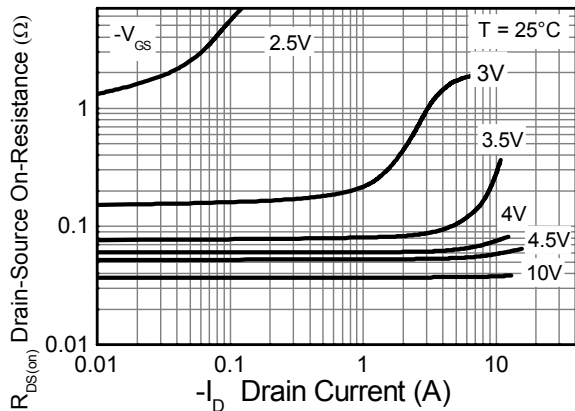
**Output Characteristics**



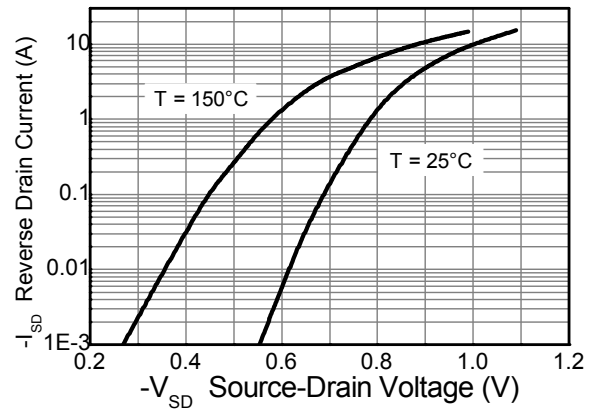
**Typical Transfer Characteristics**



**Normalised Curves v Temperature**



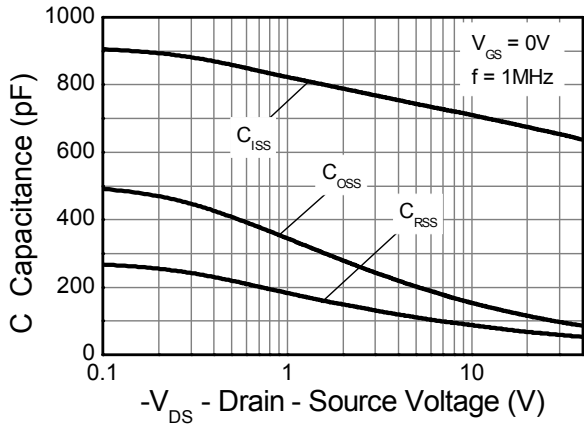
**On-Resistance v Drain Current**



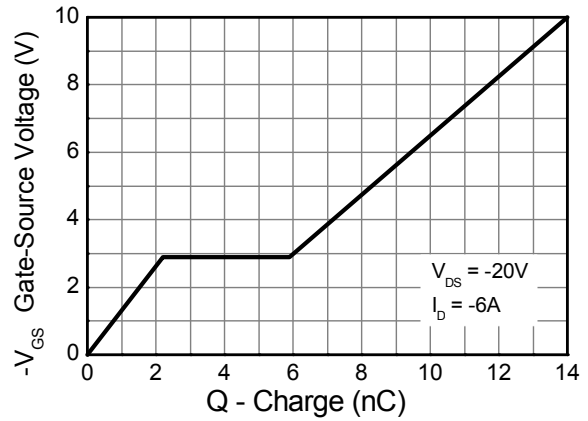
**Source-Drain Diode Forward Voltage**



**Typical Characteristics – Q2 P-Channel – (cont.)**

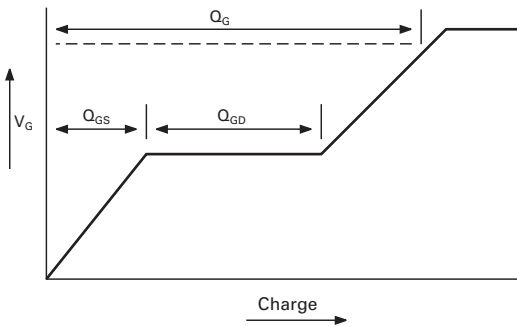


**Capacitance v Drain-Source Voltage**

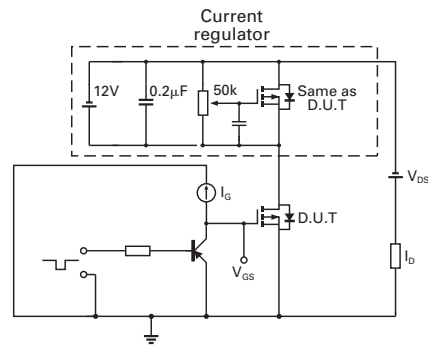


**Gate-Source Voltage v Gate Charge**

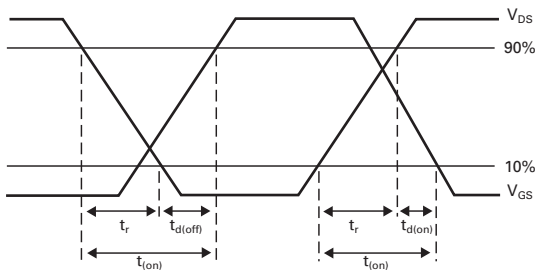
**Test Circuits – Q2 P-Channel**



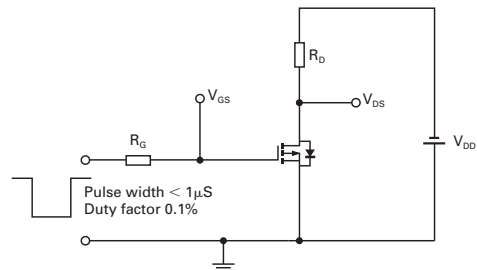
**Basic gate charge waveform**



**Gate charge test circuit**



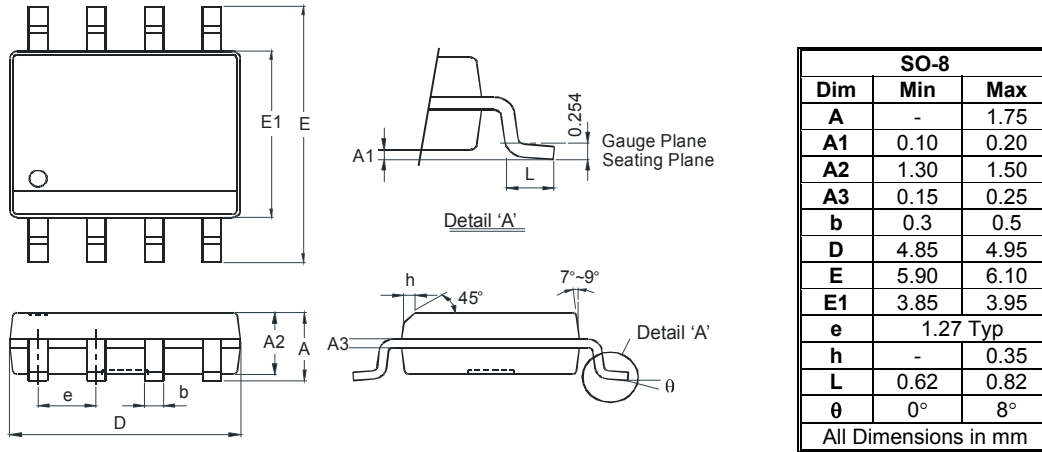
**Switching time waveforms**



**Switching time test circuit**

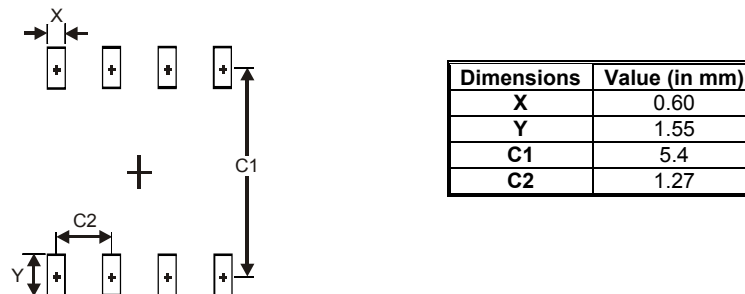
## Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



## Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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