



ON Semiconductor®

<http://onsemi.com>

LV8713T

Bi-CMOS LSI

PWM Constant-Current Control Stepping Motor Driver

Overview

The LV8713T is a stepping motor driver of the micro-step drive corresponding to supports 8W 1-2 phase excitation. It is the best for the drive of the stepping motor for a scanner and a small printer.

Features

- Single-channel PWM constant-current control stepping motor driver incorporated.
- Control mode can be set to 2-phase, 1-2 phase, 4W1-2 phase, or 8W1-2 phase
- Microstep can control easily by the CLK-IN input.
- Power-supply voltage of motor : VM max = 18V
- Output current : IO max = 0.8A
- Output ON resistance : RON = 1.1Ω (upper and lower total, typical, Ta = 25°C)
- A thermal shutdown circuit and a low voltage detecting circuit are built into.

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|---------|-------------------------------|-------------------|------|
| Motor supply voltage | VM max | | 18 | V |
| Logic supply voltage | VCC max | | 6 | V |
| Output peak current | IO peak | Each 1ch, tw ≤ 10ms, duty 20% | 1.0 | A |
| Output continuousness current | IO max | Each 1ch | 800 | mA |
| Logic input voltage | VIN | | -0.3 to VCC + 0.3 | V |
| Allowable power dissipation | Pd max | * | 1.35 | W |
| Operating temperature | Topr | | -20 to +85 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Specified circuit board : 57.0mm×57.0mm×1.7mm, glass epoxy 2-layer board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LV8713T

Allowable Operating Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------|--------|------------|-----------------|------|
| Motor supply voltage range | VM | | 4 to 16 | V |
| Logic supply voltage range | VCC | | 2.7 to 5.5 | V |
| Logic input voltage | VIN | | -0.3 to VCC+0.3 | V |
| VREF input voltage range | VREF | | 0 to VCC-1.8 | V |

Electrical Characteristics at Ta = 25°C, VM = 12V, VCC = 3.3V, VREF = 1.0V

| Parameter | Symbol | Conditions | Ratings | | | Unit | |
|---|-------------------|--|--|-------|-------|-------|---|
| | | | min | typ | max | | |
| Standby mode current drain | IMstn | PS = "L", no load | | | 1 | μA | |
| | ICCstn | PS = "L", no load | | | 1 | μA | |
| Current drain | IM | PS = "H", no load | 0.3 | 0.5 | 0.7 | mA | |
| | ICC | PS = "H", no load | 0.9 | 1.3 | 1.7 | mA | |
| Thermal shutdown temperature | TSD | Design guarantee | | 180 | | °C | |
| Thermal hysteresis width | ΔTSD | Design guarantee | | 40 | | °C | |
| VCC low voltage cutting voltage | VthVCC | | 2.1 | 2.4 | 2.7 | V | |
| Low voltage hysteresis voltage | VthHIS | | 100 | 130 | 160 | mV | |
| REG5 output voltage | Vreg5 | IO = -1mA | 4.5 | 5 | 5.5 | V | |
| Output on resistance | RonU | IO = -800mA, Source-side on resistance | | 0.78 | 1.0 | Ω | |
| | RonD | IO = 800mA, Sink-side on resistance | | 0.32 | 0.43 | Ω | |
| Output leakage current | IOleak | VO = 15V | | | 10 | μA | |
| Diode forward voltage | VD | ID = -800mA | | 1.0 | 1.2 | V | |
| Logic pin input current | IINL | VIN = 0.8V | 4 | 8 | 12 | μA | |
| | IINH | VIN = 3.3V | 22 | 33 | 45 | μA | |
| Logic high-level input voltage | VINH | | 2.0 | | | V | |
| Logic low-level input voltage | VINL | | | | 0.8 | V | |
| VREF input current | IREF | VREF = 1.0V | -0.5 | | | μA | |
| Current setting comparator threshold voltage (current attenuation rate switching) | Vtatt00 | ATT1 = L, ATT2 = L | 0.191 | 0.200 | 0.209 | V | |
| | Vtatt01 | ATT1 = H, ATT2 = L | 0.152 | 0.160 | 0.168 | V | |
| | Vtatt10 | ATT1 = L, ATT2 = H | 0.112 | 0.120 | 0.128 | V | |
| | Vtatt11 | ATT1 = H, ATT2 = H | 0.072 | 0.080 | 0.088 | V | |
| Chopping frequency | Fchop | Cchop = 220pF | 36 | 45 | 54 | kHz | |
| CHOP pin threshold voltage | VCHOPH | | 0.6 | 0.7 | 0.8 | V | |
| | VCHOPL | | 0.17 | 0.2 | 0.23 | V | |
| CHOP pin charge/discharge current | Ichop | | 7 | 10 | 13 | μA | |
| MONI pin saturation voltage | Vsatmon | Imoni = 1mA | | 250 | 400 | mV | |
| Current setting comparator threshold voltage (current step switching) | 8W1-2-phase drive | Vtdac0_2W | Step 0 (When initialized : channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac1_8W | Step 1 (Initial state+1) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac2_8W | Step 2 (Initial state+2) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac3_8W | Step 3 (Initial state+3) | 0.189 | 0.198 | 0.207 | V |
| | | Vtdac4_8W | Step 4 (Initial state+4) | 0.187 | 0.196 | 0.205 | V |
| | | Vtdac5_8W | Step 5 (Initial state+5) | 0.185 | 0.194 | 0.203 | V |
| | | Vtdac6_8W | Step 6 (Initial state+6) | 0.183 | 0.192 | 0.201 | V |
| | | Vtdac7_8W | Step 7 (Initial state+7) | 0.179 | 0.188 | 0.197 | V |
| | | Vtdac8_8W | Step 8 (Initial state+8) | 0.175 | 0.184 | 0.193 | V |
| | | Vtdac9_8W | Step 9 (Initial state+9) | 0.171 | 0.180 | 0.189 | V |
| | | Vtdac10_8W | Step 10 (Initial state+10) | 0.167 | 0.176 | 0.185 | V |
| | | Vtdac11_8W | Step 11 (Initial state+11) | 0.163 | 0.172 | 0.181 | V |
| | | Vtdac12_8W | Step 12 (Initial state+12) | 0.158 | 0.166 | 0.174 | V |
| | | Vtdac13_8W | Step 13 (Initial state+13) | 0.152 | 0.160 | 0.168 | V |
| | | Vtdac14_8W | Step 14 (Initial state+14) | 0.146 | 0.154 | 0.162 | V |
| | | Vtdac15_8W | Step 15 (Initial state+15) | 0.140 | 0.148 | 0.156 | V |
| | | Vtdac16_8W | Step 16 (Initial state+16) | 0.132 | 0.140 | 0.148 | V |

Continued on next page.

LV8713T

Continued from preceding page.

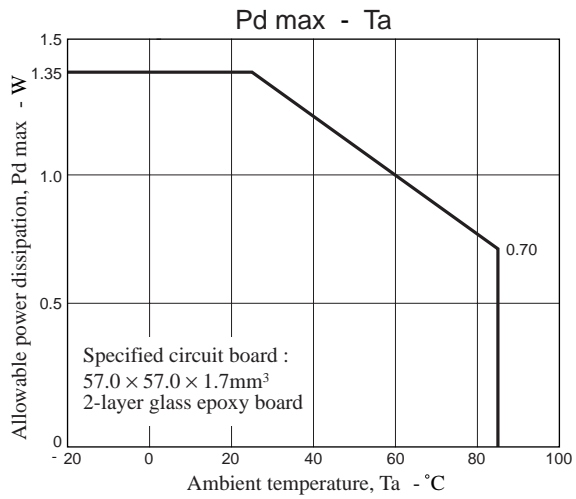
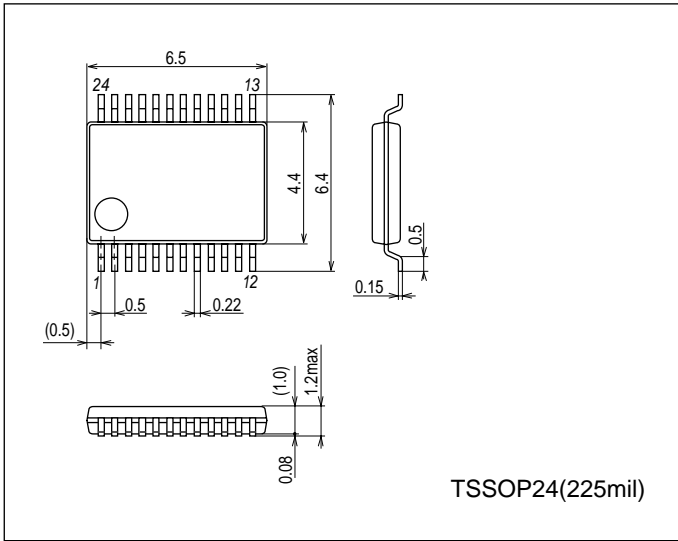
| Parameter | | Symbol | Conditions | Ratings | | | Unit |
|---|-------------------|---|--|---------|-------|-------|------|
| | | | | min | typ | max | |
| Current setting comparator threshold voltage (current step switching) | 8W1-2-phase drive | Vtdac17_8W | Step 17 (Initial state+17) | 0.126 | 0.134 | 0.142 | V |
| | | Vtdac18_8W | Step 18 (Initial state+18) | 0.118 | 0.126 | 0.134 | V |
| | | Vtdac19_8W | Step 19 (Initial state+19) | 0.112 | 0.120 | 0.128 | V |
| | | Vtdac20_8W | Step 20 (Initial state+20) | 0.102 | 0.110 | 0.118 | V |
| | | Vtdac21_8W | Step 21 (Initial state+21) | 0.094 | 0.102 | 0.110 | V |
| | | Vtdac22_8W | Step 22 (Initial state+22) | 0.086 | 0.094 | 0.102 | V |
| | | Vtdac23_8W | Step 23 (Initial state+23) | 0.078 | 0.086 | 0.094 | V |
| | | Vtdac24_8W | Step 24 (Initial state+24) | 0.068 | 0.076 | 0.084 | V |
| | | Vtdac25_8W | Step 25 (Initial state+25) | 0.060 | 0.068 | 0.076 | V |
| | | Vtdac26_8W | Step 26 (Initial state+26) | 0.050 | 0.058 | 0.066 | V |
| | | Vtdac27_8W | Step 27 (Initial state+27) | 0.040 | 0.048 | 0.056 | V |
| | | Vtdac28_8W | Step 28 (Initial state+28) | 0.032 | 0.040 | 0.048 | V |
| | | Vtdac29_8W | Step 29 (Initial state+29) | 0.022 | 0.030 | 0.038 | V |
| | | Vtdac30_8W | Step 30 (Initial state+30) | 0.012 | 0.020 | 0.028 | V |
| | | Vtdac31_8W | Step 31 (Initial state+31) | 0.002 | 0.010 | 0.018 | V |
| | 4W1-2-phase drive | Vtdac0_4W | Step 0 (When initialized : channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac2_4W | Step 2 (Initial state+1) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac4_4W | Step 4 (Initial state+2) | 0.187 | 0.196 | 0.205 | V |
| | | Vtdac6_4W | Step 6 (Initial state+3) | 0.183 | 0.192 | 0.201 | V |
| | | Vtdac8_4W | Step 8 (Initial state+4) | 0.175 | 0.184 | 0.193 | V |
| | | Vtdac10_4W | Step 10 (Initial state+5) | 0.167 | 0.176 | 0.185 | V |
| | | Vtdac12_4W | Step 12 (Initial state+6) | 0.158 | 0.166 | 0.174 | V |
| | | Vtdac14_4W | Step 14 (Initial state+7) | 0.146 | 0.154 | 0.162 | V |
| | | Vtdac16_4W | Step 16 (Initial state+8) | 0.132 | 0.140 | 0.148 | V |
| | | Vtdac18_4W | Step 18 (Initial state+9) | 0.118 | 0.126 | 0.134 | V |
| | | Vtdac20_4W | Step 20 (Initial state+10) | 0.102 | 0.110 | 0.118 | V |
| | | Vtdac22_4W | Step 22 (Initial state+11) | 0.086 | 0.094 | 0.102 | V |
| | | Vtdac24_4W | Step 24 (Initial state+12) | 0.068 | 0.076 | 0.084 | V |
| | | Vtdac26_4W | Step 26 (Initial state+13) | 0.050 | 0.058 | 0.066 | V |
| | | Vtdac28_4W | Step 28 (Initial state+14) | 0.032 | 0.040 | 0.048 | V |
| | Vtdac30_4W | Step 30 (Initial state+15) | 0.012 | 0.020 | 0.028 | V | |
| | 1-2 phase drive | Vtdac0_H | Step 0 (When initialized : channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
| | | Vtdac16_H | Step 4 (Initial state+1) | 0.132 | 0.140 | 0.148 | V |
| 2 phase drive | Vtdac16_F | Step 4' (When initialized : channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V | |

LV8713T

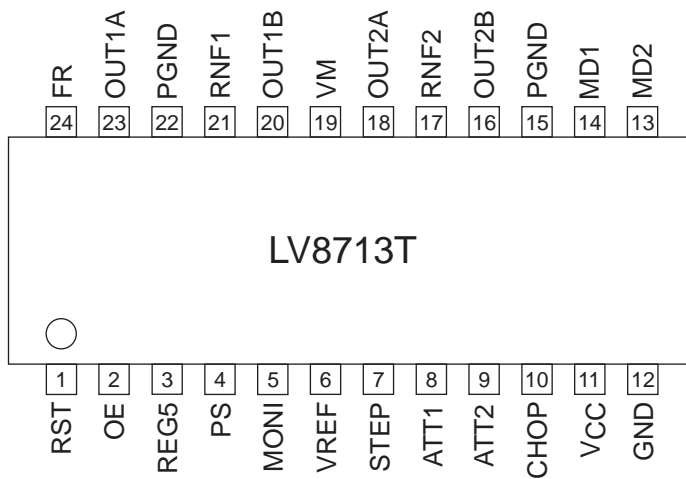
Package Dimensions

unit : mm (typ)

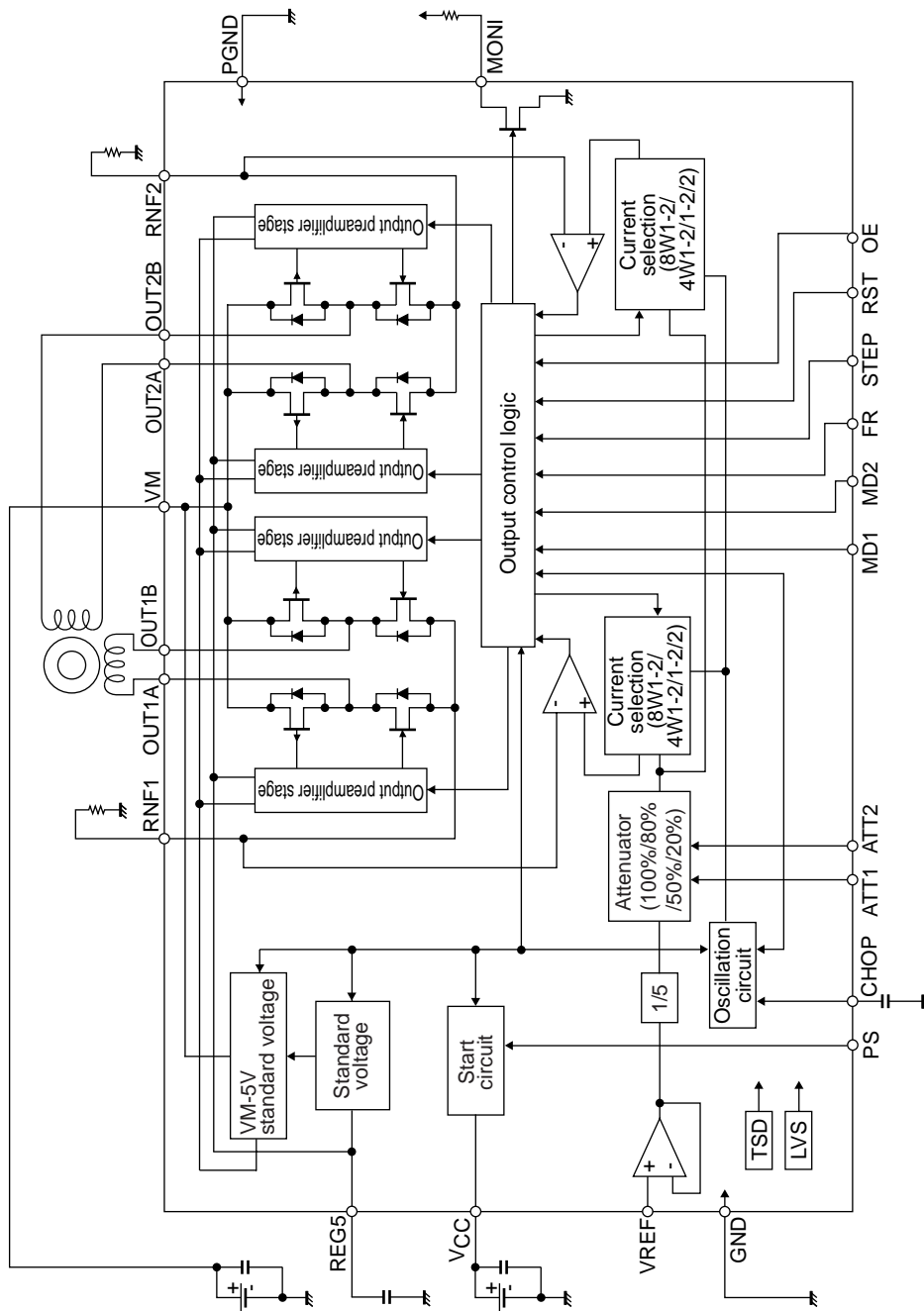
3260A



Pin Assignment



Block Diagram



LV8713T

Pin Functions

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|---|---|---|--------------------|
| 1 2 7 8 9 13 14 24 | RST OE STEP ATT1 ATT2 MD2 MD1 FR | Excitation reset signal input pin. Output enable signal input pin. STEP signal input pin. Motor holding current switching pin. Motor holding current switching pin. Excitation mode switching pin 2. Excitation mode switching pin 1. CW / CCW switching signal input pin. | |
| 4 | PS | Power save signal input pin. | |
| 16 17 18 20 21 23 | OUT2B RNF2 OUT2A OUT1B RNF1 OUT1A | Channel 2 OUTB output pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 OUTA output pin. Power | |
| 6 | VREF | Constant current control reference voltage input pin. | |

Continued on next page.

LV8713T

Continued from preceding page.

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
|---------|----------|--|--------------------|
| 3 | REG5 | Internal power supply capacitor connection pin. | |
| 5 | MONI | Position detection monitor pin. | |
| 10 | CHOP | Chopping frequency setting capacitor connection pin. | |

Description of operation

Stepping motor control

(1) Power save function

This IC is switched between standby and operating mode by setting the PS pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit do not operate in standby mode.

| PS | Mode | Internal regulator |
|-------------|----------------|--------------------|
| Low or Open | Standby mode | Standby |
| High | Operating mode | Operating |

(2) The order of turning on recommended power supply



The order of turning on each power supply recommends the following.

VCC power supply order → VM power supply order → PS pin = High

It becomes the above-mentioned opposite for power supply OFF.

However, the above-mentioned is a recommendation, the overcurrent is not caused by not having defended this, and IC is destroyed.

(3) STEP pin function

| Input | | Operating mode |
|-------|---|--------------------------|
| PS | STP | |
| Low | * | Standby mode |
| High |  | Excitation step proceeds |
| High |  | Excitation step is kept |

(4) Excitation mode setting function(initial position)

| MD1 | MD2 | Excitation mode | Initial position | |
|------|------|------------------------|------------------|-----------|
| | | | Channel 1 | Channel 2 |
| Low | Low | 2 phase excitation | 100% | -100% |
| High | Low | 1-2 phase excitation | 100% | 0% |
| Low | High | 4W1-2 phase excitation | 100% | 0% |
| High | High | 8W1-2 phase excitation | 100% | 0% |

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

(5) Position detection monitoring function

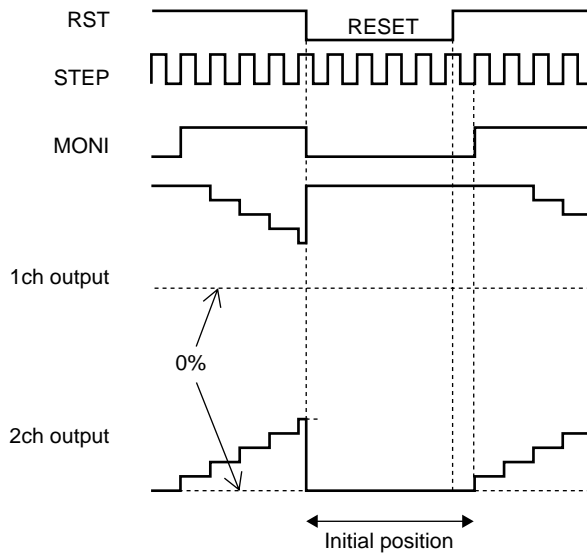
The MONI position detection monitoring pin is of an open drian type.

When the excitation position is in the initial position, the MONI output is placed in the ON state.

(Refer to "(12) Examples of current waveforms in each of the excitation modes.")

(6) Reset function

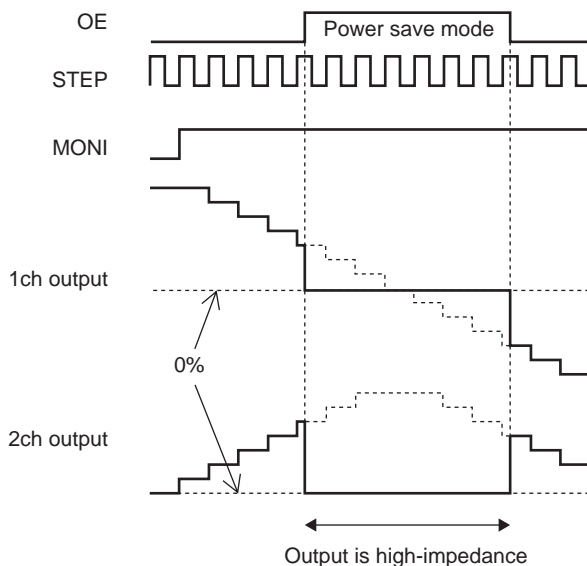
| RST | Operating mode |
|------|------------------|
| High | Normal operation |
| Low | Reset state |



When the RST pin is set to Low, the excitation position of the output is forcibly set to the initial position, and the MONI output is placed in the ON state. When RST is then set to High, the excitation position is advanced by the next STEP input.

(7) Output enable function

| OE | Operating mode |
|------|----------------|
| Low | Output ON |
| High | Output OFF |



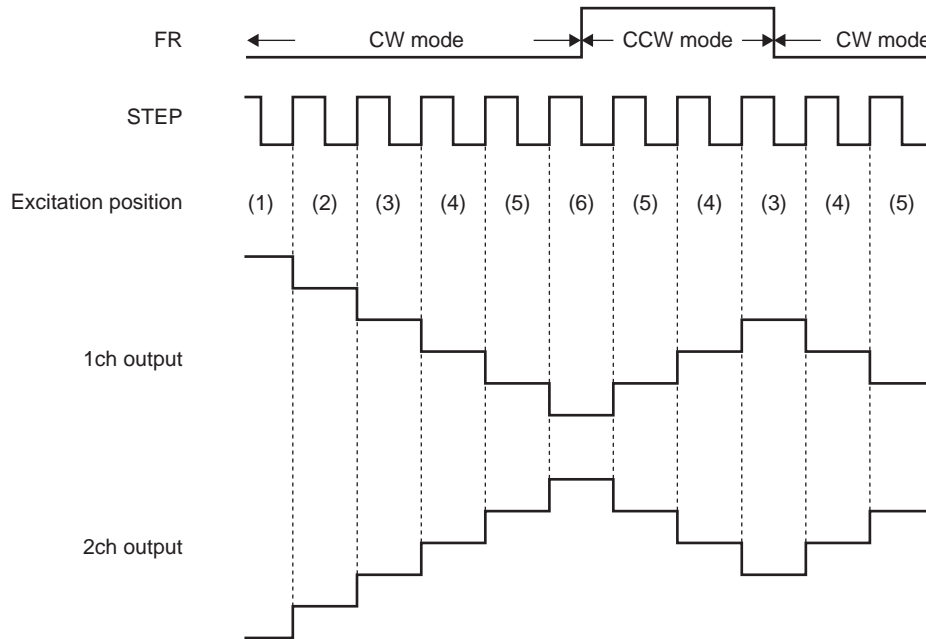
When the OE pin is set High, the output is forced OFF and goes to high impedance.

However, the internal logic circuits are operating, so the excitation position proceeds when the STEP signal is input.

Therefore, when OE is returned to Low, the output level conforms to the excitation position proceeded by the STEP input.

(8) Forward/reverse switching function

| | |
|------|-------------------------|
| FR | Operating mode |
| Low | Clockwise (CW) |
| High | Counter-clockwise (CCW) |



The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.
 In addition, CW and CCW mode are switched by setting the FR pin.
 In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
 In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(9) Setting constant-current control

The setting of STM driver's constant current control is decided the VREF voltage from the resistance connected between RNF and GND by the following expression.

$$I_{OUT} = (VREF/5)/RNF \text{ resistance}$$

* The above setting is the output current at 100% of each excitation mode.

The voltage input to the VREF pin can be switched to four-step settings depending on the statuses of the two inputs, ATT1 and ATT2. This is effective for reducing power consumption when motor holding current is supplied.

Attenuation function for VREF input voltage

| ATT1 | ATT2 | Current setting reference voltage attenuation ratio |
|------|------|---|
| Low | Low | 100% |
| High | Low | 80% |
| Low | High | 60% |
| High | High | 40% |

The formula used to calculate the output current when using the function for attenuating the VREF input voltage is given below.

$$I_{OUT} = (VREF/5) \times (\text{attenuation ratio})/RNF \text{ resistance}$$

Example : At VREF of 1.0V, a reference voltage setting of 100% [(ATT1, ATT2) = (L, L)] and an RNF resistance of 0.5Ω, the output current is set as shown below.

$$I_{OUT} = 1.0V/5 \times 100\%/0.5\Omega = 400mA$$

If, in this state, (ATT1, ATT2) is set to (H, H), IO_{UT} will be as follows :

$$I_{OUT} = 400mA \times 40\% = 160mA$$

In this way, the output current is attenuated when the motor holding current is supplied so that power can be conserved.

(10) Chopping frequency setting

For constant-current control, this IC performs chopping operations at the frequency determined by the capacitor (Cchop) connected between the CHOP pin and GND.

The chopping frequency is set as shown below by the capacitor (Cchop) connected between the CHOP pin and GND.

$$T_{chop} \doteq C \times V \times 2 / I \text{ (s)}$$

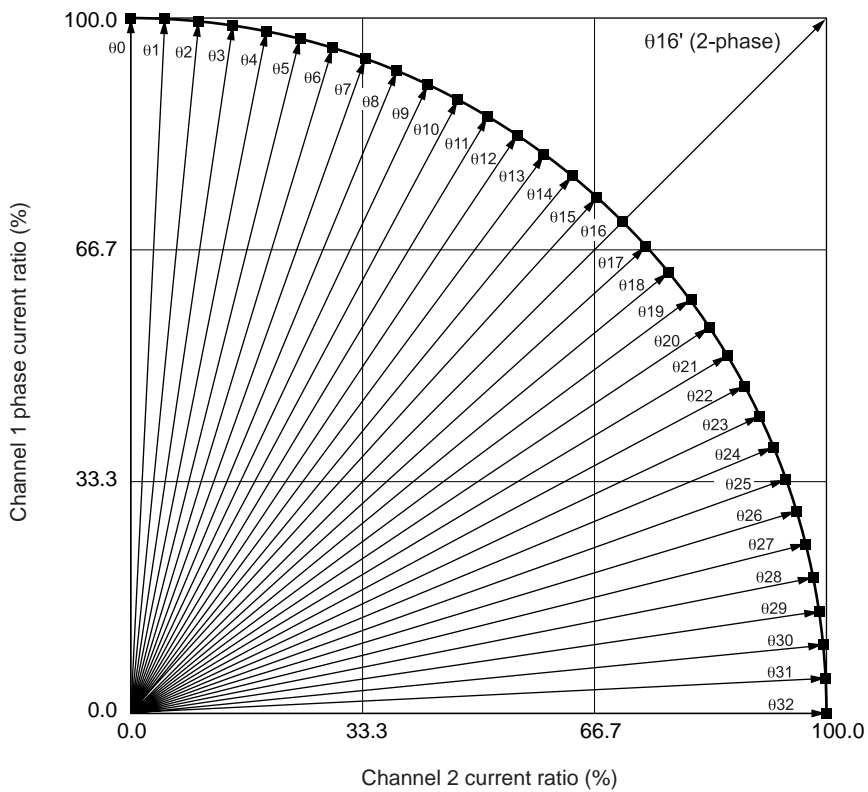
V : Width of suresshu voltage, typ 0.5V

I : Charge/discharge current, typ 10μA

For instance, when Cchop is 200pF, the chopping frequency will be as follows :

$$F_{chop} \doteq 1 / T_{chop} \text{ (Hz)}$$

(11) Output current vector locus (one step is normalized to 90 degrees)



LV8713T

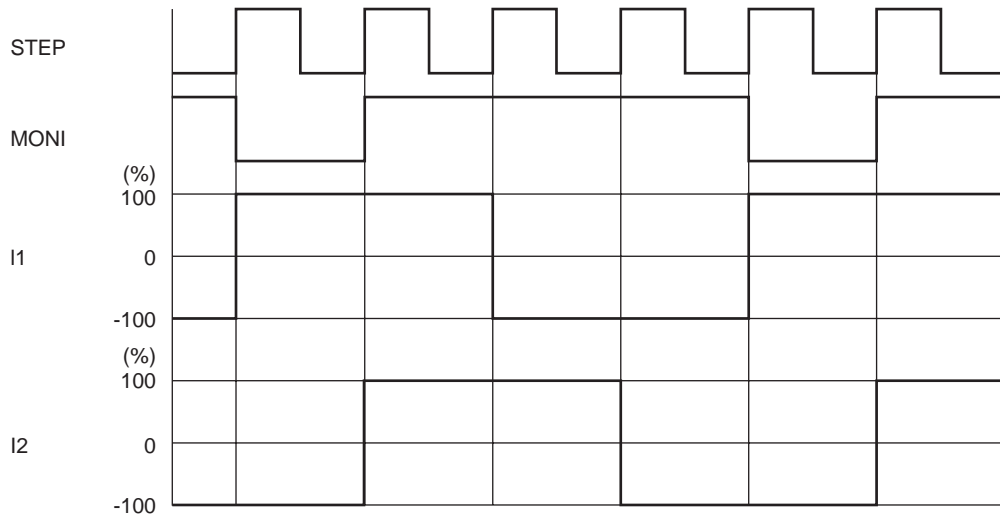
Setting current ration in each excitation mode

| STEP | 8W1-2 phase (%) | | 4W1-2 phase (%) | | 1-2 phase (%) | | 2-phase (%) | |
|------|-----------------|-----------|-----------------|-----------|---------------|-----------|-------------|-----------|
| | Channel 1 | Channel 2 | Channel 1 | Channel 2 | Channel 1 | Channel 2 | Channel 1 | Channel 2 |
| 00 | 100 | 0 | 100 | 0 | 100 | 0 | | |
| 01 | 100 | 5 | | | | | | |
| 02 | 100 | 10 | 100 | 10 | | | | |
| 03 | 99 | 15 | | | | | | |
| 04 | 98 | 20 | 98 | 20 | | | | |
| 05 | 97 | 24 | | | | | | |
| 06 | 96 | 29 | 96 | 29 | | | | |
| 07 | 94 | 34 | | | | | | |
| 08 | 92 | 38 | 92 | 38 | | | | |
| 09 | 90 | 43 | | | | | | |
| 010 | 88 | 47 | 88 | 47 | | | | |
| 011 | 86 | 51 | | | | | | |
| 012 | 83 | 55 | 83 | 55 | | | | |
| 013 | 80 | 60 | | | | | | |
| 014 | 77 | 63 | 77 | 63 | | | | |
| 015 | 74 | 67 | | | | | | |
| 016 | 70 | 70 | 70 | 70 | 70 | 70 | 100 | 100 |
| 017 | 67 | 74 | | | | | | |
| 018 | 63 | 77 | 63 | 77 | | | | |
| 019 | 60 | 80 | | | | | | |
| 020 | 55 | 83 | 55 | 83 | | | | |
| 021 | 51 | 86 | | | | | | |
| 022 | 47 | 88 | 47 | 88 | | | | |
| 023 | 43 | 90 | | | | | | |
| 024 | 38 | 92 | 38 | 92 | | | | |
| 025 | 34 | 94 | | | | | | |
| 026 | 29 | 96 | 29 | 96 | | | | |
| 027 | 24 | 97 | | | | | | |
| 028 | 20 | 98 | 20 | 98 | | | | |
| 029 | 15 | 99 | | | | | | |
| 030 | 10 | 100 | 10 | 100 | | | | |
| 031 | 5 | 100 | | | | | | |
| 032 | 0 | 100 | 0 | 100 | 0 | 100 | | |

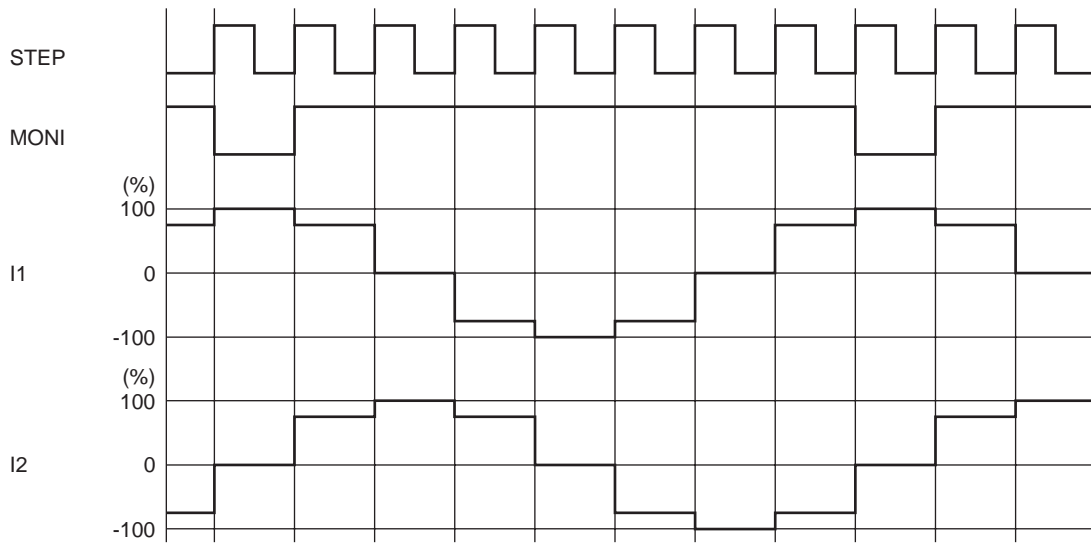
LV8713T

(12) Typical current waveform in each excitation mode

2-phase excitation (CW mode)

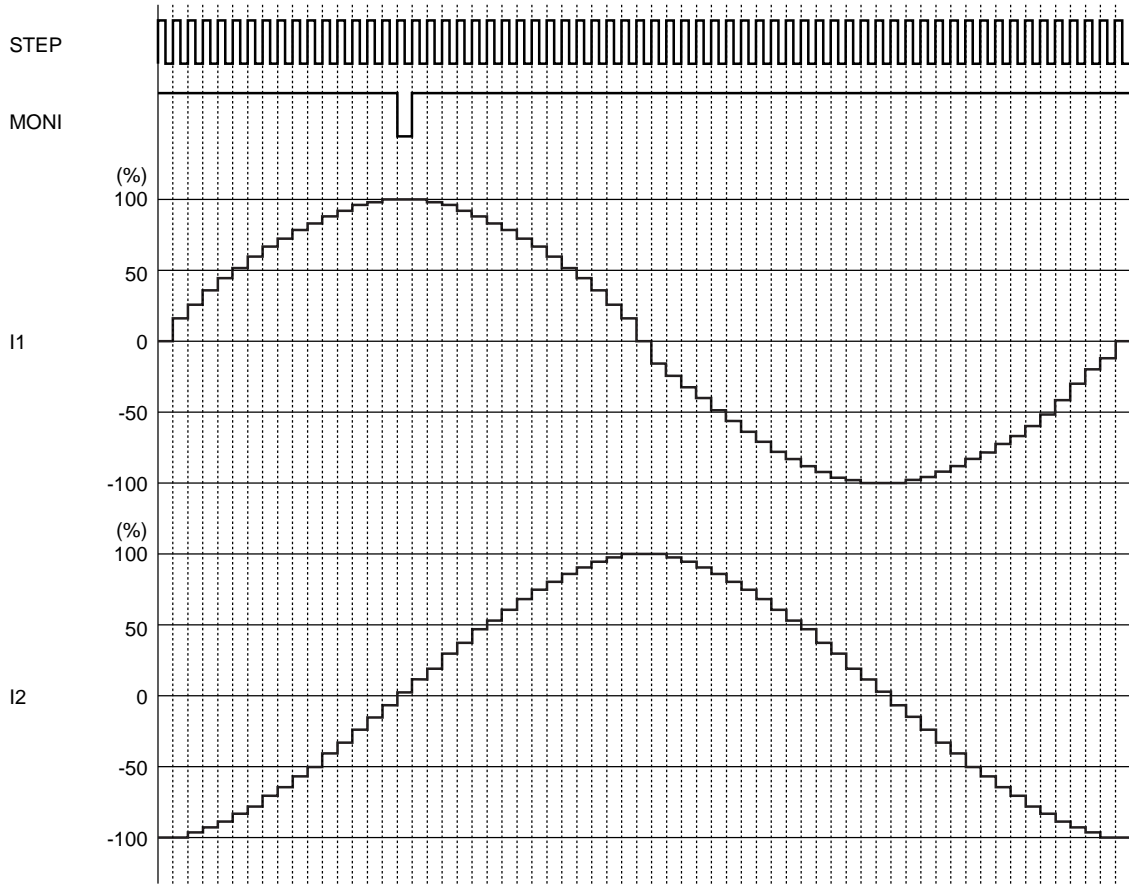


1-2 phase excitation (CW mode)

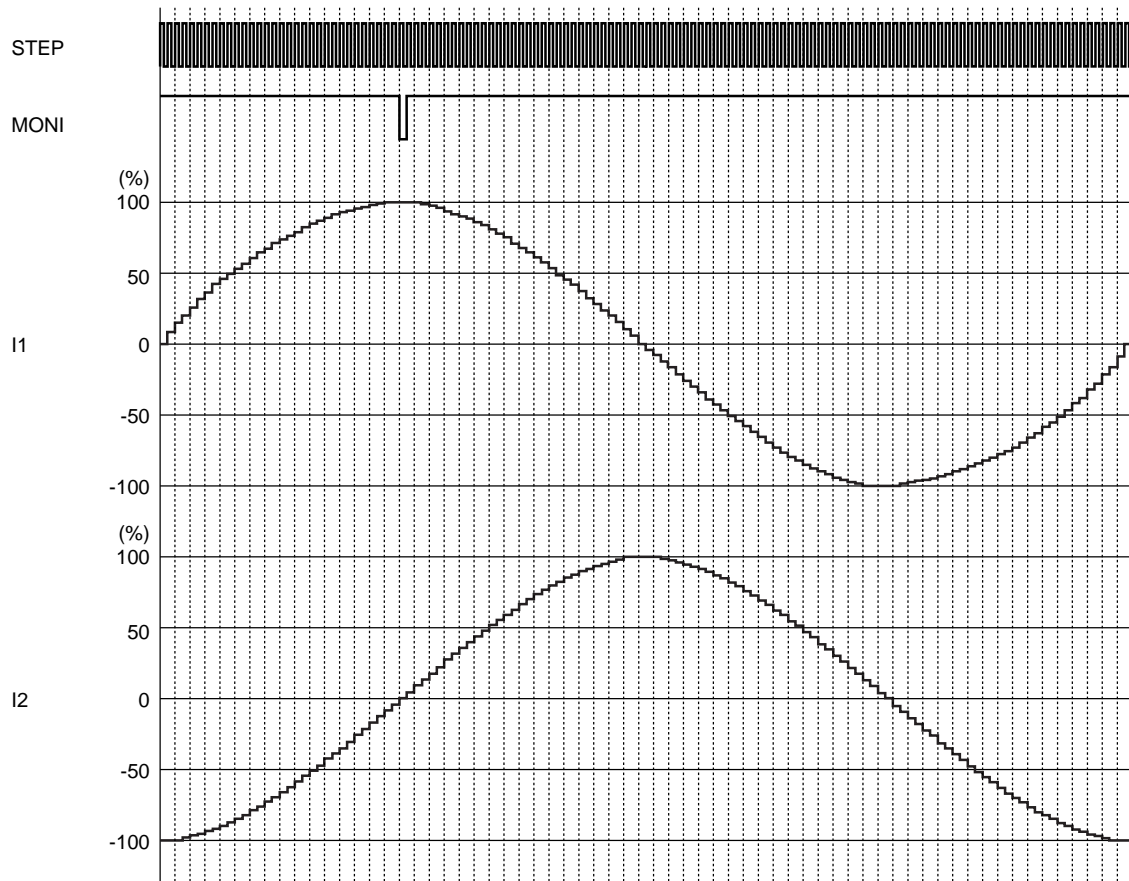


LV8713T

4W1-2 phase excitation (CW mode)

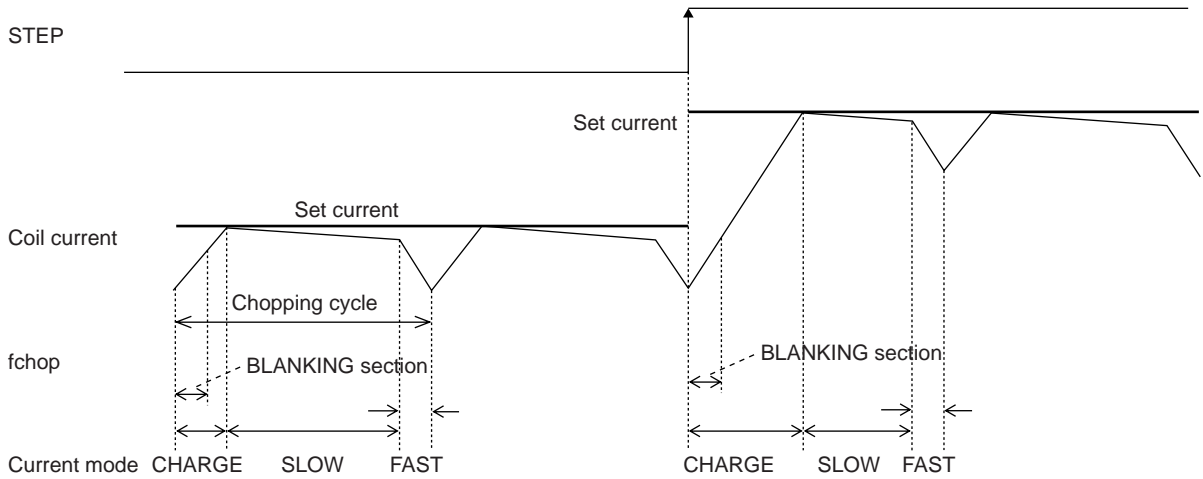


8W1-2 phase excitation (CW mode)

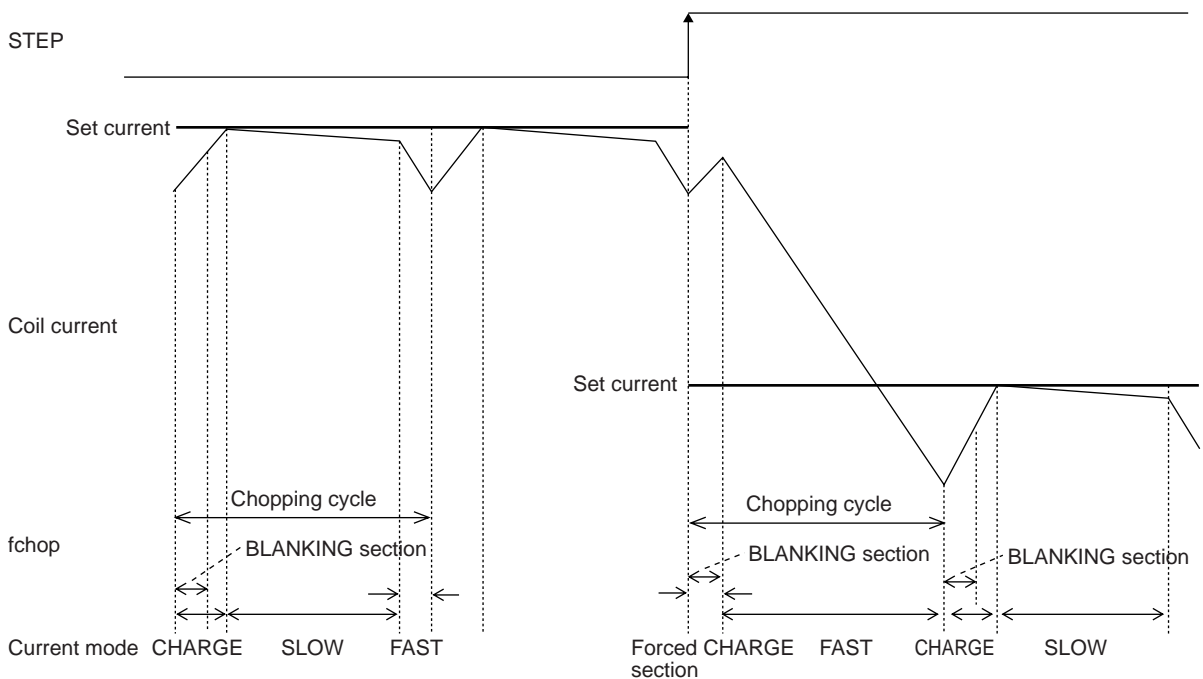


(13) Current control timing chart(Chopping operation)

(Sine wave increasing direction)



(Sine wave decreasing direction)



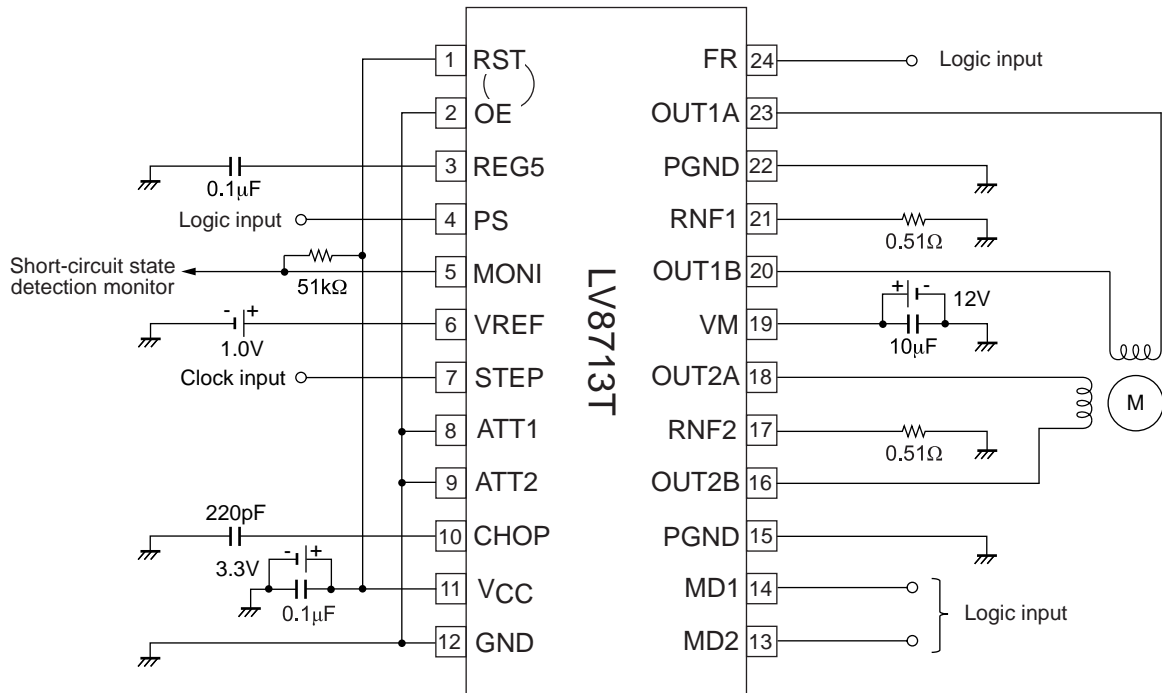
In each current mode, the operation sequence is as described below :

- At rise of chopping frequency, the CHARGE mode begins. (The Blanking section in which the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) exists for 1μs.)
- The coil current (ICOIL) and set current (IREF) are compared in this blanking time.
 - When (ICOIL < IREF) state exists ;
 - The CHARGE mode up to $ICOIL \geq IREF$, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for approximately 1μs.
 - When (ICOIL < IREF) state does not exist ;
 - The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

LV8713T

Application Circuit Example



The formulae for setting the constants in the examples of the application circuits above are as follows :

Constant current (100%) setting

When $V_{REF} = 1.0V$

$$I_{OUT} = V_{REF}/5/RNF \text{ resistance}$$

$$= 1.0V/5/0.51\Omega = 0.392A$$

Chopping frequency setting

$$F_{chop} = I_{chop}/(C_{chop} \times V_{tchop} \times 2)$$

$$= 10\mu A/(220pF \times 0.5V \times 2) = 45kHz$$

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.