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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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RD74LVC125B

Quad. Bus Buffer Gates with 3-state Outputs

REJ03D0498-0200

Rev.2.00

Dec. 10, 2004

Description

The RD74LVC125B has four bus buffer gates in a 14 pin package. The device requires the three state control input \overline{OE} to be taken high to put the output into the high impedance condition. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$
- All inputs $V_{IH} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V to } 5.5 \text{ V})$
- All outputs $V_{OUT} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V or output off state})$
- Typical V_{OL} ground bounce $< 0.8 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- Typical V_{OH} undershoot $> 2.0 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- High output current
 - $\pm 4 \text{ mA} (@V_{CC} = 1.65 \text{ V})$
 - $\pm 8 \text{ mA} (@V_{CC} = 2.3 \text{ V})$
 - $\pm 12 \text{ mA} (@V_{CC} = 2.7 \text{ V})$
 - $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 5.5 \text{ V})$
- Ordering Information

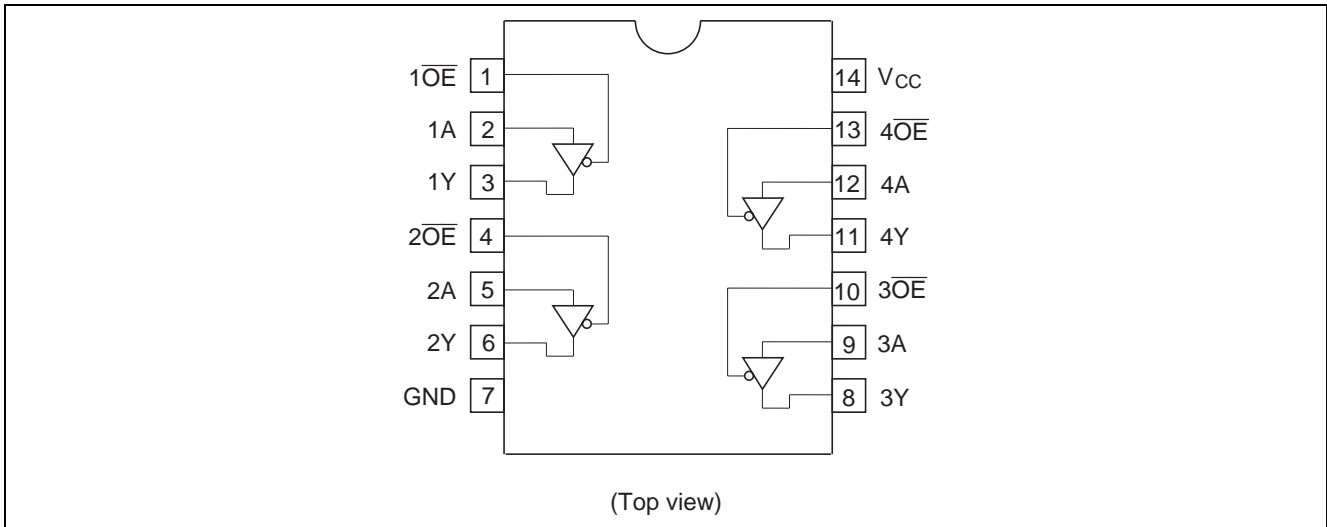
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC125BFPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
RD74LVC125BTELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

Function Table

Inputs		Outputs Y
\overline{OE}	A	
H	X	Z
L	L	L
L	H	H

- H: High level
- L: Low level
- X: Immaterial
- Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 7.0	V	
Input diode current	I_{IK}	-50	mA	$V_I = -0.5\text{ V}$
Input voltage	V_I	-0.5 to 7.0	V	
Output diode current	I_{OK}	-50	mA	$V_O = -0.5\text{ V}$
		50		$V_O = V_{CC} + 0.5\text{ V}$
Output voltage	V_O	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 7.0		Output "Z" or V_{CC} : OFF
Output current	I_O	± 50	mA	
V_{CC} , GND current / pin	I_{CC} or I_{GND}	± 100	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	
	V_O	0 to V_{CC} 0 to 5.5	V	Output "H" or "L" Output "Z" or V_{CC} : OFF
Operating temperature	T_a	-40 to 85	°C	
Output current	I_{OH}	-4	mA	$V_{CC} = 1.65\text{ V}$
		-8		$V_{CC} = 2.3\text{ V}$
		-12		$V_{CC} = 2.7\text{ V}$
		-24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	I_{OL}	4	mA	$V_{CC} = 1.65\text{ V}$
		8		$V_{CC} = 2.3\text{ V}$
		12		$V_{CC} = 2.7\text{ V}$
		24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time **1	t_r, t_f	20	ns/V	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$
		10		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V _{IH}	1.65 to 1.95	V _{CC} ×0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V _{CC} ×0.7	—		
	V _{IL}	1.65 to 1.95	—	V _{CC} ×0.35	V	
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V _{CC} ×0.3		
Output voltage	V _{OH}	1.65 to 5.5	V _{CC} -0.2	—	V	I _{OH} = -100 μA
		1.65	1.2	—		I _{OH} = -4 mA
		2.3	1.7	—		I _{OH} = -8 mA
		2.7	2.2	—		I _{OH} = -12 mA
		3.0	2.4	—		I _{OH} = -24 mA
		3.0	2.2	—		
		4.5	3.8	—		
	V _{OL}	1.65 to 5.5	—	0.2	V	I _{OL} = 100 μA
		1.65	—	0.45		I _{OL} = 4 mA
		2.3	—	0.7		I _{OL} = 8 mA
		2.7	—	0.4		I _{OL} = 12 mA
		3.0	—	0.55		I _{OL} = 24 mA
		4.5	—	0.55		
	Input current	I _{IN}	0 to 5.5	—	±5.0	μA
Output leak current	I _{OFF}	0	—	±5.0	μA	V _{IN} / V _{OUT} = 5.5 V
Off state output current	I _{OZ}	2.7 to 5.5	—	±5.0	μA	V _{IN} = V _{CC} or GND, V _{OUT} = 5.5 V or GND
Quiescent supply current	I _{CC}	2.7 to 3.6	—	±5.0	μA	V _{IN} = 3.6 V to 5.5 V
		2.7 to 5.5	—	5.0		V _{IN} = V _{CC} or GND
	ΔI _{CC}	2.7 to 3.6	—	500	μA	V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND

Switching Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t _{PLH}	1.8±0.15	1.0	—	12.3	ns	A	Y
	t _{PHL}	2.5±0.2	1.0	—	6.3			
		2.7	1.0	—	5.5			
		3.3±0.3	1.0	—	4.8			
		5.0±0.5	1.0	—	3.8			
Output enable time	t _{ZH}	1.8±0.15	1.0	—	14.3	ns	\overline{OE}	Y
	t _{ZL}	2.5±0.2	1.0	—	7.4			
		2.7	1.0	—	6.6			
		3.3±0.3	1.0	—	5.4			
		5.0±0.5	1.0	—	4.4			
Output disable time	t _{HZ}	1.8±0.15	1.0	—	11.1	ns	\overline{OE}	Y
	t _{LZ}	2.5±0.2	1.0	—	5.6			
		2.7	1.0	—	5.0			
		3.3±0.3	1.0	—	4.6			
		5.0±0.5	1.0	—	3.6			
Between output pins skew ^{*1}	t _{OSLH}	1.8±0.15	—	—	—	ns		
	t _{OSSL}	2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C _{IN}	3.3	—	4.0	—	pF		
Output capacitance	C _O	3.3	—	7.0	—	pF		

Note: 1. This parameter is characterized but not tested.

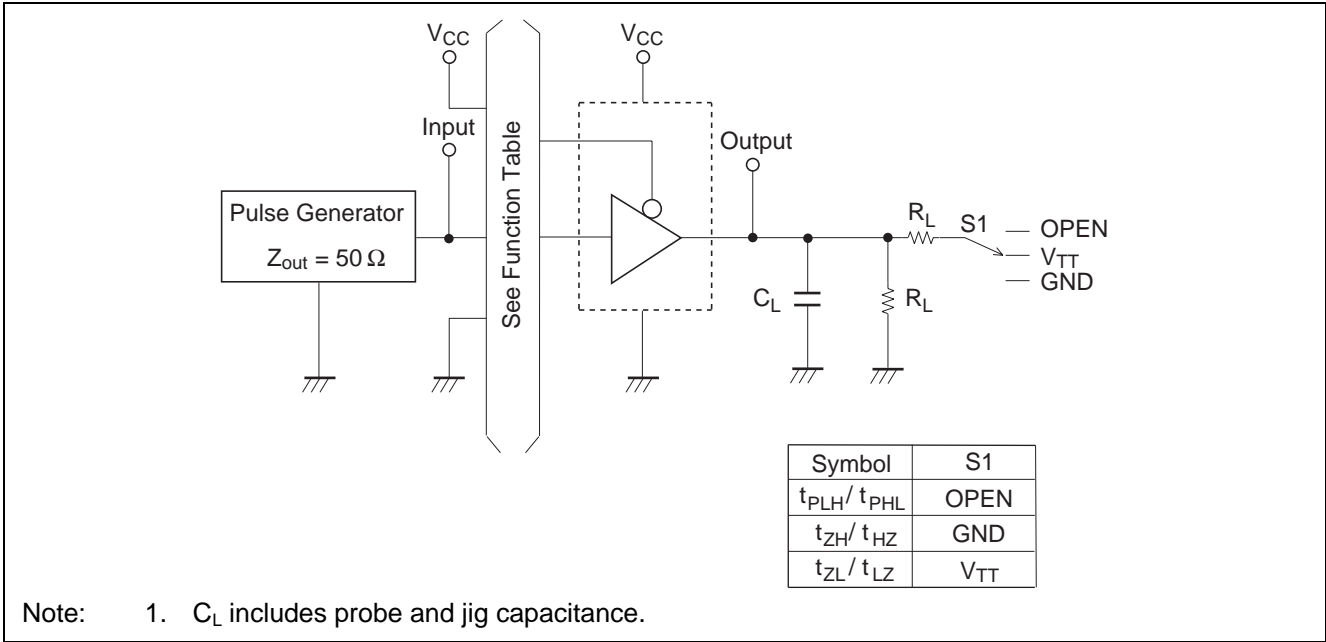
$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSSL} = |t_{PHLm} - t_{PHLn}|$$

Operating Characteristics

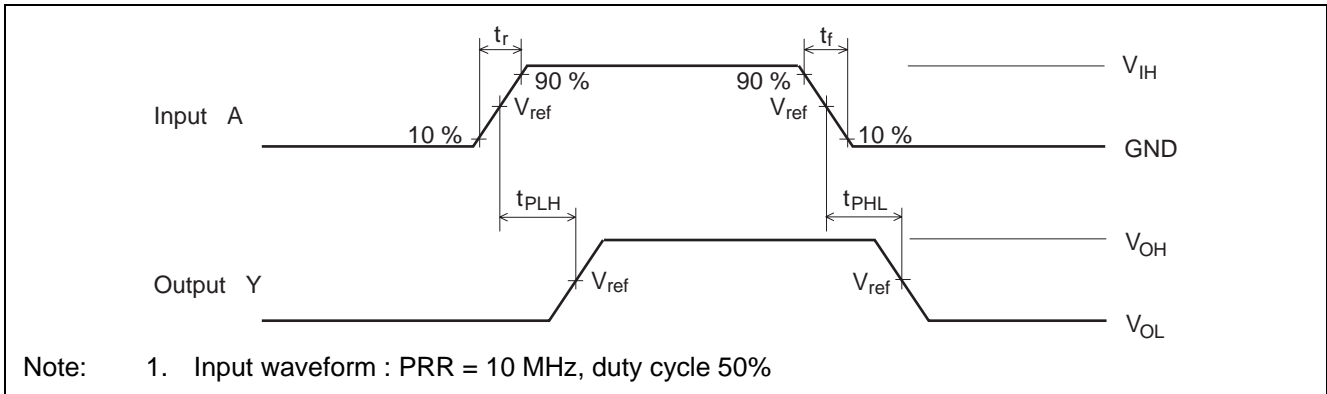
Ta = 25°C

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test conditions
Power dissipation capacitance	C _{PD}	1.8	—	21	—	pF	f = 10 MHz
		2.5	—	22	—		
		3.3	—	23	—		
		5.0	—	27	—		

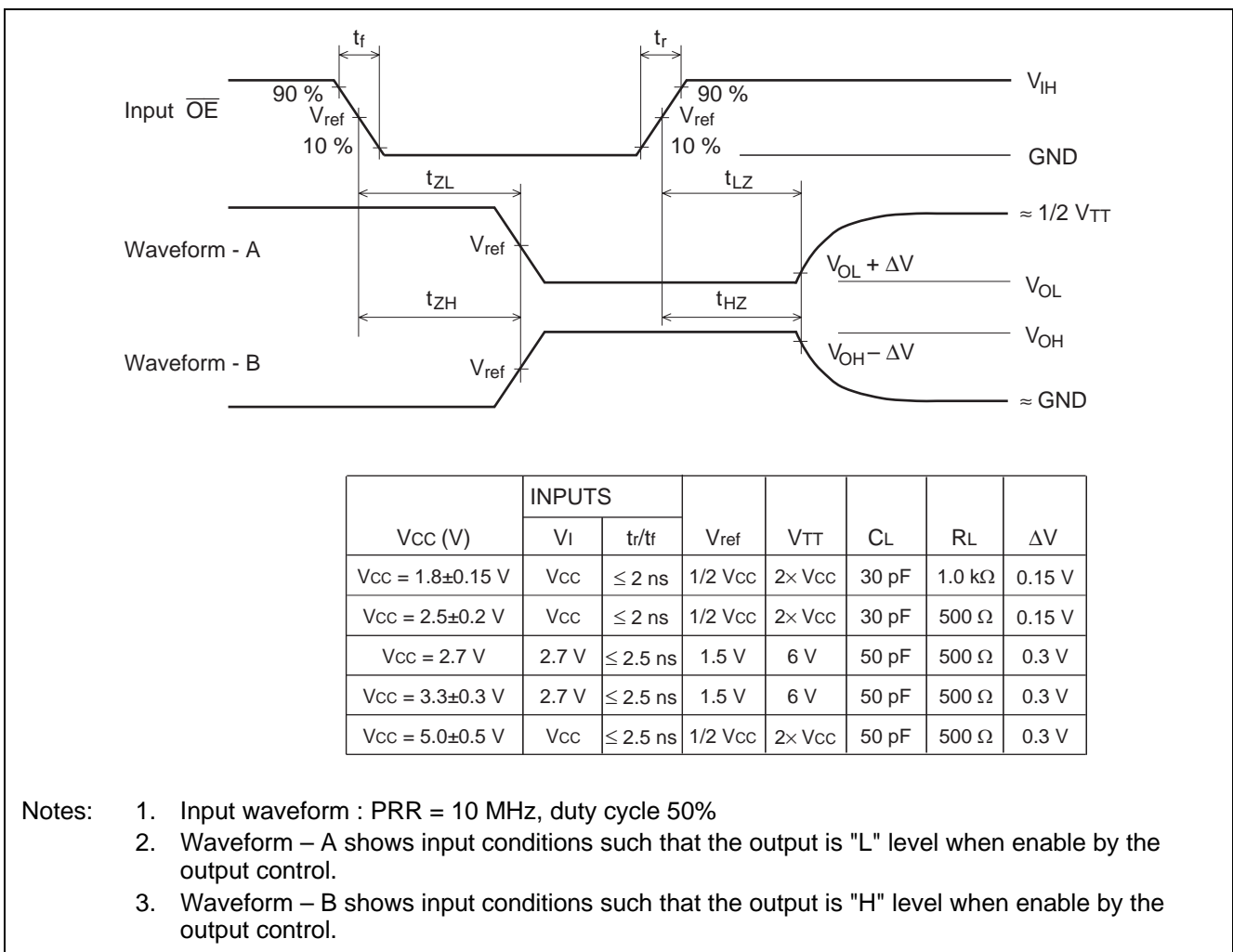
Test Circuit



Waveforms – 1

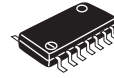
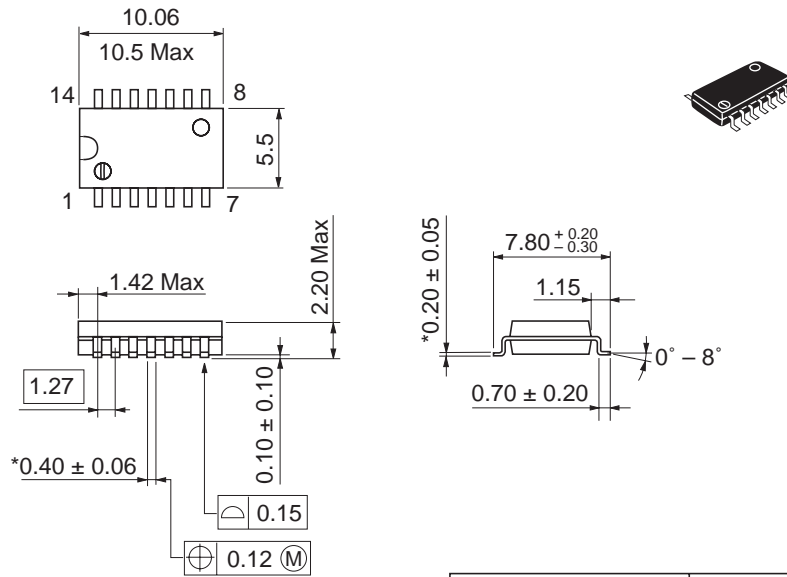


Waveforms – 2



Package Dimensions

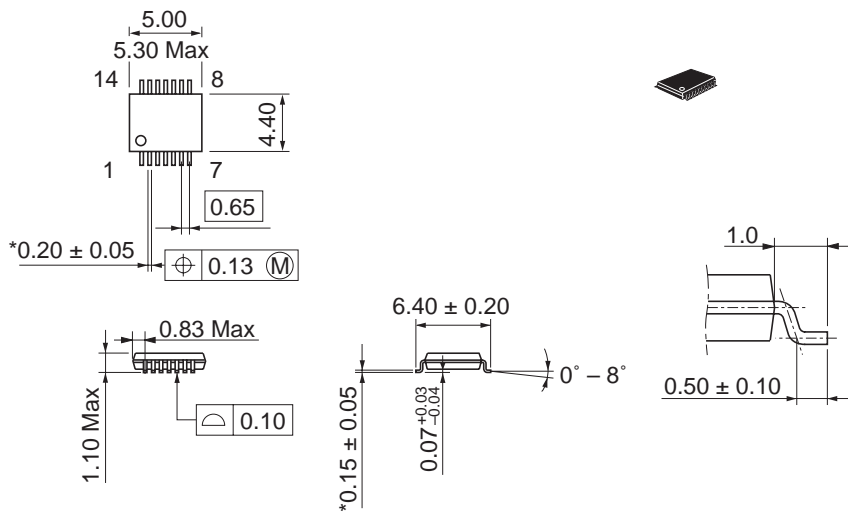
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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