



U74AUC1G126

CMOS IC

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

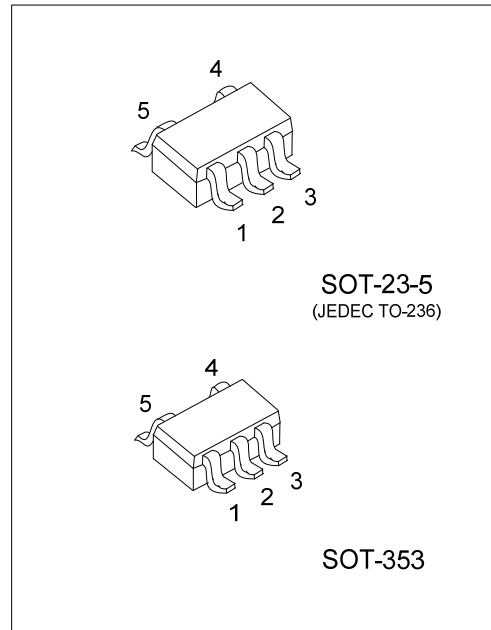
DESCRIPTION

The **U74AUC1G126** is single bus buffer gate with 3-state output. The output is disabled When the output enable (OE) is low. When OE is high, true data is passed from A input to the Y output.

This device has power-down protective circuit, preventing device destruction when it is powered down.

FEATURES

- * Operate from 0.8V to 2.7V
- * Low power dissipation: $I_{CC}=10\mu A$ (Max.)
- * $\pm 8mA$ Output Driver : $V_{CC}=1.8V$
- * I_{off} Supports partial-Power-Down Mode Operation

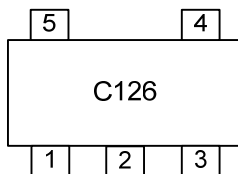


ORDERING INFORMATION

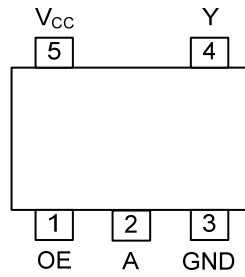
Ordering Number	Package	Packing
U74AUC1G126G-AE5-R	SOT-23-5	Tape Reel
U74AUC1G126G-AL5-R	SOT-353	Tape Reel

<p>U74AUC1G126G-AE5-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) AE5: SOT-23-5, AL5: SOT-353 (3) G: Halogen Free and Lead Free</p>
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MARKING



■ PIN CONFIGURATION

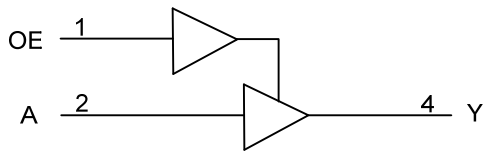


■ FUNCTION TABLE

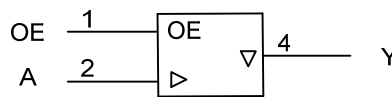
INPUT(OE)	INPUT(A)	OUTPUT(Y)
H	H	H
H	L	L
L	X	Z

Note: H: HIGH voltage level; L: LOW voltage level; X=don't care; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +3.6	V
Input Voltage	V_{IN}		-0.5 ~ +3.6	V
Output Voltage	V_{OUT}	Enable mode	-0.5 ~ $V_{CC} + 0.5$	V
		Disable mode	-0.5 ~ +3.6	V
		Power-down mode	-0.5 ~ +3.6	V
V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	$V_{OUT}=0 \sim V_{CC}$	±20	mA
Input Clamp Current	I_{IK}	$V_{IN}<0$	-50	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0$	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	0.8		2.7	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Operating Temperature	T_A		-40		85	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=0.8V \sim 1.6V$			20	ns/V
		$V_{CC}=1.65V \sim 1.95V$			10	ns/V
		$V_{CC}=2.3V \sim 2.7V$			3	ns/V

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC}=0.8V$	V_{CC}			V
		$V_{CC}=1.1V \sim 1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V \sim 2.7V$	1.7			V
Low-level Input Voltage	V_{IL}	$V_{CC}=0.8V$			0	V
		$V_{CC}=1.1V \sim 1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V \sim 2.7V$			0.7	V
High-Level Output Voltage	V_{OH}	$V_{CC}=0.8 \sim 2.7V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=0.8V, I_{OH}=-0.7mA$		0.55		V
		$V_{CC}=1.1V, I_{OH}=-3mA$	0.8			V
		$V_{CC}=1.4V, I_{OH}=-5mA$	1			V
		$V_{CC}=1.65V, I_{OH}=-8mA$	1.2			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=0.8 \sim 2.7V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=0.8V, I_{OL}=0.7mA$		0.25		V
		$V_{CC}=1.1V, I_{OL}=3mA$			0.3	V
		$V_{CC}=1.4V, I_{OL}=5mA$			0.4	V
		$V_{CC}=1.65V, I_{OL}=8mA$			0.45	V
Input Leakage Current	$I_{(LEAK)}$	$V_{CC}=2.7V, V_{IN}=V_{CC}$ or GND			±5	μA
		$V_{CC}=0V, V_{IN}$ or $V_{OUT}=2.7V$		±0.1	±10	μA
Power OFF Leakage Current	I_{off}	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=2.7V$		±0.1	±10	μA
3-state Output OFF-state Current	I_{OZ}	$V_{CC}=2.7V, V_{OUT}=V_{CC}$ or GND		±0.1	±10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=0.8V$ to $2.7V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$		0.1	10	μA
Input Capacitance	C_I	$V_{CC}=2.5V, V_{IN}=V_{CC}$ or GND		2.5		pF
output Capacitance	C_O	$V_{CC}=2.5V, V_{IN}=V_{CC}$ or GND		5.5		pF

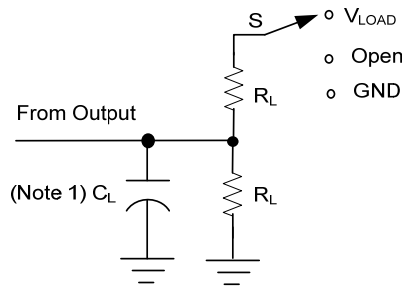
■ SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input A to output Y	t_{PLH} / t_{PHL}	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	$V_{CC} = 0.8\text{V}$		4.5	ns
			$V_{CC} = 1.2 \pm 0.1\text{V}$	0.8		ns
			$V_{CC} = 1.5 \pm 0.1\text{V}$	0.6		ns
			$V_{CC} = 1.8 \pm 0.15\text{V}$	0.6	1	ns
			$V_{CC} = 2.5 \pm 0.2\text{V}$	0.5		ns
		$C_L = 30\text{pF}$, $R_L = 1\text{k}\Omega$	$V_{CC} = 1.8 \pm 0.15\text{V}$	1	1.5	ns
		$C_L = 30\text{pF}$, $R_L = 500\Omega$	$V_{CC} = 2.5 \pm 0.2\text{V}$	0.9		ns
3-state output enable time from input $\overline{\text{OE}}$ to output Y	t_{PZH} / t_{PZL}	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	$V_{CC} = 0.8\text{V}$		4.9	ns
			$V_{CC} = 1.2 \pm 0.1\text{V}$	0.7		ns
			$V_{CC} = 1.5 \pm 0.1\text{V}$	0.7		ns
			$V_{CC} = 1.8 \pm 0.15\text{V}$	0.3	0.9	ns
			$V_{CC} = 2.5 \pm 0.2\text{V}$	0.3		ns
		$C_L = 30\text{pF}$, $R_L = 1\text{k}\Omega$	$V_{CC} = 1.8 \pm 0.15\text{V}$	1.1	1.6	ns
		$C_L = 30\text{pF}$, $R_L = 500\Omega$	$V_{CC} = 2.5 \pm 0.2\text{V}$	0.9		ns
3-state output disable time from input $\overline{\text{OE}}$ to output Y	t_{PLZ} / t_{PLH}	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	$V_{CC} = 0.8\text{V}$		4.9	ns
			$V_{CC} = 1.2 \pm 0.1\text{V}$	2.2		ns
			$V_{CC} = 1.5 \pm 0.1\text{V}$	1.8		ns
			$V_{CC} = 1.8 \pm 0.15\text{V}$	1.6	2.4	ns
			$V_{CC} = 2.5 \pm 0.2\text{V}$	1		ns
		$C_L = 30\text{pF}$, $R_L = 1\text{k}\Omega$	$V_{CC} = 1.8 \pm 0.15\text{V}$	1.3	2.6	ns
		$C_L = 30\text{pF}$, $R_L = 500\Omega$	$V_{CC} = 2.5 \pm 0.2\text{V}$	1		ns

■ OPERATING CHARACTERISTICS ($f = 10\text{MHz}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance (Outputs enabled)	C_{PD}	$V_{CC} = 0.8\text{V}$		14		pF
		$V_{CC} = 1.2\text{V}$		14		pF
		$V_{CC} = 1.5\text{V}$		14		pF
		$V_{CC} = 1.8\text{V}$		15		pF
		$V_{CC} = 2.5\text{V}$		16		pF
Power Dissipation Capacitance (Outputs Disabled)	C_{PD}	$V_{CC} = 0.8\text{V}$		1.5		pF
		$V_{CC} = 1.2\text{V}$		1.5		pF
		$V_{CC} = 1.5\text{V}$		1.5		pF
		$V_{CC} = 1.8\text{V}$		2		pF
		$V_{CC} = 2.5\text{V}$		2.5		pF

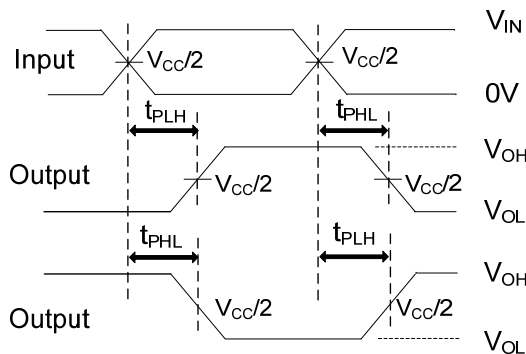
■ TEST CIRCUIT AND WAVEFORMS



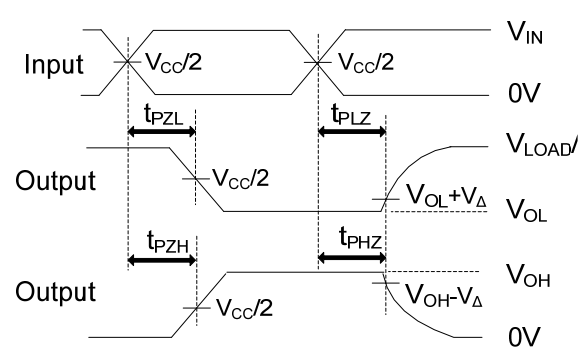
TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$

TEST CIRCUIT

V_{CC}	C_L	R_L	V_{Δ}
0.8V	15pF	2k Ω	0.1V
1.2V \pm 0.1V	15pF	2k Ω	0.1V
1.5V \pm 0.1V	15pF	2k Ω	0.1V
1.8V \pm 0.15V	15pF	2k Ω	0.15V
2.5V \pm 0.2V	15pF	2k Ω	0.15V
1.8V \pm 0.15V	30pF	1k Ω	0.15V
2.5V \pm 0.2V	30pF	500 Ω	0.15V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR \leq 10MHz, $Z_0 = 50\Omega$.

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