Data Sheet March 5, 2010 FN6786.0

DAE-1 for Manufacturers of High-Performance Class-D Audio Amplifiers

The D2Audio™ D2-814xx is a fully self-contained 4 channel digital amplifier controller System-On-Chip (SOC). The D2-814xx enables rapid system design for manufacturers of home theater receivers, multi-room distributed audio systems, and powered speakers.

The D2-814xx contains a high-performance digital switching controller to play any input source on any output channel.

A configurable audio signal processor provides equalization, volume control, tone control, and compression for each channel, also crossover and power limiting for powered speaker applications.

The D2-814xx includes 4-channels I^2S/Left-Justified inputs (16 to 24-bit, 32kHz to 192kHz), optional S/PDIF receiver (16 to 24-bit).

Boot options include: Self-boot from external serial ROM, asynchronous SCI slave boot, and serial slave boot from host uCon.

Please see the part number availability table for additional information on support for D2Audio™ SoundSuite™ firmware, as well as for SRS Labs™ and Dolby Labs™ algorithm support.

Features

- Powerful Digital Audio Management - Reference Design Dependant SRC, Routing, Mixing, Multiple Digital Audio I/O, Tone Control, Parametric EQ, Compression
- Reduced Audio System Cost for Manufacturers of Class-D Audio Amplifiers
- Audio Processing Features Enable Optimized Speaker Performance and Delivers Dramatically Improved Sound Quality
- Minimum Development Cost/Risk/ Time-to-Market
- Pure Digital Path
- Superior Dynamic Range
- >110dB SNR, <0.1% THD+N
- 20Hz - 20kHZ ±0.5dB Frequency Response

Complete Class-D Amplifier Controller SOC

- Digital Switching Controller
- Flexible Audio Input Sources
- Multiple Controller Synchronization
- Bridge and Non-Bridged Output Topologies
- Stand-Alone or Micro-Controller Boot Option
- 4 Channels
- Pb-Free (RoHS Compliant)

High-Performance Sound

- Unique Performance for Each Part Number
- Superior Dynamic Range
- >110 dB SNR, <0.1% THD+N
- 20Hz-20kHz ±0.5dB Frequency Response

Graceful Protection and Recovery

- Complete Short-Circuit, Overcurrent, and Overvoltage Fault Protection

Pure Digital Path

- Digital Audio Inputs which Support I^2S and Left-Justified Formats with Linear PCM (32kHz to 192kHz, 16 to 24-bit)
- Digital Audio Input which Supports S/PDIF Format with Linear PCM (32kHz to 192kHz, 16 to 24-bit)

Multiple Part Offerings

- D2-81412-LR: 144-pin LQFP
- D2-81433-LR: 128-pin LQFP
- D2-81434-LR: 128-pin LQFP Supporting Dolby Labs™ Technology
- D2-81435-LR: 128-pin LQFP Supporting SRS Labs™ Technology

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
D2-81412-LR	D2-81412-LR	144 Ld LQFP	Q144.20x20B
D2-81433-LR	D2-81433-LR	128 Ld LQFP	Q128.14x14
D2-81434-LR (Note 1)	D2-81434-LR	128 Ld LQFP	Q128.14x14
D2-81435-LR (Note 1)	D2-81435-LR	128 Ld LQFP	Q128.14x14

NOTES:

1. D2Audio is obliged to confirm that NDAs and/or Evaluation Sample Licenses are in place with all 3rd Party IP Owners and potential D2Audio customers before the sale of product or evaluation kits which contains either a D2-81434-LR or D2-81435-LR. Sale of the D2-81434-LR is only available to Dolby Laboratories licensees in good standing. Sale of the D2-81435-LR is only available to SRS Labs licensees in good standing.
2. Delivery of 3rd party Firmware is subject to prior confirmation with the 3rd party IP vendors that the OEM/ODM/Customer is currently in good standing and having the appropriate licenses in place for the respective technology. TruSurround HD and TruSurround HD4 are trademarks of SRS Labs, Inc. Dolby and the Double-D symbol are registered trademarks of Dolby Laboratories.
3. Please see separate Application Notes for D2Audio™ SoundSuite, Dolby Labs™, and SRS Labs™ firmware, register tables and signal flow information.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Table of Contents

D2-814xx Architecture

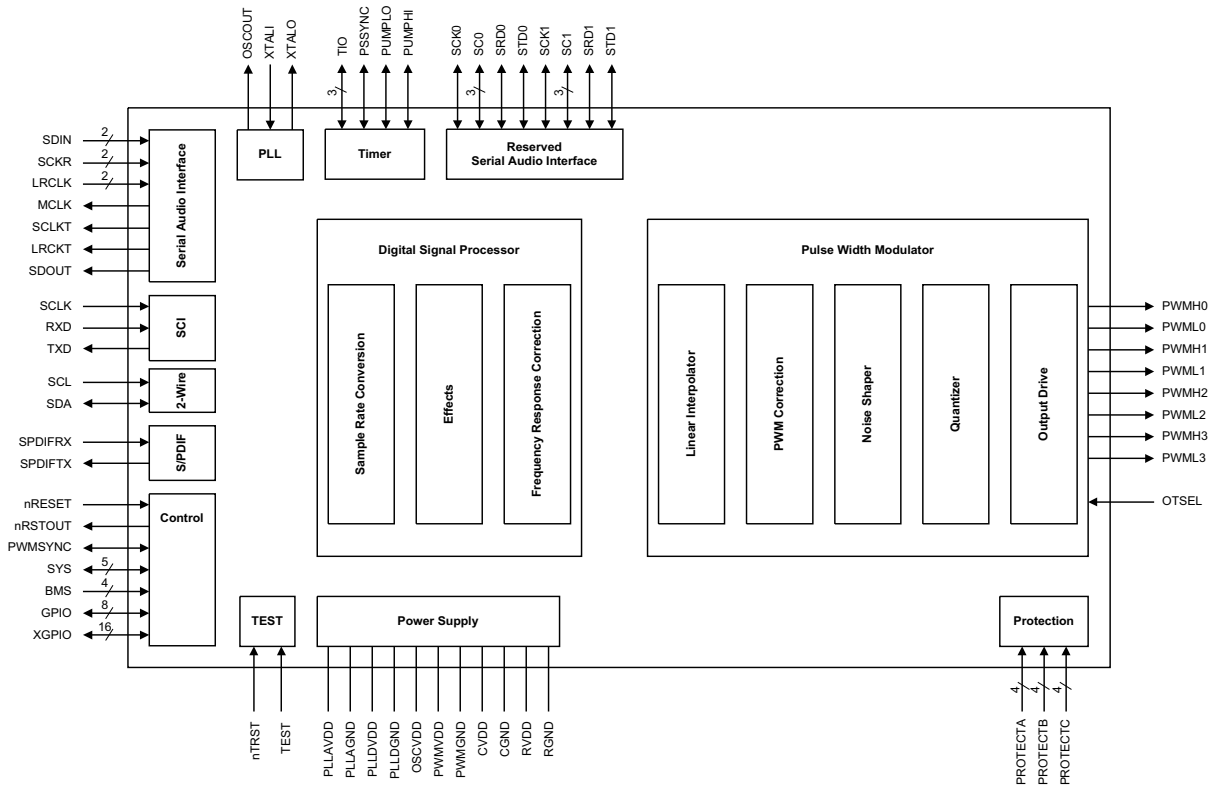

FIGURE 1. D2-814xx BLOCK DIAGRAM (144-PIN PACKAGE)

D2-814xx Signal Flow

The D2-814xx supports a wide variety of signal flows that are fully programmable and are reference design dependant. The D2-814xx IC is to only be used as part of a licensed Reference Design Platform (RDP) package from D2Audio Corporation. The designer should note that each Reference Design Platform (RDP) package has a set signal flow, which is handled by the specified firmware and associated performance level, which is determined primarily by the surrounding components used in the design. Please refer to the specific D2Audio Digital Amplifier Datasheet for the design-specific signal flows and corresponding register set.

Absolute Maximum Ratings

Supply Voltage RVDD, PWMVDD . . . . . -0.3V to 4.0V
Supply Voltage
CVDD, PLLAVDD, PLLDVDD, OSCVDD . . . . . -0.3V to 2.4V
Input Voltage, any input but XTALI. . . . . -0.3V to RVDD + 0.3V
Input Voltage XTALI . . . . . .-0.3V to OSCVDD + 0.3V
Input Current, any pin but supplies . . . . . ±10mA

Operating Conditions

Operating Temperature (T_{MAX}) (Note 5) . . . . . .-10°C to +85°C

Thermal Information

hermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
128 Ld LQFP		
Airflow @ 0	59.1	17.8
Airflow @ 1m/s	52.8	17.8
Airflow @ 2m/s	50.5	17.8
144 Ld LQFP		
Airflow @ 0	56.5	17.6
Airflow @ 1m/s	50.9	17.6
Airflow @ 2m/s	48.9	17.6

Junction Temperature (T_{JNC}) (Note 5) . . . . . +125°C
Storage Temperature Range (T_{STG}) (Note 5) . . . . . -55°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. For both 128 Ld LQFP and 144 Ld LQFP

Electrical Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PIN CHARACTERISTICS T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground					
High Level Input Drive Voltage (Note 6)	V_{IH}	2.0	-	-	V
Low Level Input Drive Voltage (Note 6)	V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (Note 7) Iout = -Pad Drive	V_{OH}	RVDD - 0.3	-	-	V
Low Level Output Drive Voltage (Note 7) Iout = +Pad drive	V_{OL}	-	-	0.3	V
High Level Input Drive Voltage (Note 8)	V_{IHX}	0.7	-	OSCVDD	V
Low Level Input Drive Voltage (Note 8)	V_{ILX}	-	-	0.3	V
High Level Output Drive Voltage OSCOUT pin	V_{OHO}	PLLDVDD - 0.3	-	-	V
Low Level Output Drive Voltage OSCOUT pin	V_{OLO}	-	-	0.3	V
Input Leakage Current	I_{IN}	-		±10	uA
Input Capacitance	C_{IN}	-	9	-	pF
Output Capacitance	C_{OUT}	-	9	-	pF
POWER REQUIREMENTS Typical supply currents measured at T_A = +25°C, PLL at 300MHz, OSC at 27MHz, core running at 150MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.					
Core Supply Pins	CVDD	1.7	1.8	1.9	V
		0.01	325		mA
Digital I/O Pad Ring Supply Pins	RVDD	3.0	3.3	3.6	V
		0.01	10		mA
PWM I/O Pad Ring Supply Pins	PWMVDD	3.0	3.3	3.6	V
		0.01	5		mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog Supply Pins (PLL)	PLLAVDD	1.7	1.8	1.9	V
		0.01	10		mA
	PLLDVDD	1.7	1.8	1.9	V
		0.01	2		mA
	OSCVDD	1.7	1.8	1.9	V
		0.01	4		mA

NOTES:

6. All input pins except XTALI
7. All digital output pins
8. For XTALI input overdrive operation only

Switching Characteristics - Serial Audio Port

T_A = +25°C, CVDD = PLLAVDD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_cSCLK	SCKRx frequency - SCKR0, SCKR1			12.5	MHz
t_wSCLK	SCKRx pulse width (high and low) - SCKR0, SCKR1	40			ns
t_sLRCLK	LRCKRx setup to SCLK rising - LRCKR0, LRCKR1	20			ns
t_hLRCLK	LRCKRx hold from SCLK rising - LRCKR0, LRCKR1	20			ns
t_sSDI	SDINx setup to SCLK rising - SDIN0, SDIN1	20			ns
t_hSDI	SDINx hold from SCLK rising - SDIN0, SDIN1	20			ns
t_dSDO	SDOUTx delay from SCLK falling			20	ns

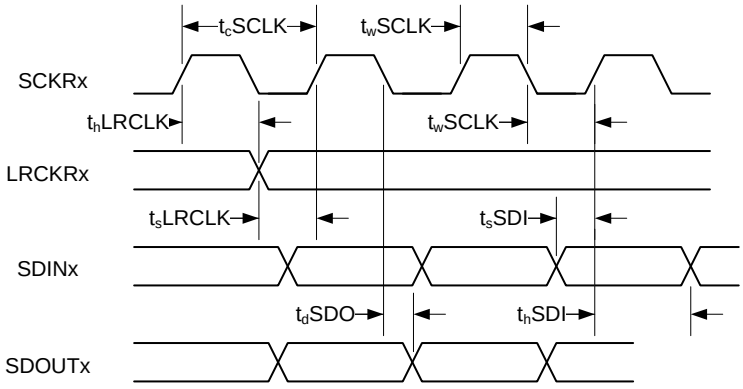

FIGURE 2. SERIAL AUDIO PORT TIMING

SERIAL AUDIO INTERFACE (SAI PORTS)

The D2-814xx IC contains one SAI port for each pair of channels. Each input can support an individually selectable sample rate from 32kHz to 192kHz. All digital audio inputs are 3.3V CMOS logic. The SAI port is designed to interface with standard digital audio components and to accept I^2S or Left-Justified data formats. Note: This port is entirely independent from the Reserved SAI port. The Reserved SAI port may or may not be used in a particular design.

For I^2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

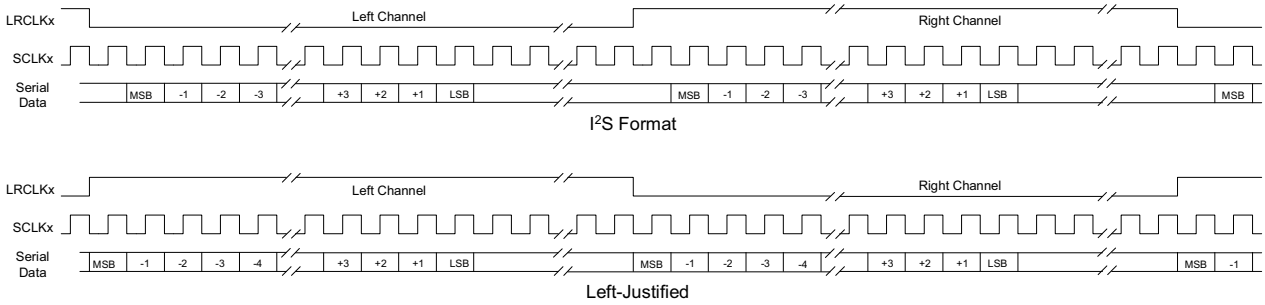

FIGURE 3. SAI PORT DATA FORMATS

Switching Characteristics - 2-Wire Interface

T_A = +25°C, CVDD = PLLAVD = PLLDVDD = OSCVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
fSCL	SCL frequency		100	kHz
t_{buf}	Bus free time between transmissions	4.7		µs
t_{wlow}SCLx	SCL clock low	4.7		µs
t_{whigh}SCLx	SCL clock high	4.0		µs
t_sSTA	Setup time for a (repeated) Start	4.7		µs
t_hSTA	Start condition Hold time	4.0		µs
t_hSDAx	SDA hold from SCL falling (see note)	0		µs
t_sSDAx	SDA setup time to SCL rising	250		ns
t_dSDAx	SDA output delay time from SCL falling		3.5	µs
t_r	Rise time of both SDA and SCL		1	µs
t_f	Fall time of both SDA and SCL		300	ns
t_sSTO	Setup time for a Stop condition	4.7		µs

NOTE:

9. Data must be held sufficient time to bridge the 300ns transition time of SCL

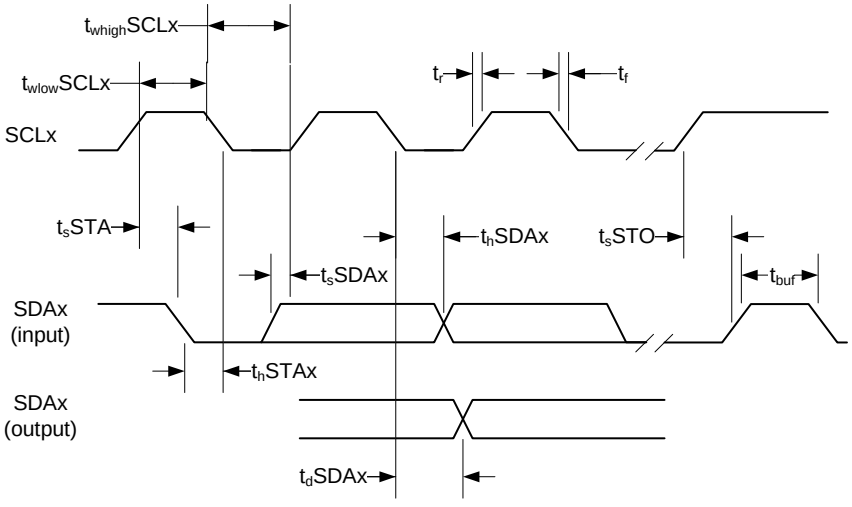

FIGURE 4. 2-WIRE INTERFACE TIMING

D2-814xx 128-Pin Package Pinout

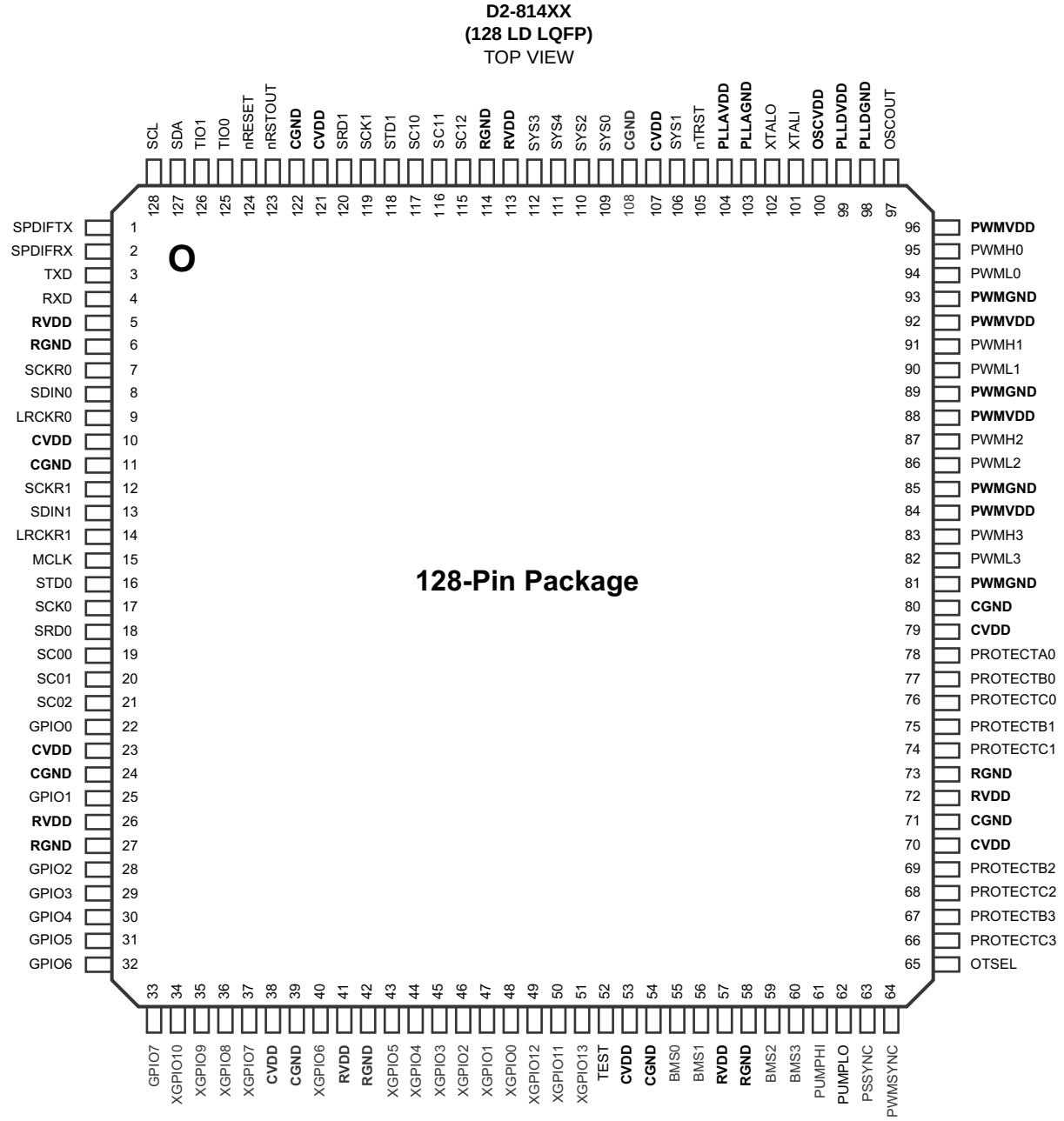

FIGURE 5. D2-814xx PINOUT, 128-PIN LQFP PACKAGE

Pin Definitions, 128-Pin LQFP Package

TABLE 1. PIN DEFINITIONS TABLE, 128-PIN LQFP PACKAGE

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
SERIAL AUDIO INTERFACE (SAI) PINS			
15	MCLK	Output	Master Clock
7	SCKR0	I/O	Serial Audio Bit Clock Receiver 0
9	LRCKR0	I/O	Serial Audio Left/Right Clock Receiver 0
8	SDIN0	Input	Serial Audio Data In 0
12	SCKR1	I/O	Serial Audio Bit Clock Receiver 1
14	LRCKR1	I/O	Serial Audio Left/Right Clock Receiver 1
13	SDIN1	Input	Serial Audio Data In 1
SPDIF PINS			
1	SPDIFTX	Output	S/PDIF data output
2	SPDIFRX	Input	S/PDIF data input
PWM PINS			
95	PWMH0	Output	Channel 0 PWM high side output
94	PWML0	Output	Channel 0 PWM low side output
91	PWMH1	Output	Channel 1 PWM high side output
90	PWML1	Output	Channel 1 PWM low side output
87	PWMH2	Output	Channel 2 PWM high side output
86	PWML2	Output	Channel 2 PWM low side output
83	PWMH3	Output	Channel 3 PWM high side output
82	PWML3	Output	Channel 3 PWM low side output
65	OTSEL	Input	Output topology select input
64	PWMSYNC	I/O	PWM Sync
2-WIRE SERIAL PINS			
128	SCL	I/O	Two wire serial clock
127	SDA	I/O	Two wire serial data
XGPIO PINS			
34, 35, 36, 37, 40, 43, 44, 45, 46, 47, 48	XGPIO[10:0]	I/O	General purpose I/O
50	XGPIO[11]	I/O	
49	XGPIO[12]	I/O	
51	XGPIO[13]	I/O	
GPIO PINS			
33, 32, 31, 30, 29, 28, 25, 22	GPIO[7:0]	I/O	General purpose I/O
RESET AND TEST PINS			
124	nRESET	Input	Reset - active low
123	nRSTOUT	Output	Reset output- active low output
105	nTRST	Input	Test reset - active low
52	TEST	Input	Hardware test pin
CRYSTAL OSCILLATOR AND PLL PINS			
97	OSCOUT	Output	Oscillator output to slave device
101	XTALI	Input	Crystal Oscillator input
102	XTALO	Output	Crystal Oscillator output

TABLE 1. PIN DEFINITIONS TABLE, 128-PIN LQFP PACKAGE (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
SYSTEM CONFIGURATION PINS			
109	SYS0	I/O	Reserved for factory test
106	SYS1	I/O	
110	SYS2	I/O	
112	SYS3	I/O	
111	SYS4	I/O	
SERIAL COMMUNICATIONS INTERFACE (SCI) PINS			
4	RXD	I/O	SCI receive data
3	TXD	I/O	SCI transmit data
RESERVED SERIAL AUDIO INTERFACE PINS			
16	STD0	I/O	Reserved Serial Audio Interface 0 Tx Data or GPIO
17	SCK0	I/O	Reserved Serial Audio Interface 0 Clock or GPIO
18	SRD0	I/O	Reserved Serial Audio Interface 0 Rx Data or GPIO
19	SC00	I/O	Reserved Serial Audio Interface 0 Control 0 or GPIO
20	SC01	I/O	Reserved Serial Audio Interface 0 Control 1 or GPIO
21	SC02	I/O	Reserved Serial Audio Interface 0 Control 2 or GPIO
118	STD1	I/O	Reserved Serial Audio Interface 1 Tx Data or GPIO
119	SCK1	I/O	Reserved Serial Audio Interface 1 Clock or GPIO
120	SRD1	I/O	Reserved Serial Audio Interface 1 Rx Data or GPIO
117	SC10	I/O	Reserved Serial Audio Interface 1 Control 0 or GPIO
116	SC11	I/O	Reserved Serial Audio Interface 1 Control 1 or GPIO
115	SC12	I/O	Reserved Serial Audio Interface 1 Control 2 or GPIO
BOOT MODE SELECT PINS			
55	BMS0	Input	Boot Mode Select 0
56	BMS1	Input	Boot Mode Select 1
59	BMS2	Input	Boot Mode Select 2
60	BMS3	Input	Boot Mode Select 3
TIMER (TIO) PINS			
126, 125	TIO[1:0]	I/O	Timer I/O ports
61	PUMPHI	I/O	Power supply pump control, high side or GPIO
62	PUMPLO	I/O	Power supply pump control, low side or GPIO
63	PSSYNC	I/O	Power supply synchronization or GPIO
PWM PROTECTION PINS			
78	PROTECTA0	I/O	PWM Temperature status input, or GPIO
67, 69, 75, 77	PROTECTB[3:0]	I/O	PWM Over Current Protection inputs, or GPIO
66, 68, 74, 76	PROTECTC[3:0]	I/O	PWM Shoot Through Current inputs or GPIO
POWER PINS			
104	PLLAVDD	Power	PLL Analog power
103	PLLAGND	Ground	PLL Analog ground
99	PLLDVDD	Power	PLL Digital power
98	PLLDGND	Ground	PLL Digital ground
100	OSCVDD	Power	Oscillator power
121, 107, 79, 70, 53, 38, 23, 10,	CVDD	Power	Core power - 8 pins

TABLE 1. PIN DEFINITIONS TABLE, 128-PIN LQFP PACKAGE (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
122, 108, 80, 71, 54, 39, 24, 11	CGND	Ground	Core ground - 8 pins
96, 92, 88, 84	PWMVDD	Power	PWM output pin power - 4 pins
93, 89, 85, 81	PWMGND	Ground	PWM output pin ground - 4 pins
113, 72, 57, 41, 26, 5	RVDD	Power	Digital pad ring power - 6 pins
114, 73, 58, 42, 27, 6	RGND	Ground	Digital pad ring ground - 6 pins

Pin Descriptions 128-Pin Package

Pins are 100% firmware and Reference Design Platform (RDP) Package dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

SERIAL AUDIO INTERFACE (SAI) PINS

MCLK Master Clock Output

Master Clock output for external ADC/DAC components with 8mA drive strength. Pin drives low on reset. MCLK is also used by test hardware to monitor various internal clocks.

SCKR0 SAI Receiver Bit Clock 1

SAI Receiver 0 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR0 SAI Receiver Left/Right Clock 0

SAI Receiver 0 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN0 SAI Receiver Serial Data Input 0

SAI Receiver 0 data input.

SCKR1 SAI Receiver Bit Clock 1

SAI Receiver 1 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR1 SAI Receiver Left/Right Clock 1

SAI Receiver 1 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN1 SAI Receiver Serial Data Input 1

SAI Receiver 1 data input.

S/PDIF PINS

SPDIFRX S/PDIF Data Input

This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to clean logic levels.

SPDIFTX S/PDIF Data Output

This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz.

PWM PINS

PWMxH PWM High Side Driver Outputs

PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

PWMxL PWM Low Side Driver Outputs

PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL Output Topology Select Input

Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

PWMSYNC PWM Synchronization

PWM synchronization port with 4mA drive. Used in multi-D2-814xx configurations to synchronize the PWM controllers. The master D2-814xx will drive synchronization data to the slave D2-814xx(s), thus the pin will be an output on the master D2-814xx and an input on the slave D2-814xx(s). Pin floats on reset.

2-WIRE SERIAL PINS

SCL Serial Clock

Two-Wire Serial clock port, open drain driver with 4mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA Serial Data

Two-Wire Serial data port, open drain driver with 4mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

XGPIO PINS

XGPIO[10:0] General Purpose I/O

Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[11] General Purpose I/O

Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[12] General Purpose I/O

Bidirectional GPIO port with 4mA driver. Resets to input port.

XGPIO[13] General Purpose I/O

Bidirectional GPIO port with 4mA driver. Resets to input port.

RESET AND TEST PINS

nRESET System Reset Input

Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nRSTOUT System Reset Output

Active low reset output with 4mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST Test Mode Input

Hardware test mode control. For D2Audio usage only. Must be tied low.

nTRST Test Reset Input

Active low test port reset. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

CRYSTAL OSCILLATOR AND PLL PINS

OSCOUT Oscillator Output

Analog oscillator output to slave D2-814xx devices. On reset, OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin. May be turned off by program control.

XTALI Crystal Oscillator Input

Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-814xx systems, the OSCOUT from the master D2-814xx would drive the XTALI pin.

XTALO Crystal Oscillator Output

Crystal oscillator analog output port. When using an external clock source, this pin must be open.

GPIO PINS

GPIO[7:0] General Purpose I/O

Bidirectional GPIO ports with 4mA driver. Resets to input ports.

SYSTEM CONFIGURATION PINS

SYS0 System Configuration Data 0

Reserved for factory test. Tie low with 10kΩ resistor.

SYS1 System Configuration Data 1

Reserved for factory test. Tie high with 10kΩ resistor.

SYS2 System Configuration Data 2

Reserved for factory test. Tie high with 10kΩ resistor.

SYS3 System Configuration Data 3

Reserved for factory test. Tie high with 10kΩ resistor.

SYS4 System Configuration Data 4

Reserved for factory test. Tie high with 10kΩ resistor.

SERIAL COMMUNICATIONS INTERFACE (SCI) PINS

RXD Receive Data

Serial communications receiver data with 4mA drive. Resets to input port. May be configured to GPIO.

TXD Transmit Data

Serial communications transmitter data with 4mA drive. Resets to input port. May be configured to GPIO.

OPTIONAL/RESERVED FUNCTION PINS

SCK0 Reserved Serial Audio Interface 0 Serial Clock

Serial Audio Interface 0 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC00-SC02 Reserved Serial Audio Interface 0 Serial Control

0 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD0 Reserved Serial Audio Interface 0 Serial Transmit Data

Serial Audio Interface 0 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD0 Reserved Serial Audio Interface 0 Serial Receive Data

Serial Audio Interface 0 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

SCK1 Reserved Serial Audio Interface 1 Serial Clock

Serial Audio Interface 1 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC10-SC12 Reserved Serial Audio Interface 1 Serial Control

Serial Audio Interface 1 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD1 Reserved Serial Audio Interface 1 Serial Transmit Data

Serial Audio Interface 1 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD1 Reserved Serial Audio Interface 1 Serial Receive Data

Serial Audio Interface 1 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

BOOT MODE SELECT PINS

BMS[3:0] Boot Mode Select Inputs

External boot mode select inputs. On nRESET deassertion, these pins provide the boot mode selection.

TIMER (TIO) PINS

TIO[1:0] Timer

Timer I/O ports with 4mA driver. May be configured as GPIO.

PUMPHI Power Supply Pump High

High side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PUMPLO Power Supply Pump Low

Low side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PSSYNC Power Supply Synchronization

Switching power supply synchronization signal with 16mA driver. May be configured as GPIO. Resets to

input port.

PWM PROTECTION PINS

PROTECTA0 PWM Temperature Protection Input

PWM temperature protection input with hysteresis. May be configured as GPIO. In this instance, the GPIO pin has a 4mA driver.

PROTECTB[3:0] PWM Overcurrent Protection Inputs

PWM overcurrent protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMOCP input is associated with the corresponding PWM driver channel.

PROTECTC[3:0] PWM Shoot-Through Current Protection

PWM shoot-through-current protection inputs with hysteresis. In this instance, the GPIO pins each have a 4mA driver. May be configured as GPIO. Each PWMSTC input is associated with the corresponding PWM driver channel.

POWER PINS

PLLAVDD/PLLAGND PLL Analog power and ground

PLL analog supply/return. This 1.8V supply is used for the jitter critical sections of the PLL.

PLLDVDD/PLLDGND PLL Digital power and ground

PLL digital supply/return. This 1.8V supply is used for the “dirty” sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD Oscillator power

Oscillator supply. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND Core power and ground

Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 8 core supply pad pairs internally connected around the pad ring.

PWMVDD/PWMGND PWM driver power and ground

PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

RVDD/RGND Pad Ring power and ground

Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 6 ring supply pairs internally connected around the pad ring.

D2-814xx 144-Pin Package Pinout

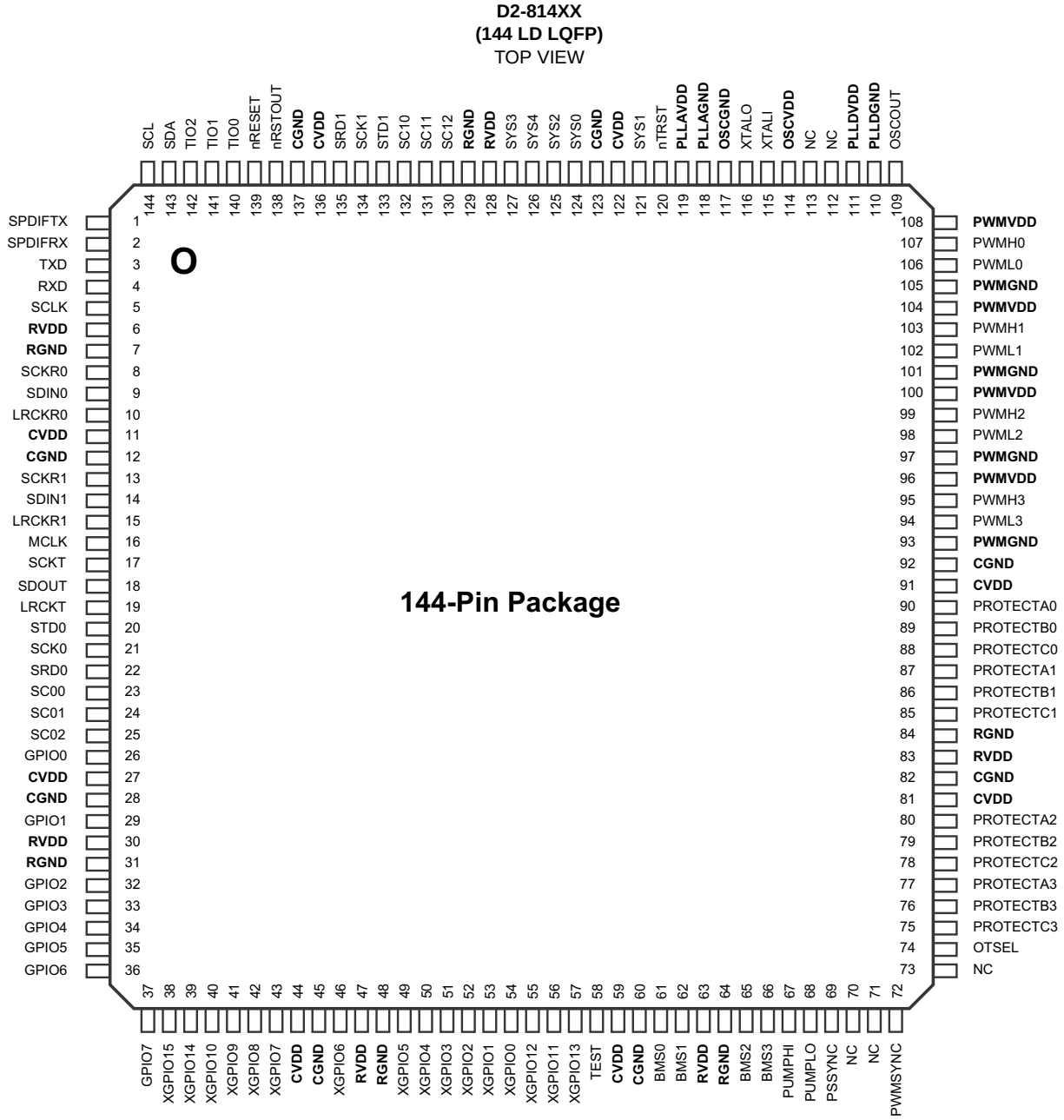

FIGURE 6. D2-814xx PINOUT, 144-PIN LQFP PACKAGE

Pin Definitions 144-Pin LQFP Package

TABLE 2. PIN DEFINITIONS, 144-PIN LQFP PACKAGE

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
SERIAL AUDIO INTERFACE (SAI) PINS			
16	MCLK	Output	Master clock output
8	SCKR0	I/O	Serial Audio Input 0 clock receiver
10	LRCKR0	I/O	Serial Audio Input 0 left/right clock receiver
9	SDIN0	Input	Serial Audio Input 0 data
13	SCKR1	I/O	Serial Audio Input Clock 1 receiver
15	LRCKR1	I/O	Serial Audio Input 1 left/right clock receiver
14	SDIN1	Input	Serial Audio Input 1 data
17	SCKT	I/O	Serial Audio Output clock transmit
19	LRCKT	I/O	Serial Audio Output left/right clock transmit
18	SDOUT	Output	Serial Audio Output
S/PDIF			
1	SPDIFTX	Output	S/PDIF data out
2	SPDIFRX	Input	S/PDIF data in
PWM PINS			
107	PWMH0	Output	Channel 0 PWM high side output
106	PWML0	Output	Channel 0 PWM low side output
103	PWMH1	Output	Channel 1 PWM high side output
102	PWML1	Output	Channel 1 PWM low side output
99	PWMH2	Output	Channel 2 PWM high side output
98	PWML2	Output	Channel 2 PWM low side output
95	PWMH3	Output	Channel 3 PWM high side output
94	PWML3	Output	Channel 3 PWM low side output
74	OTSEL	Input	Output topology select input
72	PWMSYNC	I/O	PWM sync
2-WIRE SERIAL PINS			
144	SCL	I/O	Two wire serial clock
143	SDA	I/O	Two wire serial data
XGPIO PINS			
43, 46, 49, 50, 51, 52, 53, 54	XGPIO[7:0]	I/O	General purpose I/O
38, 39, 57, 55, 56, 40, 41, 42	XGPIO[15:8]	I/O	
RESET AND TEST PINS			
139	nRESET	Input	Reset - active low
138	nRSTOUT	Output	Reset output- active low output
120	nTRST	Input	Test reset - active low
58	TEST	Input	Hardware test pin
CRYSTAL OSCILLATOR AND PLL PINS			
109	OSCOUT	Output	Oscillator output to slave device

TABLE 2. PIN DEFINITIONS, 144-PIN LQFP PACKAGE (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
115	XTALI	Input	Crystal Oscillator input
116	XTALO	Output	Crystal Oscillator output
GPIO PINS			
37, 36, 35, 34, 33, 32, 29, 26	GPIO[7:0]	I/O	General Purpose I/O
SYSTEM CONFIGURATION PINS			
124	SYS0	I/O	Reserved for factory test
121	SYS1	I/O	
125	SYS2	I/O	
127	SYS3	I/O	
126	SYS4	I/O	
SERIAL COMMUNICATIONS INTERFACE (SCI) PINS			
5	SCLK	I/O	SCI clock
4	RXD	I/O	SCI receive data
3	TXD	I/O	SCI transmit data
RESERVED SERIAL AUDIO INTERFACE PINS			
20	STD0	I/O	Reserved Serial Audio Interface 0 Tx Data or GPIO
21	SCK0	I/O	Reserved Serial Audio Interface 0 Clock or GPIO
22	SRD0	I/O	Reserved Serial Audio Interface 0 Rx Data or GPIO
23	SC00	I/O	Reserved Serial Audio Interface 0 Control 0 or GPIO
24	SC01	I/O	Reserved Serial Audio Interface 0 Control 1 or GPIO
25	SC02	I/O	Reserved Serial Audio Interface 0 Control 2 or GPIO
133	STD1	I/O	Reserved Serial Audio Interface 1 Tx Data or GPIO
134	SCK1	I/O	Reserved Serial Audio Interface 1 Clock or GPIO
135	SRD1	I/O	Reserved Serial Audio Interface 1 Rx Data or GPIO
132	SC10	I/O	Reserved Serial Audio Interface 1 Control 0 or GPIO
131	SC11	I/O	Reserved Serial Audio Interface 1 Control 1 or GPIO
130	SC12	I/O	Reserved Serial Audio Interface 1 Control 2 or GPIO
BOOT MODE SELECT PINS			
61	BMS0	Input	Boot Mode Select 0
62	BMS1	Input	Boot Mode Select 1
65	BMS2	Input	Boot Mode Select 2
66	BMS3	Input	Boot Mode Select 3
TIMER (TIO) PINS			
142, 141, 140	TIO[2:0]	I/O	Timer I/O ports
67	PUMPHI	I/O	Power supply pump control, high side or GPIO
68	PUMPLO	I/O	Power supply pump control, low side or GPIO
69	PSSYNC	I/O	Power supply synchronization or GPIO
PWM PROTECTION PINS			
77, 80, 87, 90	PROTECTA[3:0]	I/O	PWM Temperature status input, or GPIO

TABLE 2. PIN DEFINITIONS, 144-PIN LQFP PACKAGE (Continued)

PIN NUMBER	PORT NAME	TYPE	DESCRIPTION
76, 79, 86, 89	PROTECTB[3:0]	I/O	PWM Over Current Protection inputs, or GPIO.
75, 78, 85, 88	PROTECTC[3:0]	I/O	PWM Shoot Through Current inputs or GPIO.
POWER PINS			
119	PLLAVDD	Power	PLL Analog power
118	PLLAGND	Ground	PLL Analog ground
111	PLLDVDD	Power	PLL Digital power
110	PLLDGND	Ground	PLL Digital ground
114	OSCVDD	Power	Oscillator power
117	OSCGND	Ground	Oscillator ground
11, 27, 44, 59, 81, 91, 122, 136	CVDD	Power	Core power - 8 pins
12, 28, 45, 60, 82, 92, 123, 137	CGND	Ground	Core ground - 8 pins
96, 100, 104, 108	PWMVDD	Power	PWM output pin power - 4 pins
93,97,101,105	PWMGND	Ground	PWM output pin ground.- 4 pins
6, 30, 47, 63, 83, 128	RVDD	Power	Digital pad ring power - 6 pins
7, 31, 48, 64, 84, 129	RGND	Ground	Digital pad ring ground- 6 pins
NO CONNECT PINS			
70, 71, 73, 112, 113	NC		No connect, leave pin floating

Pin Descriptions 144-Pin Package

Pins are 100% firmware and Reference Design Platform (RDP) package dependent for their functionality. Output pins have one of 3 drive strengths - 4mA, 8mA, or 16mA. These strengths are characterized by the current that the pin will source or sink at the specified output voltage level.

SERIAL AUDIO INTERFACE (SAI) PINS

MCLK Master Clock Output

Master Clock output for external ADC/DAC components with 8mA drive strength. Pin drives low on reset. MCLK is also used by test hardware to monitor various internal clocks.

SCKR0 SAI Receiver Bit Clock 1

SAI Receiver 0 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR0 SAI Receiver Left/Right Clock 0

SAI Receiver 0 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN0 SAI Receiver Serial Data Input 0

SAI Receiver 0 data input.

SCKR1 SAI Receiver Bit Clock 1

SAI Receiver 1 bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

LRCKR1 SAI Receiver Left/Right Clock 1

SAI Receiver 1 left/right audio frame clock is an output when D2-814xx is a master or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. Input has hysteresis.

SDIN1 SAI Receiver Serial Data Input 1

SAI Receiver 1 data input.

SCKT SAI Transmitter Bit Clock

SAI Transmitter bit clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. SCKT is used to monitor the 3.3V brownout detector during the POR hardware test.

LRCKT SAI Transmitter Left/Right Clock

SAI Transmitter left/right audio frame clock is an output when D2-814xx is a master, or an input when D2-814xx is a slave. Defaults to an input on reset. Output has 4mA drive strength. LRCKT is used to monitor the 1.8V brown out detector during the POR Hardware test. LRCKT is used to monitor PLL Lock during the PLL Hardware test.

SDOUT Serial Data Output

SAI Transmitter data output with 4mA drive strength. Pin drives low on reset.

S/PDIF PINS

SPDIFRX S/PDIF Data Input

This pin is the S/PDIF audio input and accepts a 3.3V stereo input up to 192kHz. To drive this pin, appropriate buffer and/or isolation circuits may be necessary to convert the S/PDIF cable input signal to clean logic levels.

SPDIFTX S/PDIF Data Output

This pin is the S/PDIF audio output and drives a 3.3V stereo output up to 192kHz.

PWM PINS

PWMxH PWM High Side Driver Outputs

PWM high side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives to state determined by OTSEL on reset.

PWMxL PWM Low Side Driver Outputs

PWM low side driver outputs, where x is 0 to 3, with 16mA drive strength. Pin drives low on reset.

OTSEL Output Topology Select Input

Output topology select input. OTSEL pin state controls the PWMxH drive polarity. Typically, OTSEL will be tied either high for active-low PWMxH FET drivers, or tied low for active-high PWMxH FET drivers.

PWMSYNC PWM Synchronization

PWM synchronization port with 4mA drive. Used in multi-D2-814xx configurations to synchronize the PWM controllers. The master D2-814xx will drive synchronization data to the slave D2-814xx(s), thus the pin will be an output on the master D2-814xx and an input on the slave D2-814xx(s). Pin floats on reset.

2-WIRE SERIAL PINS

SCL Serial Clock

Two-Wire Serial clock port, open drain driver with 4mA drive strength. Bidirectional signal is used by both the master and slave controllers for clock signaling.

SDA Serial Data

Two-Wire Serial data port, open drain driver with 4mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport.

XGPIO PINS

XGPIO[15:0] Extended General Purpose I/O

Bidirectional GPIO port with 4mA driver. Resets to input port.

RESET AND TEST PINS

nRESET System Reset Input

Active low reset input with hysteresis. Low level activates system level reset, initializing all internal logic and program operations. System latches boot mode selection on the IRQ input pins on the rising edge.

nRSTOUT System Reset Output

Active low reset output with 4mA driver. Pin drives low on any of POR output, 3.3V brown out detector, 1.8V brown out detector.

TEST Test Mode Input

Hardware test mode control. For D2Audio usage only. Must be tied low.

nTRST Test Reset Input

Active low test port reset. Low level activates test reset, initializing test hardware. Must be driven low with nRESET.

CRYSTAL OSCILLATOR AND PLL PINS

OSCOUT Oscillator Output

Analog oscillator output to slave D2-814xx devices. On reset, OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin. May be turned off by program control.

XTALI Crystal Oscillator Input

Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-814xx systems, the OSCOUT from the master D2-814xx would drive the XTALI pin.

XTALO Crystal Oscillator Output

Crystal oscillator analog output port. When using an external clock source, this pin must be open.

GPIO PINS

GPIO[7:0] General Purpose I/O

Bidirectional GPIO ports with 4mA driver. Resets to input ports.

SYSTEM CONFIGURATION PINS

SYS0 System Configuration Data 0

Reserved for factory test. Tie low with 10kΩ resistor.

SYS1 System Configuration Data 1

Reserved for factory test. Tie high with 10kΩ resistor.

SYS2 System Configuration Data 2

Reserved for factory test. Tie high with 10kΩ resistor.

SYS3 System Configuration Data 3

Reserved for factory test. Tie high with 10kΩ resistor.

SYS4 System Configuration Data 4

Reserved for factory test. Tie high with 10kΩ resistor.

SERIAL COMMUNICATIONS INTERFACE (SCI) PINS

SCLK Serial Clock

Serial communications clock with 4mA drive and hysteresis on input. Resets to input port. May be configured to GPIO.

RXD Receive Data

Serial communications receiver data with 4mA drive. Resets to input port. May be configured to GPIO.

TXD Transmit Data

Serial communications transmitter data with 4mA drive. Resets to input port. May be configured to GPIO.

OPTIONAL/RESERVED FUNCTION PINS

SCK0 Reserved Serial Audio Interface 0 Serial Clock

Serial Audio Interface 0 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC00-SC02 Reserved Serial Audio Interface 0 Serial Control

Serial Audio Interface 0 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD0 Reserved Serial Audio Interface 0 Serial Transmit Data

Serial Audio Interface 0 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD0 Reserved Serial Audio Interface 0 Serial Receive Data

Serial Audio Interface 0 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

SCK1 Reserved Serial Audio Interface 1 Serial Clock

Serial Audio Interface 1 serial clock port with 4mA driver and hysteresis receiver. Resets to input port. May be configured as GPIO.

SC10-SC12 Reserved Serial Audio Interface 1 Serial Control

Serial Audio Interface 1 serial control port with 4mA driver. Resets to input port. May be configured as GPIO.

STD1 Reserved Serial Audio Interface 1 Serial Transmit Data

Serial Audio Interface 1 serial transmit data port with 4mA driver. Resets to input port. May be configured as GPIO.

SRD1 Reserved Serial Audio Interface 1 Serial Receive Data

Serial Audio Interface 1 serial receive data port with 4mA driver. Resets to input port. May be configured as GPIO.

BOOT MODE SELECT PINS

BMS[3:0] Boot Mode Select Inputs

External boot mode select inputs. On nRESET deassertion, these pins provide the boot mode selection.

TIMER (TIO) PINS

TIO[2:0] Timer

Timer I/O ports with 4mA driver. May be configured as GPIO.

PUMPHI Power Supply Pump High

High side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PUMPLO Power Supply Pump Low

Low side power supply pump output with 16mA driver. May be configured as GPIO. Drives low on reset. Provides control means for operating an external switching power supply.

PSSYNC Power Supply Synchronization

Switching power supply synchronization signal with 16mA driver. May be configured as GPIO. Resets to input port.

PWM PROTECTION PINS

PROTECTA[3:0] PWM Temperature Protection Inputs

PWM temperature protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMTEMP input is associated with the corresponding PWM driver channel.

PROTECTB[3:0] PWM Overcurrent Protection Inputs

PWM overcurrent protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMOCP input is associated with the corresponding PWM driver channel.

PROTECTC[3:0] PWM Shoot-Through Current Protection

PWM shoot-through-current protection inputs with hysteresis. May be configured as GPIO. In this instance, the GPIO pins each have a 4mA driver. Each PWMSTC input is associated with the corresponding PWM driver channel.

POWER PINS

PLLAVDD/PLLAGND PLL Analog power and ground

PLL analog supply/return. This 1.8V supply is used for the jitter critical sections of the PLL.

PLLDVDD/PLLDGND PLL Digital power and ground

PLL digital supply/return. This 1.8V supply is used for the “dirty” sections of the PLL, and provides the pad supplies for all of the analog pads. Note that PLLDGND and CGND are connected through the substrate.

OSCVDD/OSCGND Oscillator power and ground

Oscillator supply/return. This 1.8V supply is used for the crystal oscillator and oscillator bias circuits only.

CVDD/CGND Core power and ground

Core supply/return. This 1.8V supply is used in the chip interior logic and pad ring interfaces. There are 8 core supply pad pairs internally connected around the pad ring.

PWMVDD/PWMGND PWM driver power and ground

PWM I/O pad driver supply/return. This 3.3V supply is used for the PWM pad drivers only. There are 4 PWM internally connected supply pairs, one for each PWM data channel.

RVDD/RGND Pad Ring power and ground

Ring I/O pad driver supply/return. This 3.3V supply is used for all the digital I/O pad drivers and receivers except for the PWM and analog pads. There are 6 ring supply pairs internally connected around the pad ring.

D2-814xx Reset and Boot Modes

Reset

D2-814xx has a two reset inputs - the nRESET and nTRST input pins. The nRESET input pin is effectively a power-on system reset. All internal state logic, except internal test hardware, is initialized by nRESET. While reset is active the system is held in the reset condition. The reset condition is defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled. The nTRST input resets internal factory test hardware only.

To assure proper system initialization, the nTRST input pin must be asserted along with nRESET.

TABLE 3. POWER ON RESET TIMING DETAILS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t-1.8Vgood	Valid 1.8V power before nRESET release	10			ns
t-3.3Vgood	Valid 3.3V power before nRESET release	10			ns
tBMSsu	Boot Mode Select (BMS[3:0]) setup	10			ns
tBMShld	Boot Mode Select (BMS[3:0]) hold	0			ns

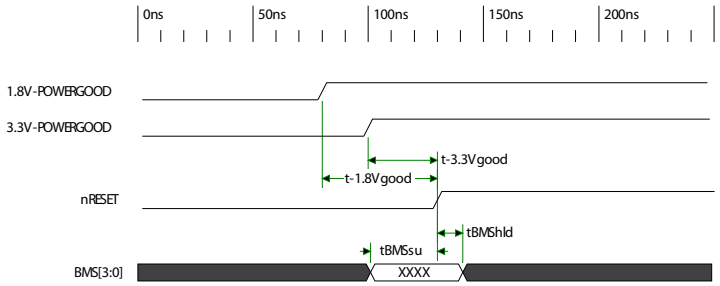

FIGURE 7. POWER ON RESET TIMING

Boot Modes

The boot mode is determined by the BMS[3:0] pin inputs. The BMS[3:0] pin state is latched on the deassertion of system reset. It is expected that the application board will have pull-ups in the BMS[3:0] pins, so that the desired boot mode is selected by default. Table 4 defines the boot modes.

TABLE 4. BOOT MODES

MODE	BMS[3:0]	M/S	INTERFACE SPEED	DESCRIPTION
0	0000			RESERVED
1	0001	M	400kb/s	ROM on 2-wire 0 port
2	0010	S	384Kb/s	Fast Asynchronous SCI slave boot (ex: D2-814xx to D2-814xx)
3	0011	S	per Master	SPI slave
7	0111	M	384Kb/s	2-wire ROM on GPIO port (SCL=GPIO7, SDA = GPIO6)
8	1000			RESERVED
9	1001			RESERVED
A	1010			RESERVED
B	1011			RESERVED
C	1100	S	per Master	2-wire slave boot from micro, address = 1000100x
D	1101			RESERVED
E	1110			RESERVED
F	1111			RESERVED

The Interface Speed specification is the speed at which the interface is configured to operate by the boot code. For the selection where the interface speed is “per Master”, the interface must operate within the requirements of the selected interface specification. For example, the EEPROM boot speed with 2-wire interface is 400kHz.

TABLE 5. EXTERNAL HOST BOOT TIMING DETAILS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tBMSsu	Boot Mode Select (BMS[3:0]) setup	10			ns
tBMShld	Boot Mode Select (BMS[3:0]) hold	0			ns
tEXTbootRDY	2-Wire external source ready to boot	2400000			ns

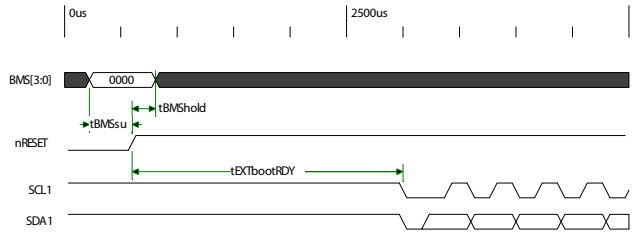

FIGURE 8. EXTERNAL HOST BOOT TIMING

TABLE 6. 2-WIRE EEPROM BOOT TIMING DETAILS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tEEboot	2-Wire EE boot delay	2650000			ns
tBMSsu	Boot Mode Select (BMS[3:0]) setup	10			ns
tBMShld	Boot Mode Select (BMS[3:0]) hold	0			ns

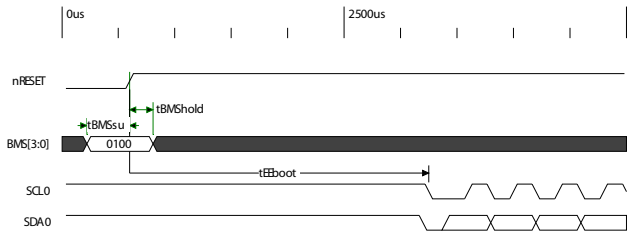

FIGURE 9. 2-WIRE EEPROM BOOT TIMING

Document Revision History

07/25/05 REVISION 0.0.1 - FIRST INTERNAL RELEASE.
Created new data sheet template, updated product features, included new drawings of 128-pin package, included new 128-pin pinout and pin name descriptions.
08/12/05 REVISION 0.0.2 - SECOND INTERNAL RELEASE.
Updated product features, included new drawings of 128-pin/144-pin package, included new 144-pin pinout and pin name descriptions.
08/15/05 REVISION 0.0.3 - THIRD INTERNAL RELEASE.
Updated pins in 128-pin/144-pin package drawings, eliminated signal flow diagram, added 2 part numbers.
08/17/05 REVISION 0.0.4 - FOURTH INTERNAL RELEASE.
Updated IC image on master pages, added Section 8.1 “0” performance option, renamed document, updated cover page.
09/14/05 REVISION 0.0.5 - FIFTH INTERNAL RELEASE.
Updated all 128/144 package pinout tables and descriptions, removed waveforms, added block diagram, updated cover page.
10/20/05 REVISION 1.0.0 - FIRST EXTERNAL RELEASE.
Updated cover page, updated block diagram Serial Audio Interface, updated OTSEL pin description, added 2-Wire interface and Serial Audio Port sections, added firmware and reference design disclaimers, updated part numbers.
12/6/05 REVISION 1.0.1
Updated SYS0 pin from tie-high to tie-low.
12/22/05 REVISION 1.0.2
Corrected cover page feature set descriptions, corrected Available Part Numbers in Ordering table.
1/31/06 REVISION 1.0.3
Changed 128-pin package pinouts in Figure 5 on page 8, and Table 1 on page 9.
2/7/06 REVISION 1.0.4
Changed text on cover page regarding valid boot modes. Updated Figure 1 on page 4 to relabel the Serial Audio block to Serial Audio Interface block. Renamed Serial Audio Interface block to be Reserved Serial Audio Interface block. Updated text in “D2-814xx Signal Flow” on page 4. Changed “module” to “IC” in “Serial Audio Interface (SAI ports)” on page 6. Updated text in Table 1 on page 9 to change “Serial Audio (SAI) Pins” to be “Serial Audio Interface (SAI) Pins”. Updated text in Table 1 on the following page to change “Serial Audio Interface Pins” to be “Reserved Serial Audio Interface Pins” in both header and pin description sections. Changed title in “Serial Audio Interface (SAI) Pins” on page 11 from “Serial Audio (SAI) Pins” to be “Serial Audio Interface (SAI) Pins”. Changed SPDIF to S/PDIF in section “Serial Audio Interface (SAI) Pins” on page 11. Deleted “or nRESET active low” from “Reset and Test Pins” on page 12 and in “Reset and Test Pins” on page 18 from the nRSTOUT pin description. Changed the title in “Optional/Reserved Function Pins” on page 12 from “Optional Function Pins” to “Optional/Reserved Function Pins”. Changed the pin descriptions in this section to now have a “Reserved” in front. Changed text in “PWM Protection Pins” on page 13 on all pin descriptions. Relabeled pin “SDO” to “SDOUT” in Figure 6 on page 14, in Table 2 on page 15 as well as in “Serial Audio Interface (SAI) Pins” on page 17.
2/8/06 REVISION 1.0.5
Changed all related text, pin descriptions and pinout drawings for CTRL0, CTRL1, CTRL2, CTRL3. CTRL0 is now PUMPHI. CTRL1 is now PUMPLO. CTRL2 is now PSSYNC. CTRL3 is now PWMSYNC.
2/20/06 REVISION 1.0.6
Added Junction Temperature to Table 1, “ABSOLUTE MAXIMUM RATINGS,” on page 5 in addition to Note 1 on Operating Temperature, Storage Temperature and Storage Temperature. Added Table 4, “THERMAL CHARACTERISTICS,” on page 6 which shows Theta J_A and J_C values for 128-pin and 144-pin LQFP packages.
3/27/06 REVISION 1.1.1
Updated Theta J_A and J_C values for 128-pin and 144-pin LQFP packages in Table 4, “THERMAL CHARACTERISTICS,” on page 6.
7/17/06 REVISION 1.1.2
Changed Core Supply Pins CVDD from 300 mA to 325 mA in Table 3, “POWER REQUIREMENTS,” on page 6
Updated Environment Category in Section , “IC Part Numbering Scheme,” on page 25
Swapped Theta J_A and J_C values for 128-pin and 144-pin LQFP packages in Table 4, “THERMAL CHARACTERISTICS,” on page 6
11/29/06 REVISION 1.1.3
Added [3:0] vector to Table 4, “BOOT MODES,” on page 20
Added timing details Table 3, “POWER ON RESET TIMING DETAILS,” on page 20, Table 5, “EXTERNAL HOST BOOT TIMING DETAILS,” on page 21, Table 6, “2-WIRE EEPROM BOOT TIMING DETAILS,” on page 21

Document Revision History (Continued)

Added timing sequence figures Figure 7, “POWER ON RESET TIMING,” on page 20, Figure 8, “EXTERNAL HOST BOOT TIMING,” on page 21, Figure 9, “2-WIRE EEPROM BOOT TIMING,” on page 21
10/4/07 REVISION 1.1.4
Added new part numbers (D2-81434-LR and D2-81435-LR) on page 1 and pages 32, 33
Revised part descriptions to include new part numbers
3/5/10 REVISION FN6786.0
Converted to Intersil format. Assigned file number FN6786. Rev 0 - first release with this file number. Removed part numbering scheme and replaced available parts with ordering information table.

Trademarks

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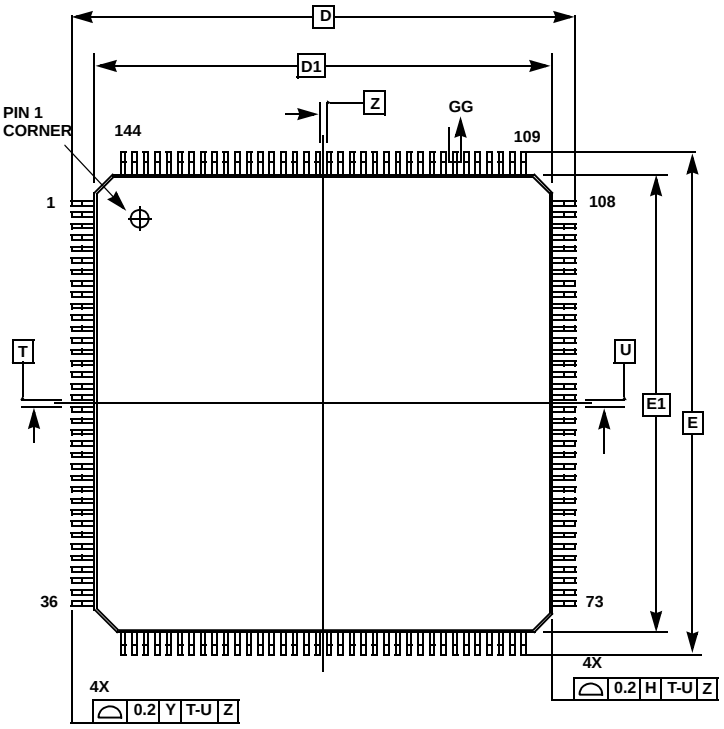
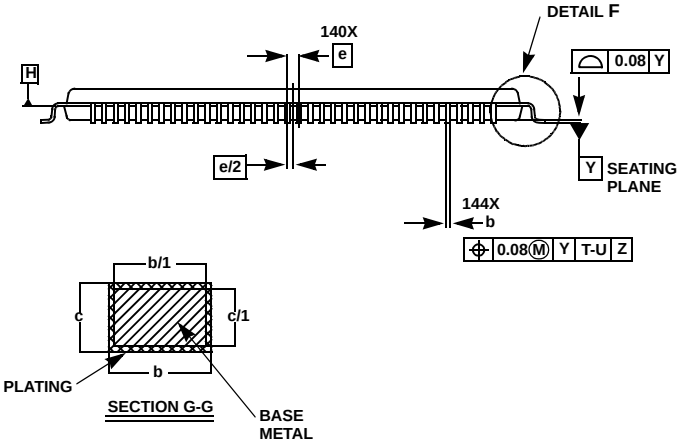
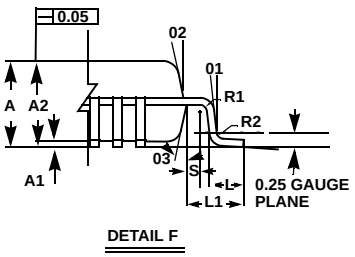
Thin Plastic Quad Flatpack Package (LQFP)







Q144.20x20B

144 Lead Thin Plastic Quad Flatpack Package

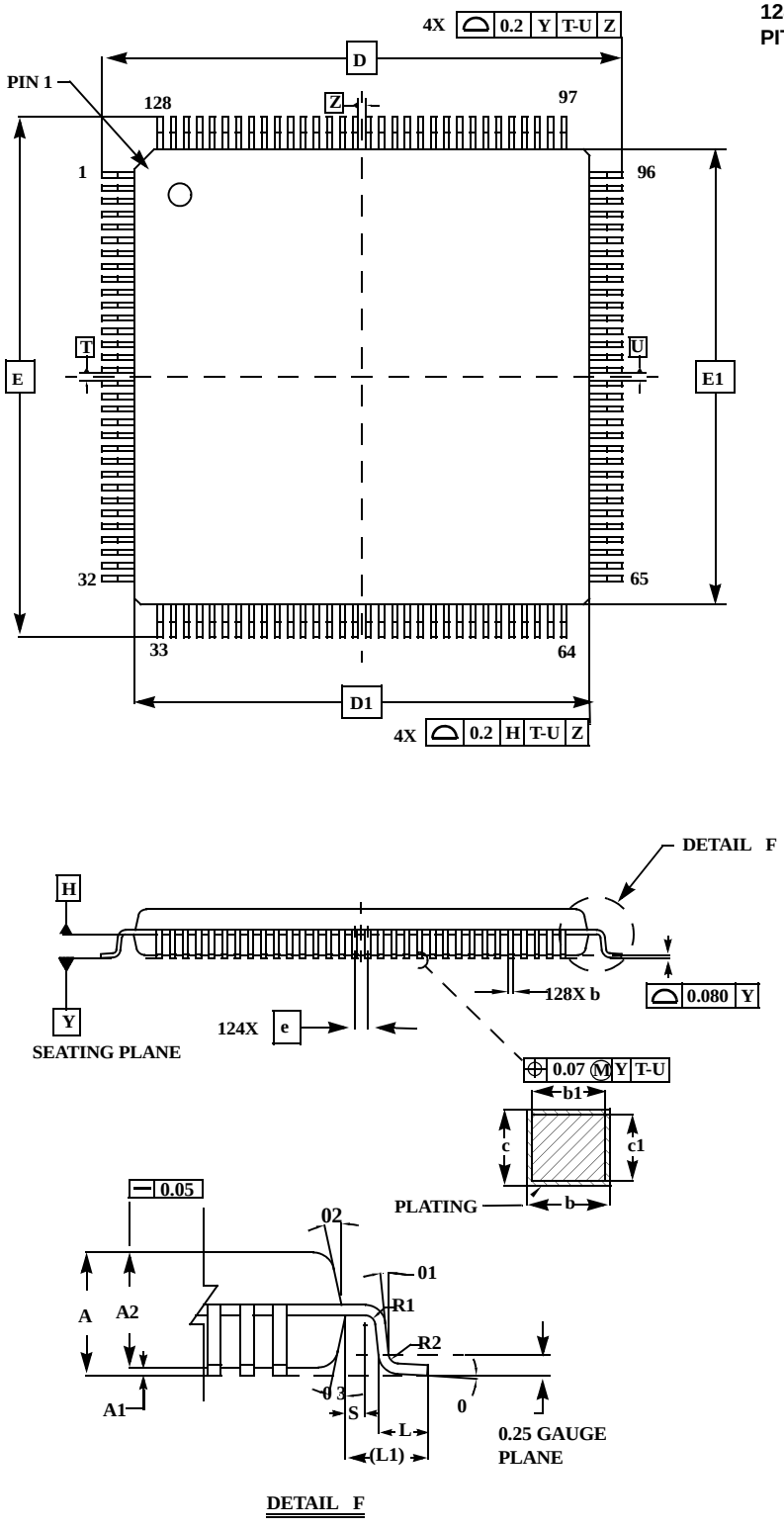
SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-	-	1.60	
A1	0.05	-	0.15	
A2	1.35	1.40	1.45	
b	0.17	0.22	0.27	4
b1	0.17	0.20	0.23	
c	0.09	-	0.20	
c1	0.09	-	0.16	
D	22 BSC			
D1	20 BSC			3
E	22 BSC			
E1	20 BSC			3
L	0.45	0.60	0.75	
L1	1.00 REF			
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
θ	0°	3.5°	7.0°	
θ1	0°	-	-	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
N	128			5
e	0.50 BSC			

Rev. 0 9/08

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are inclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm.
5. N is total number of the lead terminals.

Thin Plastic Quad Flatpack Packages (LQFP)



Q128.14x14

128 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH

SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D	16 BSC			-
D1	14 BSC			3
E	16 BSC			-
E1	14 BSC			3
L	0.45	0.60	0.75	-
L1	1.00 REF			-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N	128			-
e	0.40 BSC			-

Rev. 0 8/08

NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.