

4AM15

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

ADE-208-1213 (Z)

1st. Edition

Mar. 2001

Application

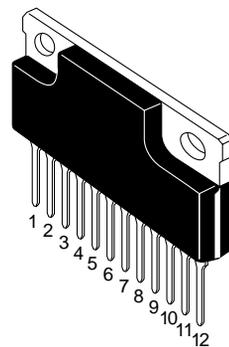
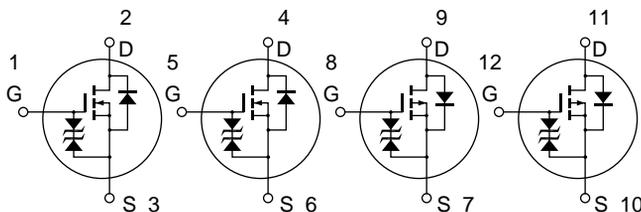
High speed power switching

Features

- Low on-resistance
N Channel: $R_{DS(on)} = 0.5 \Omega$, $V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$
P Channel: $R_{DS(on)} = 0.9 \Omega$, $V_{GS} = -10 \text{ V}$, $I_D = -2 \text{ A}$
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline

SP-12TA



1, 5, 8, 12. Gate
2, 4, 9, 11. Drain
3, 6, 7, 10. Source

4AM15

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		
		Nch	Pch	Unit
Drain to source voltage	V_{DSS}	200	-200	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	4	-4	A
Drain peak current	$I_{D(pulse)}^{*1}$	16	-16	A
Body to drain diode reverse drain current	I_{DR}	4	-4	A
Channel dissipation	$Pch (Tc = 25°C)^{*2}$	32		W
	Pch^{*2}	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

Notes: 1. PW 10 μs, duty cycle 1%
2. 4 Device Operation

Electrical Characteristics (Ta = 25°C)

Item	Symbol	N Channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 160 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.33	0.5		$I_D = 2 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.5	3.0	—	S	$I_D = 2 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	750	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	260	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	40	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	19	—	ns	$I_D = 2 \text{ A}$
Rise time	t_r	—	26	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	$R_L = 15$
Fall time	t_f	—	24	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_F = 4 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	125	—	ns	$I_F = 4 \text{ A}, V_{GS} = 0,$ $diF/dt = 100 \text{ A}/\mu\text{s}$

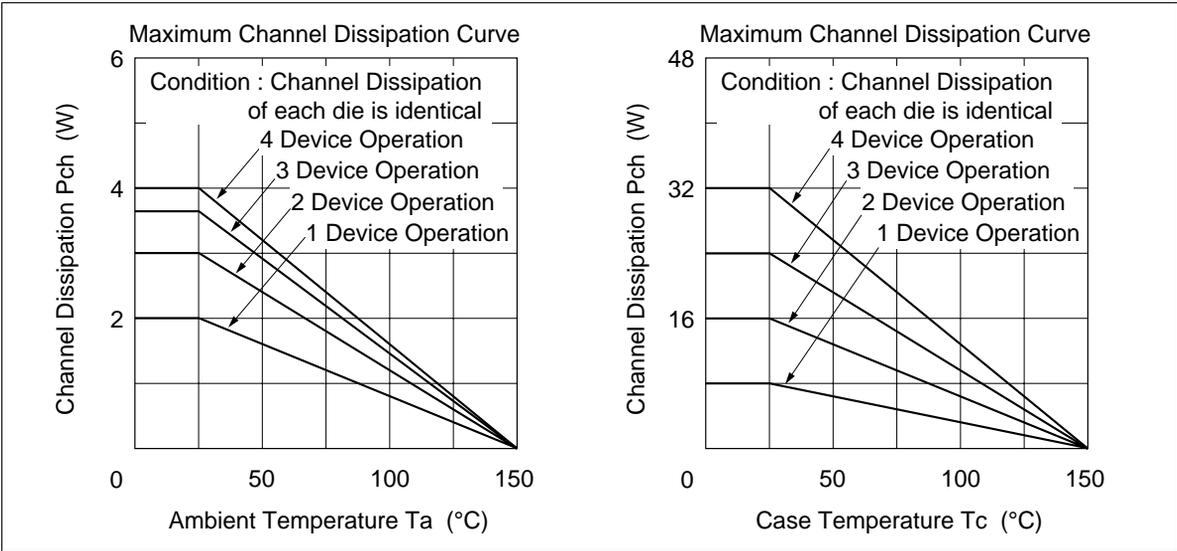
Note: 1. Pulse Test

See characteristic curves of 2SK1957

Electrical Characteristics (Ta = 25°C)

Item	Symbol	P Channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	-200	—	—	V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-250	μA	$V_{DS} = -160 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-2.0	—	-4.0	V	$I_D = -1 \text{ mA}, V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.9		$I_D = -2 \text{ A}, V_{GS} = -10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.5	3.0	—	S	$I_D = -2 \text{ A}$ $V_{DS} = -10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	920	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	23 0	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	70	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$I_D = -2 \text{ A}$
Rise time	t_r	—	40	—	ns	$V_{GS} = -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	$R_L = 15$
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.0	—	V	$I_F = -4 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	170	—	ns	$I_F = -4 \text{ A}, V_{GS} = 0,$ $diF/dt = 100 \text{ A}/\mu\text{s}$

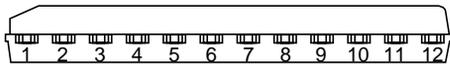
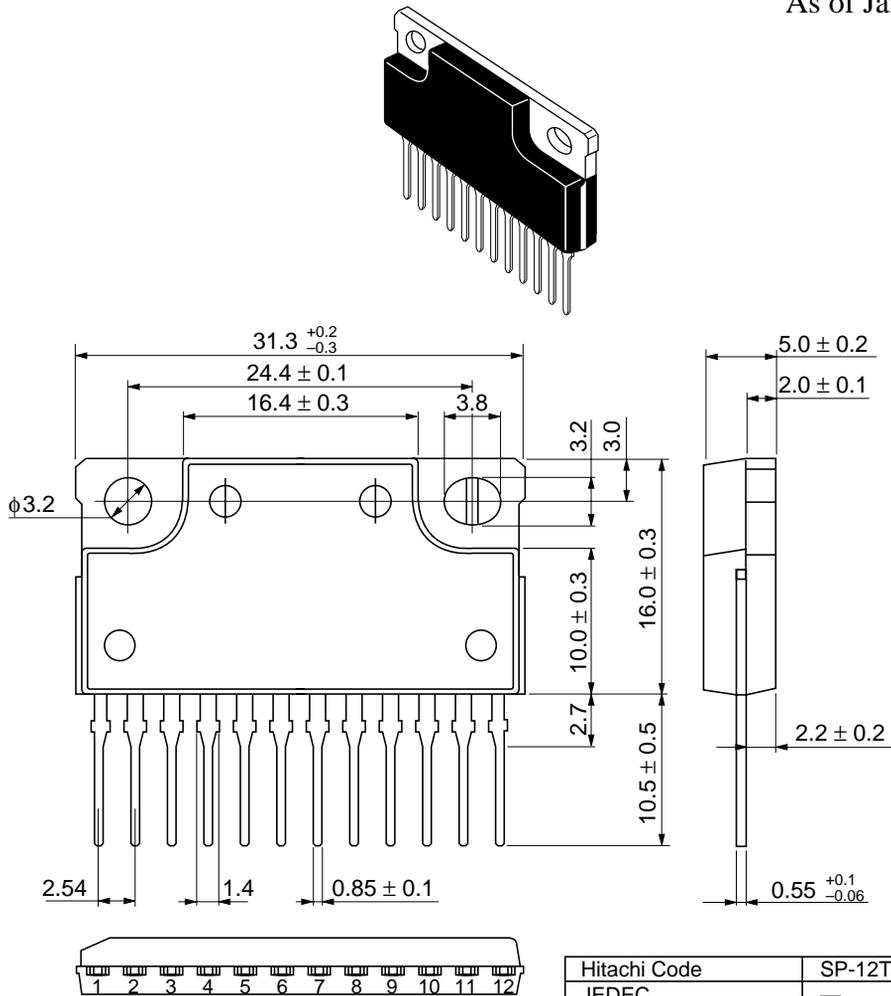
Note: 1. Pulse Test



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SP-12TA
JEDEC	—
EIAJ	—
Mass (reference value)	6.1 g

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