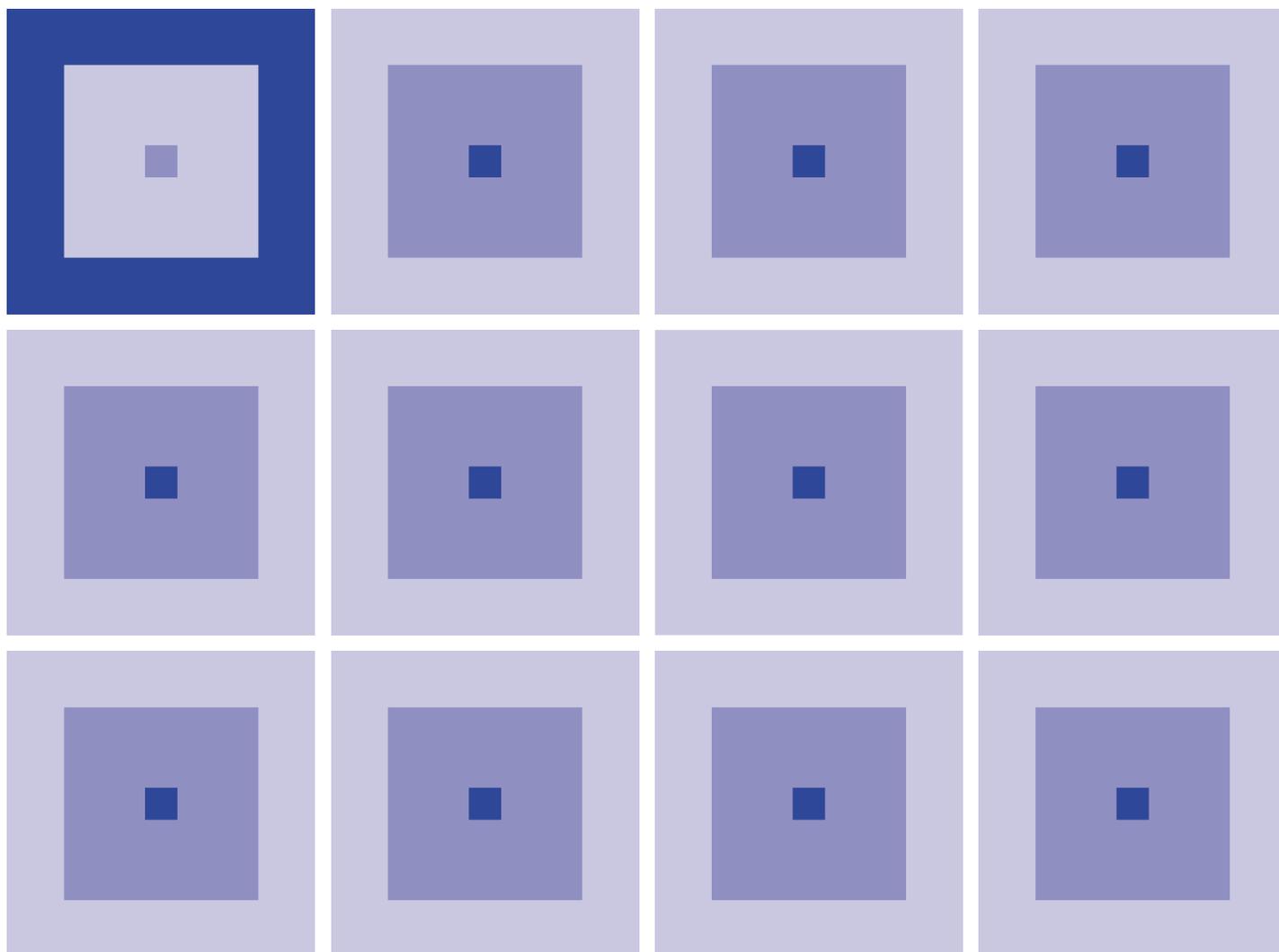


STANDARD CELL / EMBEDDED ARRAY

S1K70000 / S1X70000 Series DESIGN GUIDE



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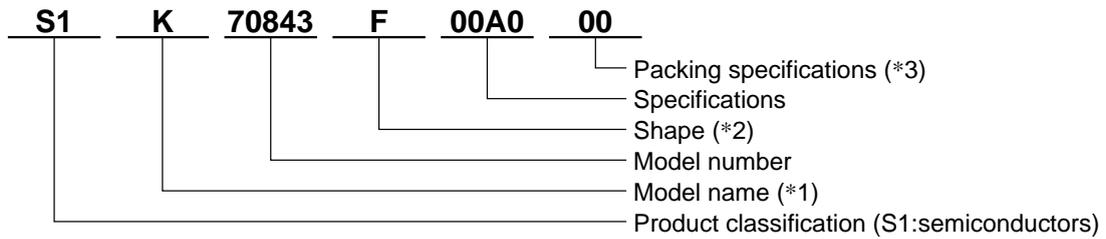
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Configuration of product number

●DEVICES



*1: Model name

K	Standard Cell
L	Gate Array
X	Embedded Array

*2: Shape

B	Assembled on board, COB, BGA
C	Plastic DIP
D	Bare Chip
F	Plastic QFP
H	Ceramic DIP
L	Ceramic QFP

M	Plastic SOP
R	TAB-QFP
T	Tape Carrier (TAB)
2	TSOP (Standard Bent)
3	TSOP (Reverse Bent)

*3: Packing Specifications

14th	15th	Packing Specifications
0	0	Besides tape & reel
0	A	TCP BL 2 directions
0	B	Tape & reel Back
0	C	TCP BR 2 directions
0	D	TCP BT 2 directions
0	E	TCP BD 2 directions
0	F	Tape & reel FRONT
0	G	TCP BT 4 directions
0	H	TCP BD 4 directions
0	J	TCP SL 2 directions
0	K	TCP SR 2 directions
0	L	Tape & reel LEFT
0	M	TCP ST 2 directions
0	N	TCP SD 2 directions
0	P	TCP ST 4 directions
0	Q	TCP SD 4 directions
0	R	Tape & reel RIGHT
9	9	Specs not fixed

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Chapter 1 Overview

Epson's S1K70000 series consists of ultra-high-speed, super-integrated CMOS-type standard cells manufactured by the 0.18- μm process. The MSI (Basic Cell type) available in this series in particular may be chosen to create conventional embedded arrays (S1X70000 series).

1.1 Features

1.1.1 Outline of the S1K/S1X70000 Series

- Integration 55.3k gates/mm² (Basic Cell type)
75.1k gates/mm² (Cell-Based type)
- Operating Speed Internal gates
INV, F/O = 1, V_{DD} = 1.8 V, Typ.Condition

Type of Transistor	Basic Cell Type	Cell-Based Type	Unit
Standard 1	25.9	26.5	ps
Standard 2	24.8	24.9	ps
High-Performance	21.4	23.2	ps
Low-Leakage	TBD	TBD	ps

INV, F/O = 1, V_{DD} = 1.5 V, Typ.Condition

Type of Transistor	Basic Cell Type	Cell-Based Type	Unit
Standard 1	33.7	34.4	ps
Standard 2	30.5	30.2	ps
High-Performance	25.5	27.2	ps
Low-Leakage	TBD	TBD	ps

NA2, F/O = 1, V_{DD} = 1.8 V, Typ.Condition

Type of Transistor	Basic Cell Type	Cell-Based Type	Unit
Standard 1	43.6	38.9	ps
Standard 2	43.2	38.8	ps
High-Performance	36.0	33.1	ps
Low-Leakage	TBD	TBD	ps

NA2, F/O = 1, V_{DD} = 1.5 V, Typ.Condition

Type of Transistor	Basic Cell Type	Cell-Based Type	Unit
Standard 1	57.7	51.6	ps
Standard 2	53.7	48.2	ps
High-Performance	43.3	39.9	ps
Low-Leakage	TBD	TBD	ps

© Input buffers

F/O = 2, Standard Wiring Load, Typ. Condition

Voltage	Operating Speed		Unit
	3.3-V Input Buffer (Y Type)	2.5-V Input Buffer (X Type)	
3.3 V/1.8 V	181	—	ps
2.5 V/1.8 V	193	152	ps
1.8 V	255	191	ps
1.5 V	307	239	ps

© Output buffers

CL = 15pF, Typ. Condition

Voltage	Operating Speed		Unit
	3.3-V Input Buffer (Y Type)	2.5-V Input Buffer (X Type)	
3.3 V/1.8 V	1.51	—	ns
2.5 V/1.8 V	1.67	1.28	ns
1.8 V	2.12	1.73	ns
1.5 V	2.71	2.21	ns

- Process 0.18 μ m, 3/4/5/6-layered metalization
- Interface Levels
 - © 3.3-V buffers (Y type)
LVCMOS-, LVTTL-compatible
 - © 2.5-V buffers (X type)
LVCMOS-compatible
- Input Modes
 - © 3.3-V buffers (Y type)
LVCMOS, LVTTL, LVCMOS Schmitt
PCI-3 V, Gated input, Fail Safe input
May be provided with internal pull-up and pull-down resistors (two resistance values for each)
 - © 2.5-V buffers (X type)
LVCMOS, LVCMOS Schmitt
Gated input, Fail Safe input
May be provided with internal pull-up and pull-down resistors (two resistance values for each)
- Output Modes Normal, 3-state, Bi-directional, and Fail Safe outputs

- Drive Output
 - ◎ 3.3-V buffers (Y type)
 - $I_{OL} = 2, 4, 8, \text{ or } 12 \text{ mA}$ selectable (HV_{DD} = 3.3 V)
 - $I_{OL} = 1.5, 3, 6, \text{ or } 9 \text{ mA}$ selectable (HV_{DD} = 2.5 V)
 - $I_{OL} = 1, 2, 4, \text{ or } 6 \text{ mA}$ selectable (V_{DD} = 1.8 V)
 - $I_{OL} = 0.75, 1.5, 3, \text{ or } 4.5 \text{ mA}$ selectable (V_{DD} = 1.5 V)
 - ◎ 2.5-V buffers (X type)
 - $I_{OL} = 2, 4, 8, \text{ or } 12 \text{ mA}$ selectable (HV_{DD} = 2.5 V)
 - $I_{OL} = 1.5, 3, 6, \text{ or } 9 \text{ mA}$ selectable (V_{DD} = 1.8 V)
 - $I_{OL} = 1, 2, 4, \text{ or } 6 \text{ mA}$ selectable (V_{DD} = 1.5 V)
- Memory
 - ◎ Basic Cell-type RAM
 - Synchronous, 1 port; Synchronous, 2 ports
 - ◎ High-Density-type RAM
 - Synchronous, 1 port; Synchronous, dual ports
 - ◎ Large Capacity-type RAM
 - Synchronous, 1 port
 - ◎ ROM
 - Synchronous
- Built-in level shifter for operation with dual supply voltages
 - Internal logic: Operates with low voltage
 - Input/output buffers: Can be interfaced with high and low voltages

1.1.2 Internal Structure of the S1K/S1X70000 Series

The S1K/S1X70000 series is constructed with an MSI cell area and an input/output buffer circuit area, as shown in Figure 1-1.

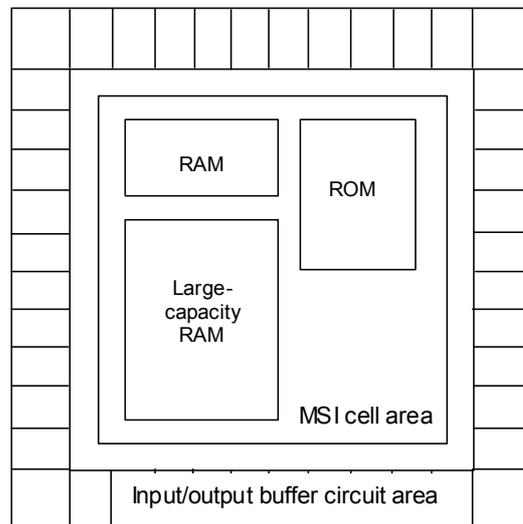


Figure 1-1 Outline Structure of the S1K/S1X70000 Series

Various MSI cells and memory blocks can be located in the MSI cell area, depending on the desired circuit. These cells can be interconnected in order to implement the desired circuit.

The input/output buffer area contains input buffers, output buffers, bi-directional buffers, and power-supply cells. In this area, signals are exchanged between external circuits and the units of the S1K70000 series.

1.1.3 Structure and Types of MSIs

The S1K70000 series is available in two types: Basic Cell-type MSI for E/A (embedded arrays S1X70000 series) and Cell Based-type MSI for S/C (standard cells).

Embedded arrays (E/A) excel in that they feature a short development period and allow circuit changes to be responded easily, while the standard cells (S/C) feature high integration and low power consumption. Either type can be selected in accordance with customer needs (however, these two types of MSIs cannot be used at the same time).

Furthermore, four MSI libraries are available to choose from: a Standard 1 library suitable for low-leakage-current (quiescent current) applications, a Standard 2 library suitable for applications that require high-speed operation, a High-Performance library suitable for applications that require ultra-high-speed operation, and a Low-Leakage library suitable for ultra-low-leakage current (quiescent current) applications. This wide availability enables the selection of a library best suited to customer needs (however, these four libraries basically cannot be used in combination).

Memory is also available in various types in addition to the Basic Cell-type RAM (Standard 1 type, High-Performance type, and Low-Leakage type). These include a highly integrated Cell Based-type RAM (with 1 port, 2 ports, or 1 large-capacity port, all of which are available only for the Standard 1 type) and a ROM (only for Standard 1). The most suitable memory type can be selected in accordance with customer needs.

For details on MSI cell types, refer to Chapter 3, "MSI Cells." For details on memory, refer to Chapter 5, "Memory Block."

1.1.4 Structure and Types of Input/Output Buffers

Two types of input/output buffers are available for the S1K/S1X70000: 3.3-V input buffers (Y type) designed to enable high-speed 3.3-V interfacing, and 2.5-V input/output buffers (X type) designed to allow for high-speed 2.5-V interfacing.

One of these two types can be selected in accordance with customer needs (however, the Y and X types cannot be used in combination).

For details on input/output buffers, refer to Chapter 4, "Types of Input/Output Buffers and Their Use."

1.2 Electrical Characteristics and Specifications

1.2.1 When Using 3.3-V Input/Output Buffers (Y Type)

Table 1-1 Absolute Maximum Ratings (for a Single Power Supply)

($V_{SS} = 0$ [V])

Parameter	Symbol	Limits	Unit
Power-Supply Voltage	V_{DD}	-0.3 to +2.5	V
Input Voltage	V_I	-0.3 to $V_{DD} + 0.5^{*1}$	V
Output Voltage	V_O	-0.3 to $V_{DD} + 0.5^{*1}$	V
Output Current/Pin	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

Table 1-2 Absolute Maximum Ratings (for Dual Power Supplies)

($V_{SS} = 0$ [V])

Parameter	Symbol	Limits	Unit
Power-Supply Voltage	HV_{DD}^{*3}	-0.3 to +4.0	V
	LV_{DD}^{*3}	-0.3 to +2.5	V
Input Voltage	HV_I	-0.3 to $HV_{DD} + 0.5^{*1}$	V
	LV_I	-0.3 to $LV_{DD} + 0.5^{*2}$	V
Output Voltage	HV_O	-0.3 to $HV_{DD} + 0.5^{*1}$	V
	LV_O	-0.3 to $LV_{DD} + 0.5^{*2}$	V
Output Current/Pin	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use -0.3 V to +4.0 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: $HV_{DD} \geq LV_{DD}$

Table 1-3 Recommended Operating Conditions (for a Single Power Supply at $V_{DD} = 1.8\text{ V}$) $(V_{SS} = 0\text{ [V]})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage	V_{DD}	1.65	1.80	1.95	V
Input Voltage	V_I	V_{SS}	—	V_{DD}^{*1}	V
Ambient Temperature	T_a	0 -40	25 25	70^{*2} 85^{*3}	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*2: The ambient temperature range is recommended for $T_j = 0$ to $+85\text{ [°C]}$.

*3: The ambient temperature range is recommended for $T_j = -40$ to $+125\text{ [°C]}$.

Table 1-4 Recommended Operating Conditions (for a Single Power Supply at $V_{DD} = 1.5\text{ V}$) $(V_{SS} = 0\text{ [V]})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	V_{DD}	1.40	1.50	1.60	V
Power-Supply Voltage	V_I	V_{SS}	—	V_{DD}^{*1}	V
Ambient Temperature	T_a	0 -40	25 25	70^{*2} 85^{*3}	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*2: The ambient temperature range is recommended for $T_j = 0$ to $+85\text{ [°C]}$.

*3: The ambient temperature range is recommended for $T_j = -40$ to $+125\text{ [°C]}$.

Table 1-5 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	3.00	3.30	3.60	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.65	1.80	1.95	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{fa}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-6 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	3.00	3.30	3.60	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.40	1.50	1.60	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{ra}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-7 Electrical Characteristics(HV_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input Leakage Current	I _{LI}	—	-5	—	5	μA	
Off State Leakage Current	I _{OZ}	—	-5	—	5	μA	
High Level Output Voltage	V _{OH}	I _{OH} = -2 mA (Type 1), -4 mA (Type 2) -8 mA (Type 3), -12 mA (Type 4) HV _{DD} = Min.	HV _{DD} -0.4	—	—	V	
Low Level Output Voltage	V _{OL}	I _{OL} = 2 mA (Type 1), 4 mA (Type 2) 8 mA (Type 3), 12 mA (Type 4) HV _{DD} = Min.	—	—	0.4	V	
High Level Input Voltage	V _{IH1}	LVC MOS Level, HV _{DD} = Max.	2.2	—	—	V	
Low Level Input Voltage	V _{IL1}	LVC MOS Level, HV _{DD} = Min.	—	—	0.8	V	
High Level Input Voltage	V _{T1+}	LVC MOS Schmitt	1.4	—	2.7	V	
Low Level Input Voltage	V _{T1-}	LVC MOS Schmitt	0.6	—	1.8	V	
Hysteresis Voltage	V _{H1}	LVC MOS Schmitt	0.3	—	—	V	
High Level Input Voltage	V _{IH2}	LVTTL Level, HV _{DD} = Max	2.0	—	—	V	
Low Level Input Voltage	V _{IL2}	LVTTL Level, HV _{DD} = Min	—	—	0.8	V	
High Level Input Voltage	V _{IH3}	PCI Level, HV _{DD} = Max	1.8	—	—	V	
Low Level Input Voltage	V _{IL3}	PCI Level, HV _{DD} = Min	—	—	0.9	V	
Pull-up Resistance	P _{PU}	V _I = 0 V	Type 1	25	50	120	kΩ
		Type 2	50	100	240	kΩ	
Pull-down Resistance	P _{PD}	V _I = HV _{DD}	Type 1	25	50	120	kΩ
			Type 2	50	100	240	kΩ
High Level Output Current ^{*1}	I _{OH3}	PCI Response	V _{OH} = 0.90 V, HV _{DD} = Min.	-36	—	—	mA
			V _{OH} = 2.52 V, HV _{DD} = Max.	—	—	-115	
Low Level Output Current ^{*1}	I _{OL3}	PCI Response	V _{OL} = 1.80 V, HV _{DD} = Min.	48	—	—	mA
			V _{OL} = 0.65 V, HV _{DD} = Max.	—	—	137	
High Level Maintenance Current	I _{BHH}	Bus Hold Response	V _{IN} = 2.0 V HV _{DD} = Min.	—	—	-20	μA
Low Level Maintenance Current	I _{BHL}	Bus Hold Response	V _{IN} = 0.8 V HV _{DD} = Min.	—	—	17	μA
High Level Reversal Current	I _{BHHO}	Bus Hold Response	V _{IN} = 0.8 V HV _{DD} = Max.	-350	—	—	μA
Low Level Reversal Current	I _{BHLO}	Bus Hold Response	V _{IN} = 2.0 V HV _{DD} = Max.	300	—	—	μA
Input Terminal Capacitance	C _I	f = 1 MHz, HV _{DD} = 0 V	—	—	8	pF	
Output Terminal Capacitance	C _O	f = 1 MHz, HV _{DD} = 0 V	—	—	8	pF	
Input/Output Terminal Capacitance	C _{IO}	f = 1 MHz, HV _{DD} = 0 V	—	—	8	pF	

Notes *1: Compliant with PCI Standard Rev. 2.2

Table 1-8 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	2.30	2.50	2.70	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.65	1.80	1.95	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{ra}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-9 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	2.30	2.50	2.70	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.40	1.50	1.60	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{ra}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 3.6 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 3.6 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-10 Electrical Characteristics(HV_{DD} = 2.5 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I _{LI}	—		-5	—	5	μA
Off State Leakage Current	I _{OZ}	—		-5	—	5	μA
High Level Output Voltage	V _{OH}	I _{OH} = -1.5 mA (Type 1), -3 mA (Type 2) -6 mA (Type 3), -9 mA (Type 4) HV _{DD} = Min.		HV _{DD} -0.4	—	—	V
Low Level Output Voltage	V _{OL}	I _{OL} = 1.5 mA (Type 1), 3 mA (Type 2) 6 mA (Type 3), 9 mA (Type 4) HV _{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V _{IH1}	LVCMOS Level, HV _{DD} = Max.		1.7	—	—	V
Low Level Input Voltage	V _{IL1}	LVCMOS Level, HV _{DD} = Min.		—	—	0.7	V
High Level Input Voltage	V _{T1+}	LVCMOS Schmitt		0.8	—	1.9	V
Low Level Input Voltage	V _{T1-}	LVCMOS Schmitt		0.5	—	1.3	V
Hysteresis Voltage	V _{H1}	LVCMOS Schmitt		0.1	—	—	V
Pull-up Resistance	P _{PU}	V _I = 0 V	Type 1	35	70	175	kΩ
			Type 2	70	140	350	kΩ
Pull-down Resistance	P _{PD}	V _I = HV _{DD}	Type 1	35	70	175	kΩ
			Type 2	70	140	350	kΩ
High Level Maintenance Current	I _{BHH}	Bus Hold Response	V _{IN} = 1.7 V HV _{DD} = Min.	—	—	-5	μA
Low Level Maintenance Current	I _{BHL}	Bus Hold Response	V _{IN} = 0.7 V HV _{DD} = Min.	—	—	5	μA
High Level Reversal Current	I _{BHHO}	Bus Hold Response	V _{IN} = 0.7 V HV _{DD} = Max.	-280	—	—	μA
Low Level Reversal Current	I _{BHLO}	Bus Hold Response	V _{IN} = 1.7 V HV _{DD} = Max.	240	—	—	μA
Input Terminal Capacitance	C _I	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF
Output Terminal Capacitance	C _O	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF
Input/Output Terminal Capacitance	C _{IO}	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF

Table 1-11 Electrical Characteristics $(V_{DD}$ or LV_{DD} = 1.8 V \pm 0.15 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input Leakage Current	I_{LI}	—	-5	—	5	μ A	
Off State Leakage Current	I_{OZ}	—	-5	—	5	μ A	
High Level Output Voltage	V_{OH}	I_{OH} = -1 mA (Type 1), -2 mA (Type 2) -4 mA (Type 3), -6 mA (Type 4) V_{DD} = Min.	V_{DD} -0.4	—	—	V	
Low Level Output Voltage	V_{OL}	I_{OL} = 1 mA (Type 1), 2 mA (Type 2) 4 mA (Type 3), 6 mA (Type 4) V_{DD} = Min.	—	—	0.4	V	
High Level Input Voltage	V_{IH1}	LVC MOS Level, V_{DD} = Max.	1.27	—	—	V	
Low Level Input Voltage	V_{IL1}	LVC MOS Level, V_{DD} = Min.	—	—	0.57	V	
High Level Input Voltage	V_{T1+}	LVC MOS Schmitt	0.6	—	1.4	V	
Low Level Input Voltage	V_{T1-}	LVC MOS Schmitt	0.3	—	1.1	V	
Hysteresis Voltage	V_{H1}	LVC MOS Schmitt	0.02	—	—	V	
Pull-up Resistance	P_{PU}	V_I = 0 V	Type 1	24	60	150	k Ω
			Type 2	48	120	300	k Ω
Pull-down Resistance	P_{PD}	V_I = V_{DD} or LV_{DD}	Type 1	24	60	150	k Ω
			Type 2	48	120	300	k Ω
High Level Maintenance Current	I_{BHH}	Bus Hold Response V_{IN} = 1.27 V V_{DD} = Min.	—	—	-2	μ A	
Low Level Maintenance Current	I_{BHL}	Bus Hold Response V_{IN} = 0.57 V V_{DD} = Min.	—	—	2	μ A	
High Level Reversal Current	I_{BHHO}	Bus Hold Response V_{IN} = 0.57 V V_{DD} = Max.	-100	—	—	μ A	
Low Level Reversal Current	I_{BHLO}	Bus Hold Response V_{IN} = 1.27 V V_{DD} = Max.	100	—	—	μ A	
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	

Table 1-12 Electrical Characteristics $(V_{DD}$ or $LV_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input Leakage Current	I_{LI}	—	-5	—	5	μA	
Off State Leakage Current	I_{OZ}	—	-5	—	5	μA	
High Level Output Voltage	V_{OH}	$I_{OH} = -0.75 \text{ mA}$ (Type 1), -1.5 mA (Type 2) -3 mA (Type 3), -4.5 mA (Type 4) $V_{DD} = \text{Min.}$	V_{DD} -0.4	—	—	V	
Low Level Output Voltage	V_{OL}	$I_{OL} = 0.75 \text{ mA}$ (Type 1), 1.5 mA (Type 2) 3 mA (Type 3), 4.5 mA (Type 4) $V_{DD} = \text{Min.}$	—	—	0.4	V	
High Level Input Voltage	V_{IH1}	LVC MOS Level, $V_{DD} = \text{Max.}$	1.04	—	—	V	
Low Level Input Voltage	V_{IL1}	LVC MOS Level, $V_{DD} = \text{Min.}$	—	—	0.49	V	
High Level Input Voltage	V_{T1+}	LVC MOS Schmitt	0.5	—	1.1	V	
Low Level Input Voltage	V_{T1-}	LVC MOS Schmitt	0.2	—	1.0	V	
Hysteresis Voltage	V_{H1}	LVC MOS Schmitt	0.01	—	—	V	
Pull-up Resistance	P_{PU}	$V_I = 0 \text{ V}$	Type 1	36	90	234	$\text{k}\Omega$
			Type 2	72	180	468	$\text{k}\Omega$
Pull-down Resistance	P_{PD}	$V_I = V_{DD}$ or LV_{DD}	Type 1	36	90	234	$\text{k}\Omega$
			Type 2	72	180	468	$\text{k}\Omega$
High Level Maintenance Current	I_{BHH}	Bus Hold Response $V_{IN} = 1.04 \text{ V}$ $V_{DD} = \text{Min.}$	—	—	-2	μA	
Low Level Maintenance Current	I_{BHL}	Bus Hold Response $V_{IN} = 0.49 \text{ V}$ $V_{DD} = \text{Min.}$	—	—	2	μA	
High Level Reversal Current	I_{BHHO}	Bus Hold Response $V_{IN} = 0.49 \text{ V}$ $V_{DD} = \text{Max.}$	-80	—	—	μA	
Low Level Reversal Current	I_{BHLO}	Bus Hold Response $V_{IN} = 1.04 \text{ V}$ $V_{DD} = \text{Max.}$	80	—	—	μA	
Input Terminal Capacitance	C_I	$f = 1 \text{ MHz}$, $V_{DD} = 0 \text{ V}$	—	—	8	pF	
Output Terminal Capacitance	C_O	$f = 1 \text{ MHz}$, $V_{DD} = 0 \text{ V}$	—	—	8	pF	
Input/Output Terminal Capacitance	C_{IO}	$f = 1 \text{ MHz}$, $V_{DD} = 0 \text{ V}$	—	—	8	pF	

1.2.2 When Using 2.5-V Input/Output Buffers (X Type)

Table 1-13 Absolute Maximum Ratings (for a Single Power Supply)

($V_{SS} = 0$ [V])

Parameter	Symbol	Limits	Unit
Power-Supply Voltage	V_{DD}	-0.3 to +2.5	V
Input Voltage	V_I	-0.3 to $V_{DD} + 0.5^{*1}$	V
Output Voltage	V_O	-0.3 to $V_{DD} + 0.5^{*1}$	V
Output Current/Pin	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +3.0 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

Table 1-14 Absolute Maximum Ratings (for Dual Power Supplies)

($V_{SS} = 0$ [V])

Parameter	Symbol	Limits	Unit
Power-Supply Voltage	HV_{DD}^{*3}	-0.3 to +3.0	V
	LV_{DD}^{*3}	-0.3 to +2.5	V
Input Voltage	HV_I	-0.3 to $HV_{DD} + 0.5^{*1}$	V
	LV_I	-0.3 to $LV_{DD} + 0.5^{*2}$	V
Output Voltage	HV_O	-0.3 to $HV_{DD} + 0.5^{*1}$	V
	LV_O	-0.3 to $LV_{DD} + 0.5^{*2}$	V
Output Current/Pin	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	-65 to +150	°C

Notes *1: Possible to use -0.3 V to +3.0 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use -0.3 V to +3.0 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: $HV_{DD} \geq LV_{DD}$

Table 1-15 Recommended Operating Conditions (for a Single Power Supply at $V_{DD} = 1.8\text{ V}$) $(V_{SS} = 0\text{ [V]})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage	V_{DD}	1.65	1.80	1.95	V
Input Voltage	V_I	V_{SS}	—	V_{DD}^{*1}	V
Ambient Temperature	T_a	0 -40	25 25	70^{*2} 85^{*3}	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

Notes *1: Possible to use up to 2.7 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*2: The ambient temperature range is recommended for $T_j = 0$ to $+85[^\circ\text{C}]$.

*3: The ambient temperature range is recommended for $T_j = -40$ to $+125[^\circ\text{C}]$.

Table 1-16 Recommended Operating Conditions (for a Single Power Supply at $V_{DD} = 1.5\text{ V}$) $(V_{SS} = 0\text{ [V]})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage	V_{DD}	1.40	1.50	1.60	V
Input Voltage	V_I	V_{SS}	—	V_{DD}^{*1}	V
Ambient Temperature	T_a	0 -40	25 25	70^{*2} 85^{*3}	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

Notes *1: Possible to use up to 2.7 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*2: The ambient temperature range is recommended for $T_j = 0$ to $+85[^\circ\text{C}]$.

*3: The ambient temperature range is recommended for $T_j = -40$ to $+125[^\circ\text{C}]$.

Table 1-17 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	2.30	2.50	2.70	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.65	1.80	1.95	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{fa}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 2.7 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 2.7 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-18 Recommended Operating Conditions (for Dual Power Supplies)(V_{SS} = 0 [V])

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV _{DD}	2.30	2.50	2.70	V
Power-Supply Voltage (Low Voltage)	LV _{DD}	1.40	1.50	1.60	V
Input Voltage	HV _I	V _{SS}	—	HV _{DD} ^{*1}	V
	LV _I	V _{SS}	—	LV _{DD} ^{*2}	V
Ambient Temperature	T _a	0	25	70 ^{*3}	°C
		-40	25	85 ^{*4}	
Normal Input Rising Time	t _{ri}	—	—	50	ns
Normal Input Falling Time	t _{ra}	—	—	50	ns
Schmitt Input Rising Time	t _{ri}	—	—	5	ms
Schmitt Input Falling Time	t _{ra}	—	—	5	ms

Notes *1: Possible to use up to 2.7 V of N channel open drain bi-directional buffers and input buffers.

*2: Possible to use up to 2.7 V of N channel open drain bi-directional buffers, input buffers, and Fail Safe cells.

*3: The ambient temperature range is recommended for T_j = 0 to +85[°C].

*4: The ambient temperature range is recommended for T_j = -40 to +125[°C].

Table 1-19 Electrical Characteristics(HV_{DD} = 2.5 V ± 0.2 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I _{LI}	—		-5	—	5	μA
Off State Leakage Current	I _{OZ}	—		-5	—	5	μA
High Level Output Voltage	V _{OH}	I _{OH} = -2 mA (Type 1), -4 mA (Type 2) -8 mA (Type 3), -12 mA (Type 4) HV _{DD} = Min.		HV _{DD} -0.4	—	—	V
Low Level Output Voltage	V _{OL}	I _{OL} = 2 mA (Type 1), 4 mA (Type 2) 8 mA (Type 3), 12 mA (Type 4) HV _{DD} = Min.		—	—	0.4	V
High Level Input Voltage	V _{IH1}	LVCMOS Level, V _{DD} = Max.		1.7	—	—	V
Low Level Input Voltage	V _{IL1}	LVCMOS Level, V _{DD} = Min.		—	—	0.7	V
High Level Input Voltage	V _{T1+}	LVCMOS Schmitt		0.8	—	1.9	V
Low Level Input Voltage	V _{T1-}	LVCMOS Schmitt		0.5	—	1.3	V
Hysteresis Voltage	V _{H1}	LVCMOS Schmitt		0.1	—	—	V
Pull-up Resistance	P _{PU}	V _I = 0 V	Type 1	25	50	125	kΩ
			Type 2	50	100	250	kΩ
Pull-down Resistance	P _{PD}	V _I = V _{DD} or LV _{DD}	Type 1	25	50	125	kΩ
			Type 2	50	100	250	kΩ
High Level Maintenance Current	I _{BHH}	Bus Hold Response	V _{IN} = 1.7 V HV _{DD} = Min.	—	—	-5	μA
Low Level Maintenance Current	I _{BHL}	Bus Hold Response	V _{IN} = 0.7 V HV _{DD} = Min.	—	—	5	μA
High Level Reversal Current	I _{BHHO}	Bus Hold Response	V _{IN} = 0.7 V HV _{DD} = Max.	-280	—	—	μA
Low Level Reversal Current	I _{BHLO}	Bus Hold Response	V _{IN} = 1.7 V HV _{DD} = Max.	240	—	—	μA
Input Terminal Capacitance	C _I	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF
Output Terminal Capacitance	C _O	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF
Input/Output Terminal Capacitance	C _{IO}	f = 1 MHz, HV _{DD} = 0 V		—	—	8	pF

Table 1-20 Electrical Characteristics $(V_{DD}$ or $LV_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input Leakage Current	I_{LI}	—	-5	—	5	μA	
Off State Leakage Current	I_{OZ}	—	-5	—	5	μA	
High Level Output Voltage	V_{OH}	$I_{OH} = -1.5\text{ mA}$ (Type 1), -3 mA (Type 2) -6 mA (Type 3), -9 mA (Type 4) $V_{DD} = \text{Min.}$	V_{DD} -0.4	—	—	V	
Low Level Output Voltage	V_{OL}	$I_{OL} = 1.5\text{ mA}$ (Type 1), 3 mA (Type 2) 6 mA (Type 3), 9 mA (Type 4) $V_{DD} = \text{Min.}$	—	—	0.4	V	
High Level Input Voltage	V_{IH1}	LVC MOS Level, $V_{DD} = \text{Max.}$	1.27	—	—	V	
Low Level Input Voltage	V_{IL1}	LVC MOS Level, $V_{DD} = \text{Min.}$	—	—	0.57	V	
High Level Input Voltage	V_{T1+}	LVC MOS Schmitt	0.6	—	1.4	V	
Low Level Input Voltage	V_{T1-}	LVC MOS Schmitt	0.3	—	1.1	V	
Hysteresis Voltage	V_{H1}	LVC MOS Schmitt	0.02	—	—	V	
Pull-up Resistance	P_{PU}	$V_I = 0\text{ V}$	Type 1	18	45	122	$\text{k}\Omega$
			Type 2	36	90	243	$\text{k}\Omega$
Pull-down Resistance	P_{PD}	$V_I = V_{DD}$ or LV_{DD}	Type 1	18	45	122	$\text{k}\Omega$
			Type 2	36	90	243	$\text{k}\Omega$
High Level Maintenance Current	I_{BHH}	Bus Hold Response $V_{IN} = 1.27\text{ V}$ $V_{DD} = \text{Min.}$	—	—	-2	μA	
Low Level Maintenance Current	I_{BHL}	Bus Hold Response $V_{IN} = 0.57\text{ V}$ $V_{DD} = \text{Min.}$	—	—	2	μA	
High Level Reversal Current	I_{BHHO}	Bus Hold Response $V_{IN} = 0.57\text{ V}$ $V_{DD} = \text{Max.}$	-100	—	—	μA	
Low Level Reversal Current	I_{BHLO}	Bus Hold Response $V_{IN} = 1.27\text{ V}$ $V_{DD} = \text{Max.}$	100	—	—	μA	
Input Terminal Capacitance	C_I	$f = 1\text{ MHz}$, $V_{DD} = 0\text{ V}$	—	—	8	pF	
Output Terminal Capacitance	C_O	$f = 1\text{ MHz}$, $V_{DD} = 0\text{ V}$	—	—	8	pF	
Input/Output Terminal Capacitance	C_{IO}	$f = 1\text{ MHz}$, $V_{DD} = 0\text{ V}$	—	—	8	pF	

Table 1-21 Electrical Characteristics $(V_{DD}$ or LV_{DD} = 1.5 V \pm 0.1 V, V_{SS} = 0 V, T_a = -40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input Leakage Current	I_{LI}	—	-5	—	5	μ A	
Off State Leakage Current	I_{OZ}	—	-5	—	5	μ A	
High Level Output Voltage	V_{OH}	I_{OH} = -1 mA (Type 1), -2 mA (Type 2) -4 mA (Type 3), -6 mA (Type 4) V_{DD} = Min.	V_{DD} -0.4	—	—	V	
Low Level Output Voltage	V_{OL}	I_{OL} = 1 mA (Type 1), 2 mA (Type 2) 4 mA (Type 3), 6 mA (Type 4) V_{DD} = Min.	—	—	0.4	V	
High Level Input Voltage	V_{IH1}	LVC MOS Level, V_{DD} = Max.	1.04	—	—	V	
Low Level Input Voltage	V_{IL1}	LVC MOS Level, V_{DD} = Min.	—	—	0.49	V	
High Level Input Voltage	V_{T1+}	LVC MOS Schmitt	0.5	—	1.1	V	
Low Level Input Voltage	V_{T1-}	LVC MOS Schmitt	0.2	—	1.0	V	
Hysteresis Voltage	V_{H1}	LVC MOS Schmitt	0.01	—	—	V	
Pull-up Resistance	P_{PU}	V_I = 0 V	Type 1	28	70	210	k Ω
			Type 2	56	140	420	k Ω
Pull-down Resistance	P_{PD}	V_I = V_{DD} or LV_{DD}	Type 1	28	70	210	k Ω
			Type 2	56	140	420	k Ω
High Level Maintenance Current	I_{BHH}	Bus Hold Response V_{IN} = 1.04 V V_{DD} = Min.	—	—	-2	μ A	
Low Level Maintenance Current	I_{BHL}	Bus Hold Response V_{IN} = 0.49 V V_{DD} = Min.	—	—	2	μ A	
High Level Reversal Current	I_{BHHO}	Bus Hold Response V_{IN} = 0.49 V V_{DD} = Max.	-80	—	—	μ A	
Low Level Reversal Current	I_{BHLO}	Bus Hold Response V_{IN} = 1.04 V V_{DD} = Max.	80	—	—	μ A	
Input Terminal Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	
Output Terminal Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	
Input/Output Terminal Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V	—	—	8	pF	

1.3 Estimating the Quiescent Current

The quiescent current for cells in the S1K/S1X70000 series can be roughly estimated using the equation shown below. When calculating the quiescent current, please assume ambient temperature (T_a) = chip temperature (T_j).

The quiescent current depends on the off current of each transistor. Because the quiescent current for the entire chip cannot easily be calculated simultaneously, divide the chip into several blocks in the calculation of the quiescent current, and use the sum total of all blocks as the chip's quiescent current.

$$I_{\text{DSS}} (T_j = 85^\circ\text{C}) = I_{\text{QBC}} + I_{\text{QBM}} + I_{\text{QCM}} + I_{\text{QIO}}$$

1.3.1 Quiescent Current in the Random Logic Part (I_{QBC})

The S1K/S1X70000 series is available in two types of MSI cells: Basic Cell-type MSI cells, which are equivalent to the conventional gate-array type, and Cell Based-type MSI cells. The quiescent current is calculated differently for each type of MSI cell. Table 1-22 lists the quiescent-current values per 1k gate of each MSI cell type.

Table 1-22 Quiescent Current per 1k Gate

($V_{\text{DD}} = 1.95 \text{ V}$, $T_j = 85^\circ\text{C}$)

	Standard 1	Standard 2	High-Performance	Low-Leakage	Unit
Basic Cell Type S1X70000	1.59×10^{-6}	5.85×10^{-5}	1.22×10^{-3}	TBD	A
Cell-Based Type S1K70000	9.62×10^{-7}	3.21×10^{-5}	6.82×10^{-4}	TBD	A

1.3.2 Quiescent Current of Basic Cell-Type RAM (I_{QBM})

The quiescent-current values of the primary Basic Cell-type RAMs in the S1X70000 series are listed in Table 1-23.

(For the quiescent-current values of RAMs not listed here, use the quiescent-current value of the RAM that is closest in structure to those RAMs. If more detailed information on quiescent-current values is required, please contact the sales division of Epson.)

Table 1-23 Quiescent-Current Values of Basic Cell-Type RAM for Each Transistor Type
(Common to 1-port RAM and 2-Port RAM, $V_{DD} = 1.95\text{ V}$, $T_j = 85^\circ\text{C}$)

Standard 1

	64Word	128Word	192Word	256Word	Unit
8 Bit	3.47×10^{-6}	6.08×10^{-6}	8.70×10^{-6}	11.31×10^{-6}	A
16 Bit	5.22×10^{-6}	9.19×10^{-6}	13.16×10^{-6}	17.13×10^{-6}	A
24 Bit	6.96×10^{-6}	12.29×10^{-6}	17.63×10^{-6}	22.96×10^{-6}	A
32 Bit	8.71×10^{-6}	15.40×10^{-6}	22.09×10^{-6}	28.79×10^{-6}	A

High-Performance

	64Word	128Word	192Word	256Word	Unit
8 Bit	2.79×10^{-3}	4.92×10^{-3}	7.05×10^{-3}	9.18×10^{-3}	A
16 Bit	4.25×10^{-3}	7.55×10^{-3}	10.85×10^{-3}	14.15×10^{-3}	A
24 Bit	5.72×10^{-3}	10.19×10^{-3}	14.66×10^{-3}	19.13×10^{-3}	A
32 Bit	7.18×10^{-3}	12.82×10^{-3}	18.46×10^{-3}	24.10×10^{-3}	A

Low-Leakage

	64Word	128Word	192Word	256Word	Unit
8 Bit	TBD	TBD	TBD	TBD	A
16 Bit	TBD	TBD	TBD	TBD	A
24 Bit	TBD	TBD	TBD	TBD	A
32 Bit	TBD	TBD	TBD	TBD	A

1.3.3 Quiescent Current of Cell Based-Type RAM (I_{QCM})

The quiescent-current values of the Cell Based-type RAMs and ROMs in the S1K70000 series vary depending on the word/bit structure. Therefore, please contact the sales division of Epson for details.

1.3.4 Quiescent Current of Input/Output Buffers (I_{QIO})

The quiescent-current values flowing in input/output buffers can be roughly estimated by using the values listed in Table 1-24 for the calculation formula shown on the next page.

(Make sure the input signals for the input and bi-directional buffers are fixed to V_{SS} or V_{DD} (LV_{DD} or HV_{DD}). If buffers with pull-up and pull-down resistors have been selected, leave the pins open.)

For systems with dual power supplies, calculate the quiescent current for the H- and L-voltage buffers separately.

Table 1-24 Quiescent-Current Value per Input/Output Buffer ($T_j = 85^\circ \text{C}$)

	Quiescent-Current Value	Unit
$V_{DD} = 3.60 \text{ V}$	450×10^{-9}	A
$V_{DD} = 2.70 \text{ V}$	105×10^{-9}	A
$V_{DD} = 1.95 \text{ V}$	75×10^{-9}	A
$V_{DD} = 1.60 \text{ V}$	75×10^{-9}	A

Quiescent-current value of input / output buffer = (values in Table 1-24)
 x (number of output cells + number of bi-directional cells
 + number of V_{DD} (HV_{DD} or LV_{DD}) power-supply cells)

Calculation example:

Find the quiescent-current value for the following case.

- Power-supply voltage : $HV_{DD} / LV_{DD} = 3.3 \text{ V} / 1.8 \text{ V}$
- Type of transistor used : Standard 1
- I/O cells
 - V_{SS} : 12
 - HV_{DD} : 12
 - LV_{DD} : 12
 - H-voltage input cells : 30
 - H-voltage output cells : 40
 - H-voltage bi-directional cells : 60
 - L-voltage input cells : 30
 - L-voltage output cells : 20
 - L-voltage bi-directional cells : 40
- Basic Cell-type 2-port RAM : 256 words x 16 bits, 4 pcs.
128 words x 8 bits, 6 pcs.
- Cell-Based Logic : 1240k gates

Because this is a dual-power-supply system, first find the quiescent current for the LV_{DD} system. From Table 1-22, the quiescent-current value of the Cell-Based Logic is

$$I_{QBC} = 9.62 \times 10^{-7} \times 1240 = 1192.9 \times 10^{-6} \text{ [A]} \quad (V_{DD} = 1.95 \text{ V}, T_j = 85^\circ \text{C})$$

Next, find the quiescent-current value of the Basic Cell-type RAMs. From Table 1-23, the quiescent-current value per piece of RAM is

$$256 \text{ Word} \times 16 \text{ Bit} \cdots 17.13 \times 10^{-6} \text{ [A]}$$

$$128 \text{ Word} \times 8 \text{ Bit} \cdots 6.08 \times 10^{-6} \text{ [A]}$$

Therefore, the quiescent-current value of the Basic Cell-type RAMs is

$$\begin{aligned} I_{QBM} &= (17.13 \times 10^{-6} \times 4) + (6.08 \times 10^{-6} \times 6) \\ &= 68.52 \times 10^{-6} + 36.48 \times 10^{-6} \\ &= 105.0 \times 10^{-6} \text{ [A]} \quad (V_{DD} = 1.95 \text{ V}, T_j = 85^\circ \text{C}) \end{aligned}$$

Next, find the quiescent-current value of the input/output buffers using the equation for quiescent-current values shown above.

$$I_{QIO} = 75 \times 10^{-9} \times (20 + 40 + 12) = 5.40 \times 10^{-6} \text{ [A]}$$

From the quiescent-current values obtained thus far, find the quiescent-current value of the LV_{DD} system.

$$\begin{aligned} I_Q (\text{LV}_{\text{DD}}) &= I_{\text{QBC}} + I_{\text{QBM}} + I_{\text{QIO}} \\ &= 1192.9 \times 10^{-6} + 105.0 \times 10^{-6} + 5.4 \times 10^{-6} \\ &= 1303.3 \times 10^{-6} \text{ [A]} \end{aligned}$$

Next, find the quiescent-current value of the HV_{DD} system. To find the quiescent-current value of the HV_{DD} system, simply calculate the quiescent current flowing in the input/output buffers.

$$I_Q (\text{HV}_{\text{DD}}) = 450 \times 10^{-9} \times (40 + 60 + 12) = 50.40 \times 10^{-6} \text{ [A]}$$

From the above calculation results, the quiescent-current values to be obtained in this example are

$$I_Q (\text{LV}_{\text{DD}}) = 1303.3 \times 10^{-6} \text{ [A]}$$

$$I_Q (\text{HV}_{\text{DD}}) = 50.40 \times 10^{-6} \text{ [A]}$$

1.3.5 Temperature Characteristics of Quiescent Current

The quiescent-current values at temperatures other than $T_j = 85[^\circ\text{C}]$ can be approximately calculated using the equation shown below.

$$I_{\text{DDS}} (T_j) = I_{\text{DDS}} (T_j = 85^\circ\text{C}) \times 0.0317e^{(0.0406 \times T_j)}$$

(where, $T_j = 0$ to 125°C)

Calculation example:

In cases in which the quiescent-current value at $T_j = 85[^\circ\text{C}]$ is $3000 \text{ } [\mu\text{A}]$, the approximate value of the quiescent current at $T_j = 50[^\circ\text{C}]$ is

$$\begin{aligned} I_{\text{DDS}} (T_j = 50^\circ\text{C}) &= I_{\text{DDS}} (T_j = 85^\circ\text{C}) \times 0.0317e^{(0.0406 \times 50)} \\ &= 3000 \times 0.24 \\ &= 720 \text{ } [\mu\text{A}] \end{aligned}$$

1.4 Product Development Flow

The standard cells and embedded arrays are developed jointly by customers and Epson. Customers perform work based on the cell libraries and various design materials supplied by Epson. This work includes system design, circuit design, and pattern design.

Before these designs can be interfaced to Epson, customers are requested to check them based on the data-release checklist included herein. After completion of that check, the necessary data and documentation may be presented to Epson.

Customers conduct simulations of said designs using EDA software or Auklet* available on hand, and Epson undertakes subsequent work following placement and routing.

Note *: Auklet is an ASIC design assistance system from Epson that can be run on an MS-Windows 95/98 or NT platform.

Currently, the following types of EDA software can be used for simulation:

- Verilog-XL^(*1)
- VSS^(*2)
- ModelSim^(*3)

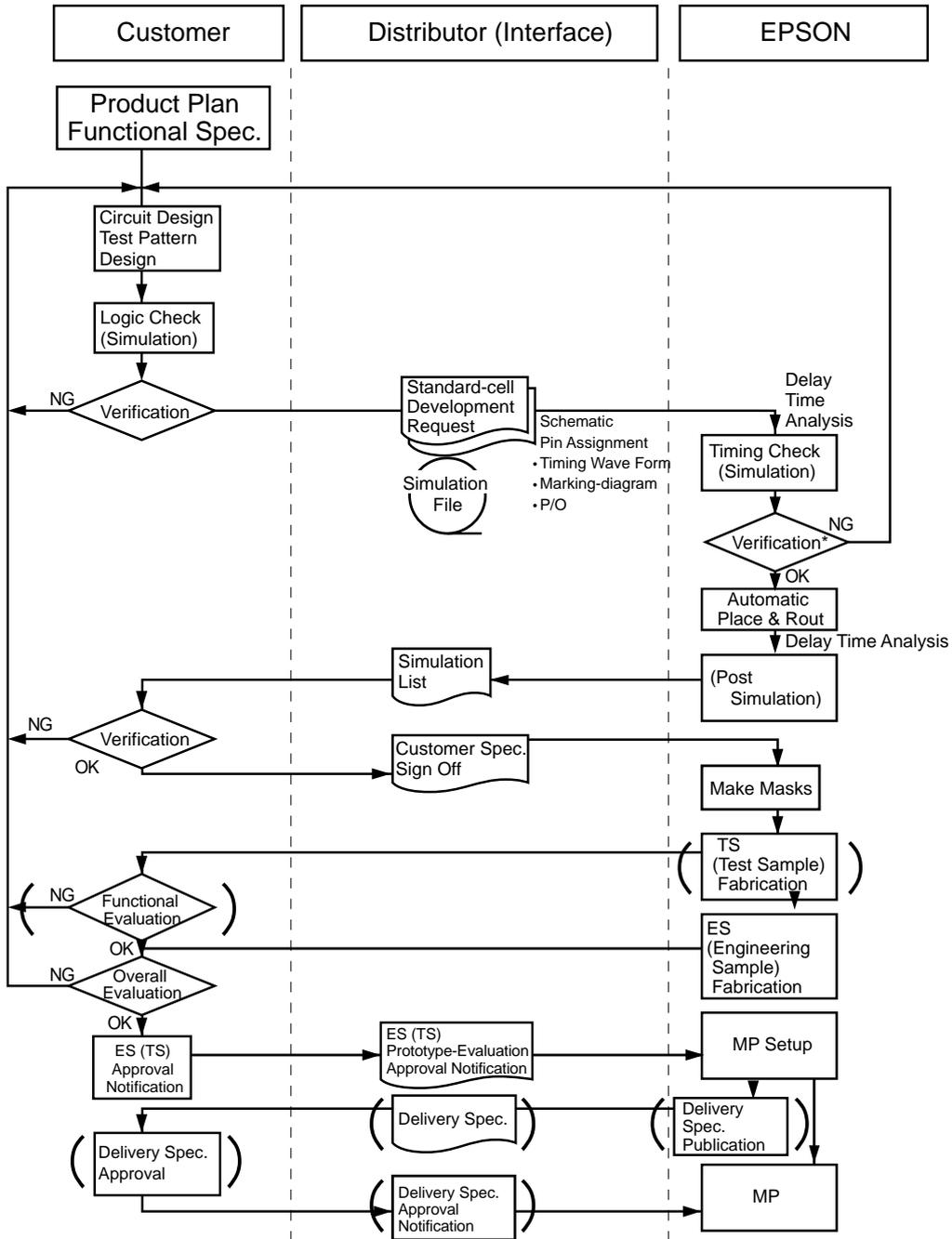
Note *1: Verilog-XL is a registered trademark of Cadence Design Systems Corporation, USA.

*2: VSS is a registered trademark of Synopsys of Inc., USA.

*3: ModelSim is a registered trademark of Model Technology Corp., USA.

For more information, please contact the sales division of Epson.

The process flow of the standard-cell / embedded-array development process is shown below.



Chapter 2 Estimating the Gate Density

This chapter describes the procedure for estimating the circuit size after cutting out circuits from the customer's system, and then estimating an approximate bulk size. The precautions to be taken when performing this work are also described.

2.1 Dividing Up Logic Between Chips

When cutting out circuits from the customer's system, care must be taken with respect to the following points.

- Precautions to be taken
 - (1) Logic size to be integrated (Gate count)
 - (2) Number of I/O pins required (Pin count)
 - (3) Package to be used
 - (4) Power consumption

Generally speaking, as the circuit size increases, so does the power consumption of the circuit and the number of input/output pins on it. If the circuit size is significantly large, the circuit may be divided into multiple chips rather than being integrated into a single chip. This helps reduce the total cost and the power consumption of the circuit.

2.2 Determining Gate Size

The number of gates used in the S1K/S1X70000-series MSI cells may be estimated from the number of pads or from the size of the circuit implemented.

2.2.1 Estimating Bulk from the Number of Pads

Table 2-1 lists the primary bulks in the S1K/S1X70000 series with respect to the number of pads.

Table 2-1 Typical Pad Counts and Total BC Counts

	Basic Cell Type			Cell Based Type ^{*2}			PAD Count ^{*1} (four sides)
	Total BC Count	X	Y	Total BC Count	X	Y	
A	150894	747	202	205808	677	304	88
B	190836	837	228	258060	759	340	100
C	306144	1063	288	416016	963	432	128
D	390222	1197	326	529480	1085	488	144
E	466004	1309	356	633858	1187	534	160
F	569330	1445	394	773490	1311	590	176
G	623356	1513	412	844536	1371	616	184
H	778780	1693	460	1059150	1535	690	208
I	845280	1761	480	1146646	1597	718	216
J	1174450	2075	566	1593018	1883	846	256
H	1647530	2459	670	2233458	2229	1002	304
L	2164992	2819	768	2940550	2557	1150	352
M	2638128	3111	848	3582670	2821	1270	388
N	3076844	3559	916	4174390	3047	1370	420
O	3498960	3585	976	4752962	3251	1462	448
P	4001652	3833	1044	5434900	3475	1564	480
Q	4487042	4057	1106	6092424	3679	1656	508
R	4897972	4237	1156	6640704	3843	1728	532
S	5373610	4441	1210	7296924	4027	1812	556

Notes *1: For pin counts less than 88, the number of pads is omitted.

*2: In the "S1K70000-/S1X70000-Series MSI Cell Library", the size of each Cell Based-type cell is expressed in grid units. Cell sizes in grid units may be converted into BC counts at a rate of 1 BC = 3.0 grids.

2.2.2 Estimating the Number of Gates Used in Basic Cell-Type MSI Cell

Before the number of gates used in the S1K/S1X70000-series Basic Cell-type MSI cell can be estimated, the following pieces of information must be available.

- Circuit size : G_0 (gate or BC)
- Maximum operating frequency in the circuit : f (MHz)
- Percentage of circuit operating at f MHz : α (%)
- Number of metalizations used : M

The rules for reinforced power supplies are determined from the above information (depending on the width of the reinforced power-supply line, one of two sets of rules applies). Because no logic circuits can be placed below reinforced power supplies, the area required for reinforced power supplies must be added to the above circuit size, G_0 gates. Here, the necessary BC count, G_A , where reinforced power supplies are considered, is defined as

$$G_A = G_0 + (\text{area required for the reinforced power supply}) \dots (1)$$

Further, the following is defined.

$$G_0 / G_A = \beta \text{ (\% Effective gate rate)} \dots (2)$$

The effective gate rates are summarized in Tables 2-2 and 2-3.

Table 2-2 Effective Gate Rates (1 BC)

(%)

Metalization Layers	Circuit Percentage	Operating Frequency (MHz)						
		50	75	100	125	150	175	200
AL3 layered	40%	89.4	87.7	84.6	—	—	—	—
	60%	88.3	85.6	80.2	—	—	—	—
	80%	87.1	83.3	—	—	—	—	—
AL4 or 5 layered	40%	90.9	90.3	89.8	89.3	88.7	88.0	87.5
	60%	90.4	89.7	88.9	88.0	87.1	86.3	85.1
	80%	90.0	89.0	87.9	86.8	85.6	84.0	83.3
	100%	89.6	88.3	86.8	85.6	84.0	82.5	80.2
AL6 layered	40%	91.2	90.9	90.6	90.3	90.0	89.7	89.3
	60%	90.9	90.5	90.0	89.6	89.1	88.6	88.1
	80%	90.7	90.1	89.5	88.9	88.3	87.7	86.8
	100%	90.4	89.7	89.0	88.1	87.3	86.6	85.6

Note: Combinations left blank in the above table are not available.

Table 2-3 Effective Gate Rates (2 BCs)

(%)

Metalization Layers	Circuit Percentage	Operating Frequency (MHz)						
		50	75	100	125	150	175	200
AL3 layered	40%	83.8	83.3	82.8	82.2	81.6	80.9	80.4
	60%	83.4	82.6	81.8	80.9	80.2	—	—
	80%	83.0	82.0	80.9	—	—	—	—
AL4 or 5 layered	40%	84.3	84.1	83.9	83.7	83.5	83.3	83.1
	60%	84.1	83.8	83.5	83.2	82.9	82.6	82.3
	80%	83.9	83.5	83.1	82.7	82.3	81.9	81.5
	100%	83.7	83.3	82.7	82.3	81.7	81.2	80.6
AL6 layered	40%	84.4	84.3	84.1	84.0	83.9	83.8	83.6
	60%	84.3	84.1	83.9	83.7	83.5	83.3	83.2
	80%	84.2	83.9	83.7	83.4	83.2	82.9	82.7
	100%	84.0	83.7	83.4	83.1	82.8	82.5	82.1

Note: Combinations left blank in the above table are not available.

From Tables 2-2 or 2-3, find the effective gate rate: β (%) corresponding to the maximum operating frequency: f (MHz), circuit percentage: α (%), and number of metalizations used: M . If the relevant operating frequency or circuit percentage does not exist, find the closest applicable value.

When the effective gate rate, β (%), is found, the necessary BC count, with reinforced power supplies considered, G_A , may be obtained from Equation (2) as follows:

$$G_A = G_0 / (\beta / 100) \dots (3)$$

For the actual chip, however, the wiring area used for P&R is required, in addition to the above. Here, let us define

$$G = G_A + (\text{wiring area required for P\&R}) \dots (4)$$

and further

$$G_A / G = P (\%) \dots (5)$$

The effective rates of wiring are summarized in Table 2-4. Using Table 2-4, find the effective rate of wiring: P (%) that corresponds to circuit size: G_0 and number of metalized layers: M . When calculating this effective rate of wiring, note that the circuit size: G_0 supplied by the customer, and not the G_A obtained above, is used as a parameter for the gate size. If the relevant circuit size does not exist, use the closest applicable value. When the effective rate of wiring, P (%), is found, the value of G may be obtained from Equation (5) as follows:

$$G = G_A / (P / 100) \dots (6)$$

The resulting G (gates or BCs) is the number of Basic Cells to be obtained.

Table 2-4 Effective Rate of Wiring

(%)

Gate	AL3 Layered	AL4 Layered	AL5 Layered	AL6 Layered
100k	75	80	85	90
200k	75	80	85	90
300k	70	75	80	85
400k	70	75	80	85
500k	65	70	75	80
600k	65	70	75	80
700k	65	70	75	80
800k	60	65	70	75
900k	60	65	70	75
1000k	60	65	70	75
1100k	55	60	65	70
1200k	55	60	65	70
1300k	55	60	65	70
1400k	55	60	65	70
1500k	55	60	65	70
1600k	55	60	65	70
1700k	55	60	65	70
1800k	55	60	65	70
1900k	55	60	65	70
2000k	55	60	65	70

Calculation example:

Estimate the number of gates used in MSI cells under the following conditions.

- Circuit size : 500k gates
- Maximum operating frequency : 66 MHz
- Circuit operating at 66 MHz : Approx. 200k gates
- Metalized layers used : 5 layers

First, determine the wiring width of reinforced power supplies. Using the values in Tables 2-2 and 2-3, determine whether the 1 BC or 2 BC type of reinforced power supply should be used. For the present example, the following applies:

- Operating frequency: 66 MHz → substituted with 75 MHz
- AL5-layered product
- Circuit percentage operating at 66 MHz (α)
 - = Circuit operating at f MHz / Circuit size x 100
 - = 200k / 500k x 100 = 40* (%)

* This value represents a percentage in cases in which cells are laid out evenly throughout the chip.

If cells are laid out unevenly so as to be concentrated in a specific location, the percentage should be increased to 60% or 80%.

Therefore, the effective gate rates may be obtained from Tables 2-2 and 2-3 as follows:

1 BC reinforced power supplies ... Effective gate rate = 90.3%

2 BC reinforced power supplies ... Effective gate rate = 84.1%

Thus, choose 1BC reinforced-power-supply rules, which have a better effective gate rate. From Equation (3), the necessary BC count, with reinforced power supplies considered, is

$$G_A = 500k / 0.903 = 553.7k \text{ (BCs)}$$

Next, determine the wiring efficiency.

From Table 2-4, we know that the effective rate of wiring for circuit size = 500k gates with an AL5-layered product is 75%. Therefore, substitute that value in Equation (6), and the following results:

$$G = 553.7k / 0.75 = 738.27k$$

Thus, the estimated number of gates used in the Basic Cell-type MSI cell is 739k (BCs).

2.2.3 Estimating the Number of Gates Used in Cell Based-Type MSI Cell

The number of gates used in the Cell Based-type MSI cell may be estimated with the same method shown in Section 2.2.2, “Estimating the Number of Gates Used in Basic Cell-Type MSI Cell.” In this case, however, note that the effective gate rates given in Tables 2-5 and 2-6 apply.

Table 2-5 Effective Gate Rates (1 BC)

(%)

Metalization Layers	Circuit Percentage	Operating Frequency (MHz)						
		50	75	100	125	150	175	200
AL3 or 4 layered	40%	90.6	89.7	88.1	85.1	80.2	—	—
	60%	90.0	88.6	85.9	82.5	—	—	—
	80%	89.4	87.5	84.0	—	—	—	—
AL5 or 6 layered	40%	91.3	91.0	90.7	90.5	90.2	89.8	89.6
	60%	91.1	90.7	90.3	89.8	89.4	89.0	88.4
	80%	90.9	90.3	89.8	89.3	88.6	87.9	87.5
	100%	90.6	90.0	89.3	88.6	87.9	87.1	85.9

Note: Combinations left blank in the above table are not available.

Table 2-6 Effective Gate Rates (2 BCs)

(%)

Metalization Layers	Circuit Percentage	Operating Frequency (MHz)						
		50	75	100	125	150	175	200
AL3 or 4 layered	40%	84.2	84.0	83.7	83.4	83.1	82.8	82.5
	60%	84.0	83.6	83.2	82.8	82.4	81.8	81.4
	80%	83.8	83.3	82.8	82.1	81.6	80.8	80.4
AL5 or 6 layered	40%	84.4	84.3	84.2	84.1	84.0	83.9	83.8
	60%	84.4	84.2	84.1	83.9	83.8	83.6	83.4
	80%	84.3	84.1	83.9	83.7	83.5	83.3	83.1
	100%	84.2	83.9	83.7	83.4	83.2	82.9	82.6

Note: Combinations left blank in the above table are not available.

Calculation example:

Estimate the number of gates used in MSI cells under the following conditions.

- Circuit size : 500k gates
- Maximum operating frequency : 150 MHz
- Circuit operating at 150 MHz : Approx. 300k gates
- Metalized layers used : 4 layers

First, determine the wiring width of reinforced power supplies. Use the values in Tables 2-5 and 2-6 to determine whether the 1 BC or 2 BC type of reinforced power supply should be used. For the present example, the following applies:

- Operating frequency: 150 MHz
- AL4-layered product
- Circuit percentage operating at 150 MHz (α)

$$= \text{Circuit operating at } f \text{ MHz} / \text{Circuit size} \times 100$$

$$= 300\text{k} / 500\text{k} \times 100 = 60^* (\%)$$

* This value represents a percentage in cases in which cells are laid out evenly throughout the chip. If cells are laid out unevenly so as to be concentrated on a specific location, the percentage should be increased to 80%.

Therefore, the effective gate rates may be obtained from Tables 2-5 and 2-6 as follows:

1 BC reinforced power supplies ... Effective gate rate = Not applicable

2 BC reinforced power supplies ... Effective gate rate = 82.4%

Because 1 BC reinforced power supplies are not applicable, choose 2 BC reinforced-power-supply rules. From Equation (3) in Section 2.2.2, "Estimating the Number of Gates Used in Basic Cell-Type MSI Cell," the necessary BC count, with reinforced power supplies considered, is

$$G_A = 500\text{k} / 0.824 = 606.8\text{k} \text{ (BCs)}$$

Next, determine the wiring efficiency.

From Table 2-4, we know that the effective rate of wiring for circuit size = 500k gates with an AL4-layered product is 70%. Therefore, substitute that value in Equation (6) in

Section 2.2.2, “Estimating the Number of Gates Used in Basic Cell-Type MSI Cell.” The following results:

$$G = 606.8k / 0.70 = 866.85k$$

Thus, the estimated number of gates used in the Cell Based-type MSI cell is 867k (BCs).

2.2.4 Estimating the Number of Gates Used in Basic Cell-Type RAM

For details on estimating the number of gates used in the S1K/S1X70000-series Basic Cell-type RAM, refer to Section 5.1.3, “RAM Sizes.”

2.2.5 Estimating the Number of Gates Used in Cell Based-Type RAM

For details on estimating the number of gates used in the S1K/S1X70000-series Cell Based-type RAM and ROM, please consult the sales division of Epson.

2.2.6 Estimating Bulk from the Implemented Circuit Size

Find the sum total of all gate counts that have been obtained in Sections 2.2.2 through 2.2.5; an approximate bulk size can be predicted from Table 2-1 based on that result.

2.3 Estimating the Number of Input/Output Pins

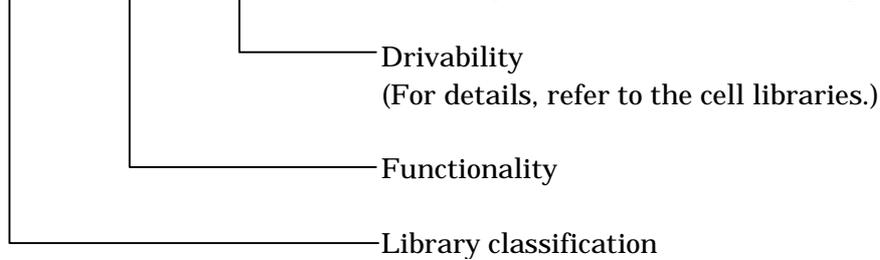
After the number of gates used in cells has been estimated, calculate the number of actually used input/output pins. When performing this calculation, make sure the test pins and power-supply pins on Basic Cell-type RAM and Cell Based-type RAM and ROM are included in the pin counts. To estimate the number of power-supply pins, use the method described in Section 7.11, "Pin Placement and Simultaneous Operation."

Chapter 3 MSI Cells

3.1 Naming Rules for MSI

With the S1K/S1X70000 series, the Basic Cell and Cell-Based types of MSI cells are available for multiple types of transistors. These types of MSI cells are functionally identified using the following naming rules:

K 1 N A 2 X 4 Cell Base/type of transistor: STD 1/2-input NAND/x4 output



Basic Cell Type	Cell-Based Type	Type of Transistor
L1*****	K1*****	Standard 1
L2*****	K2*****	High-Performance
L3*****	K3*****	Low-Leakage
L4*****	K4*****	Standard 2

3.2 MSI Cell Types

Below is a list of the functions of the MSI cell types in the S1K/S1X70000 series. The functions of all of these cells are common to L1 through L4 or K1 through K4. For more information, please contact the sales division of Epson.

List of cell functions in the S1K/S1X70000 series

- BUFFER
- INVERTER
- DELAY LINE
- AND GATE
INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
INPUT (5/6/8)
- NAND GATE
INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
INPUT (5/6/8)
- OR GATE
INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
INPUT (5/6/8)
- NOR GATE
INPUT (2/3/4) /INPUT (2/3/4) with Inverted Input (1/2/3)
INPUT (5/6/8)
- EXCLUSIVE OR/NOR
INPUT (2/3)
- AND-OR GATES
2-AND-OR INPUT (3/4/5/6/8)
3-AND-OR INPUT (4/5/6)
4-AND-OR INPUT (8)
- OR-AND GATES
2-OR-AND INPUT (3/4/5/6/8)
3-OR-AND INPUT (4/5/6)
4-OR-AND INPUT (8)
- MULTI-FUNCTION GATES
2-OR 2-AND 4-INPUT OR GATE
2-AND 2-OR 4-INPUT AND GATE
- MAJORITY GATES
2 of 3/Inverted 2 of 3
- CLOCK TREE
ROOT BUFFER
BUFFER/INVERTER

- GATED CLOCK
 - 2-INPUT AND GATE
 - 2-INPUT OR GATE
 - 2-INPUT NAND GATE
 - 2-INPUT NOR GATE
 - INVERTER
 - SELECTOR/MULTIPLEXER
- FLIP FLOPS
 - D-FLIP FLOP
 - SET/RESET
 - SYNCHRONOUS
 - ENABLE
 - OUTPUT Q
 - NEGATIVE CLOCK
 - SCAN
 - JK-FLIP FLOP
 - SET/RESET
 - OUTPUT Q
 - SCAN
 - RS-FLIP FLOP
 - NAND-TYPE/NOR-TYPE
- LATCHES
 - PRESET/RESET
 - OUTPUT M
 - NEGATIVE CLOCK
- ADDER
- DECODERS
 - 2-LINE to 4-LINE
 - ENABLE
- SELECTORS/MULTIPLEXERS
 - 2-LINE to 1-LINE
 - 4-LINE to 1-LINE
 - ENABLE
 - QUADRUPLE 2-LINE to 1-LINE
 - ENABLE
 - NEGATIVE OUTPUT
- BUS CELLS
 - LATCH
 - 3-STATE BUFFER
 - LOW ENABLE/HIGH ENABLE

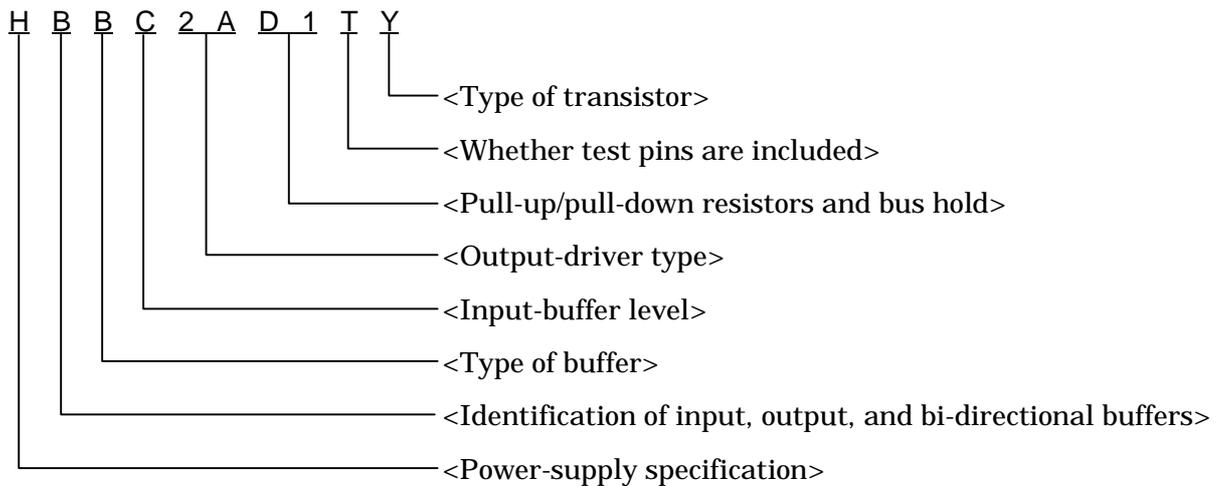
Chapter 4 Types of Input/Output Buffers and Their Use

This chapter describes in detail how the input buffers, output buffers, and bi-directional buffers are constructed.

4.1 Selecting Input/Output Buffers

4.1.1 Naming Rules for Input/Output Buffers

The S1K/S1X70000 series uses the following naming rules to identify the functionality of input/output buffers (except for some buffers).



<Power-supply specification>

H: HV_{DD} system of dual power supplies

L: LV_{DD} system of dual power supplies

M: Single power supply

<Identification of input, output, and bi-directional buffers>

I: Input buffer

B: Bi-directional buffer

O: Output buffer

T: Three-state buffer

<Type of buffer>

B: Ordinary buffer

F: Fail-Safe type

D: Open drain type

<Input-buffer level>

- C: LVCMOS level
- H: LVCMOS Schmitt level
- T: LVTTL level
- A: Gated
- V: Cutoff

<Output-driver type>

- 1A: Type 1 High speed
- 2A: Type 2 High speed
- 3A: Type 3 High speed
- 4A: Type 4 High speed
- 1B: Type 1 Low noise
- 2B: Type 2 Low noise
- 3B: Type 3 Low noise
- 4B: Type 4 Low noise

<Pull-up/pull-down resistors and bus hold>

- D1: Pull-down resistor (Type 1)
- D2: Pull-down resistor (Type 2)
- P1: Pull-up resistor (Type 1)
- P2: Pull-up resistor (Type 2)
- H: Bus hold
- None: Without pull-up/pull-down resistors and bus hold

<Whether test pins are included>

- T: Test pins included
- None: Without test pins

<Type of transistor>

- X: 2.5-V input/output buffers
- Y: 3.3-V input/output buffers

4.1.2 Bus-Hold Circuit

To ensure that the output pins and bi-directional pins will not enter a high-impedance state, the S1K/S1X70000 series has available an input/output buffer that comes equipped with a bus-hold facility to hold the data at the output pins.

However, because the bus-hold circuit's retention capability is suppressed so as not to adversely affect the ordinary operation of the cell, do not use the output data held by the circuit as valid data. The retained data may easily change state when any data is supplied from an external circuit.

For the bus-hold circuit's output retention current, refer to Table 1-7, Tables 1-10 through 1-12, and Tables 1-19 through 1-21.

4.2 Input/Output Buffers for a Single Power Supply (3.3 V: Y Type)

When the input/output buffers are used with a single power supply, the useful power-supply voltage is 1.8 V or 1.5 V only.

4.2.1 Input Buffers

Table 4-1 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	V _{DD} = 1.8 V	V _{DD} = 1.5 V	
Type 1	60	90	kΩ
Type 2	120	180	kΩ

Table 4-2 Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
MIBCY MIBCP#TY MIBCD#TY	LVC MOS LVC MOS LVC MOS	None Pull-up resistor included Pull-down resistor included
MIBHY MIBHP#TY MIBHD#TY	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor included Pull-down resistor included

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down-resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

*2: In addition to the configurations shown in Table 4-2, the input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.2.2 Output Buffers

Tables 4-4 and 4-6 list the output buffers (3.3-V buffers: Y type).

Table 4-3 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}		Unit
	$V_{DD} = 1.8\text{ V}$	$V_{DD} = 1.5\text{ V}$	
Type 1	-1/1	-0.75/0.75	mA
Type 2	-2/2	-1.5/1.5	mA
Type 3	-4/4	-3/3	mA
Type 4	-6/6	-4.5/4.5	mA

Notes *1: $V_{OH} = V_{DD} - 0.4\text{ V}$

*2: $V_{OL} = 0.4\text{ V}$

Table 4-4 Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	MOB#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	MOB#BTY
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	MTB#ATY
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	MTB#BTY
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MTB#AHTY
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MTB#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-4, the output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-5 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}^{*1}		Unit
	$V_{DD} = 1.8\text{ V}$	$V_{DD} = 1.5\text{ V}$	
Type 1	1	0.75	mA
Type 2	2	1.5	mA
Type 3	4	3	mA
Type 4	6	4.5	mA

Note *1: $V_{OL} = 0.4\text{ V}$

Table 4-6 N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	MOD#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	MOD#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-5).

*2: In addition to the configurations in Table 4-6, the N channel open drain output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.2.3 Bi-directional Buffers

Tables 4-7 and 4-8 list bi-directional buffers (3.3-V buffers: Y type).

Table 4-7 Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBH#BTY
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBC#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBC#BHTY
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBH#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBH#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-7, the bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-8 N channel Open drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name*1, *2
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBDC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBDC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBDH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBDH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-5).

*2: In addition to the configurations shown in Table 4-8, the N channel open drain bi-directional buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.2.4 Fail Safe Cells

4.2.4.1 Overview

The S1K/S1X70000-series Fail Safe cells allow signals above the power-supply voltage to be interfaced, even while power is supplied.

Furthermore, no leakage current flows in those cells, despite the fact that the signals are interfaced while the power is cut off. Therefore, they provide greater freedom of design than ever before.

4.2.4.2 Features

- (1) The Fail Safe cells can be positioned as desired by customers. There are no limitations on the number of cells that can be used or the locations in which they can be placed.
- (2) Even when input signals above the power-supply voltage are applied while power is supplied, no input leakage current flows. (For input buffers or bi-directional buffers with pull-up resistors, however, a small input leakage current of approximately 30 μA may flow due to their circuit configuration.)
- (3) Even when input signals are applied from the outside while the power is cut off, no input leakage current flows.
- (4) Fail Safe cells with two different input levels, the LVCMOS level and the LVCMOS Schmitt level, are available.
- (5) Because the Fail Safe cells are completely CMOS-structured, the power consumption can be suppressed to a minimum.

4.2.4.3 Usage Precautions

- (1) About input I/O cells
 - For input buffers without resistors or with pull-down resistors, ordinary input buffers may be used directly as Fail Safe cells.
 - If input buffers with pull-up resistors are needed, always be sure to use Fail Safe cells (however, a small input leakage current of approximately 30 μA may flow due to their circuit configuration).
- (2) About output I/O cells
 - Provided that the output buffers are placed in High-Z state or the bi-directional buffers are placed in input mode, no input leakage current may flow even when input signals above the power-supply voltage are applied while power is supplied.
 - If signals above the power-supply voltage are applied while the bi-directional buffers are placed in output mode, an input leakage current flows as in ordinary input/output buffers. The same applies when pull-up resistors above the power-supply voltage exist outside the chip. (If a High logic level above the power-supply voltage is needed, use open drain type input/output buffers, with pull-up resistors added external to the chip in order to pull up the logic level High.)
- (3) Although the Fail Safe cells can receive high-voltage signals above the LSI's operating voltage, be aware that the signal voltages applied to the Fail Safe cells must never exceed their rated maximum voltage.

4.2.4.4 List of Cells

Table 4-9 Fail Safe Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up Resistors are Included
MIFCP#TY	LVC MOS	Pull-up resistor included
MIFHP#TY	LVC MOS Schmitt	Pull-up resistor included

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

*2: In addition to the configurations shown in Table 4-9, the Fail Safe input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-10 Fail Safe Output Buffers List

Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	MTF#ATY
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	MTF#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-10, the Fail Safe output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-11 Fail Safe Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBFC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBFC#BTY
LVC MOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBFH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBFH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-11, the Fail Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.2.5 Gated Cells

4.2.5.1 Overview

The S1K/S1X70000-series Gated cell is the first product that allows inputs to pins to be placed in the floating, or High-Z, state without the use of pull-up or pull-down circuits. They also allow the input signals to be shut off by pulling down the control signals Low.

4.2.5.2 Features

- (1) The Gated cells can be positioned as desired by customers. There are no limitations on the number of cells used or the locations in which they are placed. As a result, freedom of design is increased.
- (2) Inputs can be placed in the High-Z state without the use of pull-up or pull-down circuits.
- (3) Input signals can be shut off by pulling down the control signals Low.
- (4) The input level for the Gated cells is the LVCMOS level.
- (5) Because the Gated cells are completely CMOS-structured, the power consumption can be suppressed to a minimum.

4.2.5.3 Usage Precautions

To place inputs in the High-Z state through the use of Gated cells, inputs to pins must be shut off by using Gated-cell control signals before they enter the High-Z state. If inputs are placed in the High-Z state without performing this control, current may flow into the Gated cell as in ordinary cells. In such a case, the logic level latched into the device's internal circuit cannot be guaranteed.

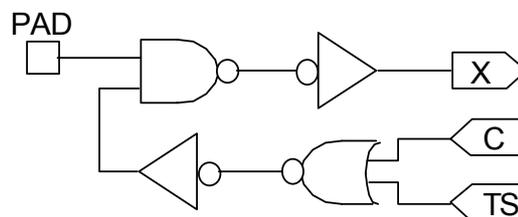


Figure 4-1 Gated-Cell Circuit

4.2.5.4 List of Cells

Table 4-12 Gated Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
MIBATY	LVCMOS	None
MIBAP#TY	LVCMOS	Pull-up resistor included
MIBAD#TY	LVCMOS	Pull-down resistor included

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-1).

*2: In addition to the configurations shown in Table 4-12, the use of Gated input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-13 Gated Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBA#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBA#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-3).

*2: In addition to the configurations shown in Table 4-13, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.3 Dual-Power-Supply Input/Output Buffers (3.3-V Buffers: Y Type)

If your system uses dual power supplies, use input/output buffers designed exclusively for operation with dual power supplies.

(In this case, be careful not to use input/output buffers designed for operation with a single power supply.)

(1) HV_{DD} input/output buffers

The HV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 3.3-V (or 2.5-V) signals, output buffers that output 3.3-V (or 2.5-V) amplitude signals, and bi-directional buffers that accept as input 3.3-V (or 2.5-V) signals or output 3.3-V (or 2.5-V) amplitude signals.

(2) LV_{DD} input/output buffers

The LV_{DD} input/output buffers are available in several types. These include input buffers that accept as input 1.8-V (or 1.5-V) signals, output buffers that output 1.8-V (or 1.5-V) amplitude signals, and bi-directional buffers that accept as input 1.8-V (or 1.5-V) signals or output 1.8-V (or 1.5-V) amplitude signals.

For LV_{DD} input or bi-directional buffers with pull-up resistors, do not apply voltages above LV_{DD}. This is due to the fact that, if HV_{DD} signals are supplied to those buffers, an excessive current flows in their internal protective diode, causing their quality to degrade (in such a case, use the Fail Safe cells described in Section 4.3.4, "Fail Safe Cells").

4.3.1 Input Buffers

(1) HV_{DD} input buffers

The input buffers are configured using only input cells.

The HV_{DD} input buffers consist of a first input stage configured with an HV_{DD} input circuit and a next stage configured with an LV_{DD} circuit, so that HV_{DD} signals are converted into LV_{DD} signals before being fed into the MSI cell (internal cell area).

Table 4-15 lists the HV_{DD} input buffers (3.3-V buffers: Y type).

Table 4-14 Rated Pull-up/Pull-down-Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	HV _{DD} = 3.3 V	HV _{DD} = 2.5 V	
Type 1	50	70	kΩ
Type 2	100	140	kΩ

Table 4-15 HV_{DD} Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
HIBCY HIBCP#TY HIBCD#TY	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor
HIBTY HIBTP#TY HIBTD#TY	LVTTL LVTTL LVTTL	None Pull-up resistor Pull-down resistor
HIBHY HIBHP#TY HIBHD#TY	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor Pull-down resistor
HIBPCIY HIBPCIP#TY HIBPCID#TY	PCI-3 V PCI-3 V PCI-3 V	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down-resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-14).

*2: In addition to the configurations shown in Table 4-15, the HV_{DD} input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} input buffers

The input buffers are configured using only input cells. Table 4-17 lists the LV_{DD} input buffers (3.3-V buffers: Y type).

Table 4-16 Rated Pull-up/Pull-down-Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	LV _{DD} = 1.8 V	LV _{DD} = 1.5 V	
Type 1	60	90	kΩ
Type 2	120	180	kΩ

Table 4-17 LV_{DD} Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
LIBCY LIBCP#TY LIBCD#TY	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor
LIBHY LIBHP#TY LIBHD#TY	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-16).

*2: In addition to the configurations shown in Table 4-17, the LV_{DD} input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.3.2 Output Buffers

(1) HV_{DD} output buffers

Tables 4-19 and 4-21 list the HV_{DD} output buffers (3.3-V buffers: Y type).

Table 4-18 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I _{OH} ^{*1} /I _{OL} ^{*2}		Unit
	HV _{DD} = 3.3 V	HV _{DD} = 2.5 V	
Type 1	-2/2	-1.5/1.5	mA
Type 2	-4/4	-3/3	mA
Type 3	-8/8	-6/6	mA
Type 4	-12/12	-9/9	mA

Note *1: V_{OH} = HV_{DD} - 0.4 V

*2: V_{OL} = 0.4 V

Table 4-19 HV_{DD} Output Buffers List

Function	I _{OL} /I _{OH}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	HOB#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	HOB#BTY
Normal output for PCI	PCI-3 V	HOBPCITY ^{*3}
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	HTB#ATY
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	HTB#BTY
3-state output for PCI	PCI-3 V	HTBPCITY ^{*3}
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HTB#AHTY
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HTB#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-19, the HV_{DD} output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

*3: PCI-3 V cells use two input/output-buffer areas.

Table 4-20 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}^{*1}		Unit
	$HV_{DD} = 3.3\text{ V}$	$HV_{DD} = 2.5\text{ V}$	
Type 1	2	1.5	mA
Type 2	4	3	mA
Type 3	8	6	mA
Type 4	12	9	mA

Note *1: $V_{OL} = 0.4\text{ V}$

Table 4-21 HV_{DD} N channel Open drain Output Buffers List

Function	I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	HOD#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	HOD#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-20).

*2: In addition to the configurations shown in Table 4-21, the HV_{DD} N channel open drain output buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} output buffers

Tables 4-23 and 4-25 list the LV_{DD} output buffers (3.3-V buffers: Y type).

Table 4-22 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}		Unit
	$LV_{DD} = 1.8\text{ V}$	$LV_{DD} = 1.5\text{ V}$	
Type 1	-1/1	-0.75/0.75	mA
Type 2	-2/2	-1.5/1.5	mA
Type 3	-4/4	-3/3	mA
Type 4	-6/6	-4.5/4.5	mA

Notes *1: $V_{OH} = LV_{DD} - 0.4\text{ V}$

*2: $V_{OL} = 0.4\text{ V}$

Table 4-23 LV_{DD} Output Buffers List

Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	LOB#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	LOB#BTY
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	LTB#ATY
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	LTB#BTY
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LTB#AHTY
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LTB#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-23, the LV_{DD} output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-24 Rated I_{OL} Values at Each Voltage

Type of Output Current	I _{OL} ^{*1}		Unit
	LV _{DD} = 1.8 V	LV _{DD} = 1.5 V	
Type 1	1	0.75	mA
Type 2	2	1.5	mA
Type 3	4	3	mA
Type 4	6	4.5	mA

Note *1: V_{OL} = 0.4 V

Table 4-25 LV_{DD} N channel Open drain Output Buffers List

Function	I _{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	LOD#ATY
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	LOD#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-24).

*2: In addition to the configurations shown in Table 4-25, the LV_{DD} N channel open drain output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.3.3 Bi-directional Buffers

(1) HV_{DD} bi-directional buffers

Tables 4-26 and 4-27 list the HV_{DD} bi-directional buffers (3.3-V buffers: Y type).

Table 4-26 HV_{DD} Bi-directional Buffers List (1/2)

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVTTTL	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBT#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBT#BTY
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBC#BTY
PCI	Bi-directional output for PCI	PCI-3 V	HBBPCITY ^{*3}
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-26, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

*3: PCI-3 V cells use two input/output-buffer areas.

Table 4-26 List of HV_{DD} Bi-directional Buffers List (2/2)

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVTTL	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBT#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBT#BHTY
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBC#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBC#BHTY
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBH#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBH#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-26, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-27 HV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name ^{*1, *2}
LVTTTL	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDT#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDT#BTY
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-20).

*2: In addition to the configurations shown in Table 4-27, the HV_{DD} N channel open drain bi-directional buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} bi-directional buffers

Tables 4-28 and 4-29 list the LV_{DD} bi-directional buffers (3.3-V buffers: Y type).

Table 4-28 LV_{DD} Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBH#BTY
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBC#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBC#BHTY
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBH#AHTY
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBH#BHTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-28, the LV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-29 LV_{DD} N channel Open drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBDC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBDC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBDH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBDH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-24).

*2: In addition to the configurations shown in Table 4-29, the LV_{DD} N channel open drain bi-directional buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.3.4 Fail Safe Cells

4.3.4.1 Overview

The dual-power-supply Fail Safe cells are outlined in Section 4.2.4.1, “Overview” (the Fail Safe cells used in the dual-power-supply specification are LV_{DD} cells).

4.3.4.2 Features

For the features of the dual-power-supply Fail Safe cells, refer to Section 4.2.4.2, “Features.”

4.3.4.3 Usage Precautions

For precautions to be taken when dual-power-supply Fail Safe cells are used, refer to Section 4.2.4.3, “Usage Precautions.”

4.3.4.4 List of Cells

Table 4-30 Fail Safe Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up Resistors are Included
LIFCP#TY	LVC MOS	Pull-up Resistors
LIFHP#TY	LVC MOS Schmitt	Pull-up Resistors

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-16).

*2: In addition to the configurations shown in Table 4-30, the Fail Safe input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-31 Fail Safe Output Buffers List

Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	LTF#ATY
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	LTF#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-31, the Fail Safe output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-32 Fail Safe Bi-directional Buffers List

Input Level	Function	I_{OH}/I_{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBFC#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBFC#BTY
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBFH#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBFH#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-32, the Fail Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.3.5 Gated Cells

4.3.5.1 Overview

The dual-power-supply Gated cells are outlined in Section 4.2.5.1, “Overview.” (The Gated cells for the dual-power-supply specification are LV_{DD} cells.)

4.3.5.2 Features

For the features of the dual-power-supply Gated cells, refer to Section 4.2.5.2, “Features.”

4.3.5.3 Usage Precautions

For the precautions to be taken when dual-power-supply Gated cells are used, refer to Section 4.2.5.3, “Usage Precautions.”

4.3.5.4 List of Cells

Table 4-33 Gated Cell Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
LIBATY	LVC MOS	None
LIBAP#TY	LVC MOS	Pull-up resistor
LIBAD#TY	LVC MOS	Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-16).

*2: In addition to the configurations shown in Table 4-33, the Gated input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-34 Gated Cell Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBA#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBA#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-22).

*2: In addition to the configurations shown in Table 4-34, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.3.6 Cutoff Cells

4.3.6.1 Overview

The S1K/S1X70000 series includes a new type of cell known as a Cutoff cell, which is used to cut off a high-voltage (HV) power supply.

The Cutoff cells allow the high-voltage (HV_{DD}) power supply in a dual-power-supply design to be cut off. By pulling control signals Low, it is possible to inhibit current from flowing in HV input cells.

4.3.6.2 Features

- (1) The Cutoff cells can be positioned as desired by customers. There are no limitations on the number of cells used or the locations in which they are placed. This provides greater freedom of design.
- (2) When the HV_{DD} power supply is to be cut off while the LV_{DD} power supply is on, it is possible to inhibit current from flowing in the input buffers by pulling control signals Low.
- (3) When bi-directional buffers are used, however, make sure that, after the HV_{DD} power supply is cut off, inputs are left in the floating, or High-Z, state. If input signals are applied while the HV_{DD} power supply is off, current leakage occurs.

4.3.6.3 Usage Precautions

To place inputs in the High-Z state through the use of Cutoff cells, inputs to pins must be shut off by pulling control signals Low before they enter the High-Z state. If inputs are placed in the High-Z state without performing this control, current may flow into the Cutoff cell as in ordinary cells.

In addition, make sure the control signal is always held High except in Cutoff mode. If a Low-level signal is applied to any pin while the control signal remains Low, an amount of current equivalent to the pull-down resistance continues flowing into the input buffer.

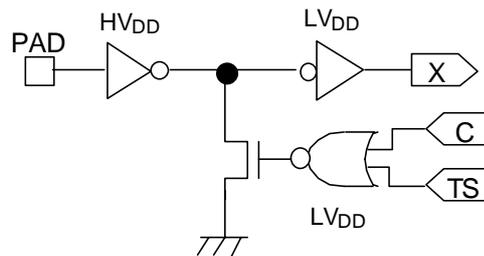


Figure 4-2 Cutoff Cell Circuit

4.3.6.4 List of Cells

Table 4-35 Cutoff Cell Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
HIBVTY HIBVP#TY HIBVD#TY	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-14).

*2: In addition to the configurations shown in Table 4-35, the Cutoff input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-36 Cutoff Cell Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBV#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBV#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-18).

*2: In addition to the configurations shown in Table 4-36, the Cutoff bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-37 Cutoff Cell N Channel Open Drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDV#ATY
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDV#BTY

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-20).

*2: In addition to the configurations shown in Table 4-37, the Cutoff N channel open drain bi-directional buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.4 Single-Power-Supply Input/Output Buffers (2.5-V Buffers: X Type)

4.4.1 Input Buffers

Table 4-38 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	V _{DD} = 1.8 V	V _{DD} = 1.5 V	
Type 1	45	70	kΩ
Type 2	90	140	kΩ

Table 4-39 Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
MIBCX MIBCP#TX MIBCD#TX	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor
MIBHX MIBHP#TX MIBHD#TX	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-38).

*2: In addition to the configurations shown in Table 4-39, the input buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.4.2 Output Buffers

Tables 4-41 and 4-43 list the output buffers (2.5-V buffers: X type).

Table 4-40 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I _{OH} ^{*1} /I _{OL} ^{*2}		Unit
	V _{DD} = 1.8 V	V _{DD} = 1.5 V	
Type 1	-1.5/1.5	-1/1	mA
Type 2	-3/3	-2/2	mA
Type 3	-6/6	-4/4	mA
Type 4	-9/9	-6/6	mA

Note *1: V_{OH} = V_{DD} - 0.4 V

*2: V_{OL} = 0.4 V

Table 4-41 Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	MOB#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	MOB#BTX
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	MTB#ATX
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	MTB#BTX
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MTB#AHTX
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MTB#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-40).

*2: In addition to the configurations shown in Table 4-41, the output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-42 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL} ^{*1}		Unit
	$V_{DD} = 1.8\text{ V}$	$V_{DD} = 1.5\text{ V}$	
Type 1	1.5	1	mA
Type 2	3	2	mA
Type 3	6	4	mA
Type 4	9	6	mA

Note *1: $V_{OL} = 0.4\text{ V}$

Table 4-43 N Channel Open Drain Output Buffers List

Function	I _{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	MOD#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	MOD#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-42).

*2: In addition to the configurations shown in Table 4-43, the N channel open drain output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.4.3 Bi-directional Buffers

Tables 4-44 and 4-45 list the bi-directional buffers (2.5-V buffers: X type).

Table 4-44 Bi-directional Buffers List

	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBH#BTX
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBC#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBC#BHTX
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBH#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	MBBH#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-40).

*2: In addition to the configurations shown in Table 4-44, the bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-45 N Channel Open Drain Bi-directional Buffers List

	Function	I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBDC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBDC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBDH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBDH#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-42).

*2: In addition to the configurations shown in Table 4-45, the N channel open drain bi-directional buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.4.4 Fail Safe Cells

4.4.4.1 Overview

The Fail Safe cells are outlined in Section 4.2.4.1, "Overview."

4.4.4.2 Features

For the features of the Fail Safe cells, refer to Section 4.2.4.2, "Features."

4.4.4.3 Usage Precautions

For the precautions to be taken in the use of the Fail Safe cells, refer to Section 4.2.4.3, "Usage Precautions."

4.4.4.4 List of Cells

Table 4-46 Fail Safe Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up Resistors are Included
MIFCP#TX	LVC MOS	Pull-up resistor
MIFHP#TX	LVC MOS Schmitt	Pull-up resistor

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-38).

*2: In addition to the configurations shown in Table 4-46, the Fail Safe input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-47 Fail Safe Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name ^{*1, *2}
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	MTF#ATX
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	MTF#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-40).

*2: In addition to the configurations shown in Table 4-47, the Fail Safe output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-48 Fail Safe Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBFC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBFC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBFH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBFH#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-40).

*2: In addition to the configurations shown in Table 4-48, the Fail Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.4.5 Gated Cells

4.4.5.1 Overview

The Gated cells are outlined in Section 4.2.5.1, "Overview."

4.4.5.2 Features

For the features of the Gated cells, refer to Section 4.2.5.2, "Features."

4.4.5.3 Usage Precautions

For the precautions to be taken in the use of Gated cells, refer to Section 4.2.5.3, "Usage Precautions."

4.4.5.4 List of Cells

Table 4-49 Gated Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
MIBATX	LVC MOS	None
MIBAP#TX	LVC MOS	Pull-up resistor
MIBAD#TX	LVC MOS	Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-38).

*2: In addition to the configurations shown in Table 4-49, the Gated input buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-50 Gated Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	MBBA#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	MBBA#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-40).

*2: In addition to the configurations shown in Table 4-50, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.5 Dual-Power-Supply Input/Output Buffers (2.5-V Buffers: X Type)

If your system uses dual power supplies, use input/output buffers designed exclusively for operation with dual power supplies. (In this case, be careful not to use input/output buffers designed for operation with a single power supply).

(1) HV_{DD} input/output buffers

The HV_{DD} input/output buffers are available in several types, including input buffers that accept as input 2.5-V signals, output buffers that output 2.5-V amplitude signals, and bi-directional buffers that accept as input 2.5-V signals or output 2.5-V amplitude signals.

(2) LV_{DD} input/output buffers

The LV_{DD} input/output buffers are available in several types, including input buffers that accept as input 1.8-V (or 1.5-V) signals, output buffers that output 1.8-V (or 1.5-V) amplitude signals, and bi-directional buffers that accept as input 1.8-V (or 1.5-V) signals or output 1.8-V (or 1.5-V) amplitude signals.

For LV_{DD} input or bi-directional buffers with pull-ups, do not apply voltages above LV_{DD}. This is due to the fact that, if HV_{DD} signals are supplied to those buffers, an excessive current flows in their internal protective diode, causing their quality to degrade. (In such a case, use the Fail Safe cells described in Section 4.5.4, "Fail Safe Cells.")

4.5.1 Input Buffers

(1) HV_{DD} input buffers

The input buffers are configured using only input cells.

The HV_{DD} input buffers consist of a first input stage configured using an HV_{DD} input circuit and a next stage configured using an LV_{DD} circuit, so that HV_{DD} signals are converted into LV_{DD} signals before being fed into the MSI cell (internal cell area).

Table 4-52 lists the HV_{DD} input buffers (2.5-V buffers: X type).

Table 4-51 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value	Unit
	HV _{DD} = 2.5 V	
Type 1	50	kΩ
Type 2	100	kΩ

Table 4-52 HV_{DD} Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
HIBCX HIBCP#TX HIBCD#TX	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor
HIBHX HIBHP#TX HIBHD#TX	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-51).

*2: In addition to the configurations shown in Table 4-52, the HV_{DD} input buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} input buffers

The input buffers are configured using only input cells.

Table 4-54 lists the LV_{DD} input buffers (2.5-V buffers: X type).

Table 4-53 Rated Pull-up/Pull-down Resistance Values at Each Voltage

Type of Pull-up/Pull-down Resistor	Resistance Value		Unit
	LV _{DD} = 1.8 V	LV _{DD} = 1.5 V	
Type 1	45	70	kΩ
Type 2	90	140	kΩ

Table 4-54 LV_{DD} Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
LIBCX LIBCP#TX LIBCD#TX	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor
LIBHX LIBHP#TX LIBHD#TX	LVC MOS Schmitt LVC MOS Schmitt LVC MOS Schmitt	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-53).

*2: In addition to the configurations shown in Table 4-54, the LV_{DD} input buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

4.5.2 Output Buffers

(1) HV_{DD} output buffers

Tables 4-56 and 4-58 list the HV_{DD} output buffers (2.5-V buffers: X type).

Table 4-55 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}	Unit
	$HV_{DD} = 2.5 V$	
Type 1	-2/2	mA
Type 2	-4/4	mA
Type 3	-8/8	mA
Type 4	-12/12	mA

Notes *1: $V_{OH} = HV_{DD} - 0.4 V$ *2: $V_{OL} = 0.4 V$ **Table 4-56** HV_{DD} Output Buffers List

Function	I_{OH}/I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	HOB#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	HOB#BTX
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	HTB#ATX
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	HTB#BTX
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HTB#AHTX
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HTB#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-55).*2: In addition to the configurations shown in Table 4-56, the HV_{DD} output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-57 Rated I_{OL} Values at Each Voltage

Type of Output Current	I_{OL}^{*1}	Unit
	$HV_{DD} = 2.5\text{ V}$	
Type 1	2	mA
Type 2	4	mA
Type 3	8	mA
Type 4	12	mA

Note *1: $V_{OL} = 0.4\text{ V}$

Table 4-58 HV_{DD} N Channel Open Drain Output Buffers List

Function	I_{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	HOD#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	HOD#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-57).

*2: In addition to the configurations shown in Table 4-58, the HV_{DD} N channel open drain output buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} output buffers

Tables 4-60 and 4-62 list the LV_{DD} output buffers (2.5-V buffers: X type).

Table 4-59 Rated I_{OH} and I_{OL} Values at Each Voltage

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}		Unit
	$LV_{DD} = 1.8\text{ V}$	$LV_{DD} = 1.5\text{ V}$	
Type 1	-1.5/1.5	-1/1	mA
Type 2	-3/3	-2/2	mA
Type 3	-6/6	-4/4	mA
Type 4	-9/9	-6/6	mA

Notes *1: $V_{OH} = LV_{DD} - 0.4\text{ V}$

*2: $V_{OL} = 0.4\text{ V}$

Table 4-60 LV_{DD} Output Buffers List

Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	LOB#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	LOB#BTX
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	LTB#ATX
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	LTB#BTX
3-state output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LTB#AHTX
3-state output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LTB#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-59).

*2: In addition to the configurations shown in Table 4-60, the LV_{DD} output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-61 Rated I_{OL} Values at Each Voltage

Type of Output Current	I _{OL} ^{*1}		Unit
	LV _{DD} = 1.8 V	LV _{DD} = 1.5 V	
Type 1	1.5	1	mA
Type 2	3	2	mA
Type 3	6	4	mA
Type 4	9	6	mA

Note *1: V_{OL} = 0.4 V

Table 4-62 LV_{DD} N Channel Open Drain Output Buffers List

Function	I _{OL}	Cell Name ^{*1, *2}
Normal output for high speed	Type 1 Type 2 Type 3 Type 4	LOD#ATX
Normal output for low noise	Type 1 Type 2 Type 3 Type 4	LOD#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-61).

*2: In addition to the configurations shown in Table 4-62, the LV_{DD} N channel open drain output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.5.3 Bi-directional Buffers

(1) HV_{DD} bi-directional buffers

Tables 4-63 and 4-64 list the HV_{DD} bi-directional buffers (2.5-V buffers: X type).

Table 4-63 HV_{DD} Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBH#BTX
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBC#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBC#BHTX
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBH#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	HBBH#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-55).

*2: In addition to the configurations shown in Table 4-63, the HV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-64 HV_{DD} N Channel Open Drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDH#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-57).

*2: In addition to the configurations shown in Table 4-64, the HV_{DD} N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

(2) LV_{DD} bi-directional buffers

Tables 4-65 and 4-66 list the LV_{DD} bi-directional buffers (2.5-V buffers: X type).

Table 4-65 LV_{DD} Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBH#BTX
LVCMOS	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBC#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBC#BHTX
LVCMOS Schmitt	Bi-directional output for high speed (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBH#AHTX
	Bi-directional output for low noise (Bus hold circuit)	Type 1 Type 2 Type 3 Type 4	LBBH#BHTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-59).

*2: In addition to the configurations shown in Table 4-65, the LV_{DD} bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-66 LV_{DD} N Channel Open Drain Bi-directional Buffers List

Input Level	Function	I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBDC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBDC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBDH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBDH#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-61).

*2: In addition to the configurations shown in Table 4-66, the LV_{DD} N channel open drain bi-directional buffers may be configured without test pins. Customers desiring to use such configurations should direct inquiries to Epson.

4.5.4 Fail Safe Cells

4.5.4.1 Overview

The dual-power-supply Fail Safe cells are outlined in Section 4.2.4.1, “Overview.” (The Fail Safe cells for the dual-power-supply specification are LV_{DD} cells.)

4.5.4.2 Features

For the features of the dual-power-supply Fail Safe cells, refer to Section 4.2.4.2, “Features.”

4.5.4.3 Usage Precautions

For the precautions to be taken in the use of the dual-power-supply Fail Safe cells, refer to Section 4.2.4.3, “Usage Precautions.”

4.5.4.4 List of Cells

Table 4-67 Fail Safe Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up Resistors are Included
LIFCP#TX	LVC MOS	Pull-up Resistors
LIFHP#TX	LVC MOS Schmitt	Pull-up Resistors

Notes *1: The # denotes 1 or 2, with the pull-up resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-53).

*2: In addition to the configurations shown in Table 4-67, the Fail Safe input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-68 Fail Safe Output Buffers List

Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
3-state output for high speed	Type 1 Type 2 Type 3 Type 4	LTF#ATX
3-state output for low noise	Type 1 Type 2 Type 3 Type 4	LTF#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-59).

*2: In addition to the configurations shown in Table 4-68, the Fail Safe output buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-69 Fail Safe Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBFC#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBFC#BTX
LVCMOS Schmitt	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBFH#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBFH#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-59).

*2: In addition to the configurations shown in Table 4-69, the Fail Safe bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.5.5 Gated Cells

4.5.5.1 Overview

The dual-power-supply Gated cells are outlined in Section 4.2.5.1, “Overview.”
(The Gated cells for the dual-power-supply specification are LV_{DD} cells).

4.5.5.2 Features

For the features of the dual-power-supply Gated cells, refer to Section 4.2.5.2, “Features.”

4.5.5.3 Usage Precautions

For the precautions to be taken in the use of dual-power-supply Gated cells, refer to Section 4.2.5.3, “Usage Precautions.”

4.5.5.4 List of Cells

Table 4-70 Gated Cell Input Buffers List

Cell Name ^{*1,*2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
LIBATX LIBAP#TX LIBAD#TX	LVC MOS LVC MOS LVC MOS	None Pull-up resistor Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-53).

*2: In addition to the configurations shown in Table 4-70, the Gated input buffers may be configured without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-71 Gated Cell Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1,*2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	LBBA#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	LBBA#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-59).

*2: In addition to the configurations shown in Table 4-71, the Gated bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.5.6 Cutoff Cells

4.5.6.1 Overview

The dual-power-supply Cutoff cells are outlined in Section 4.3.6.1, “Overview.”

4.5.6.2 Features

For the features of the dual-power-supply Cutoff cells, refer to Section 4.3.6.2, “Features.”

4.5.6.3 Usage Precautions

For the precautions to be taken in use of the dual-power-supply Cutoff cells, refer to Section 4.3.6.3, “Usage Precautions.”

4.5.6.4 List of Cells

Table 4-72 Cutoff Cell Input Buffers List

Cell Name ^{*1, *2}	Input Level	Whether Pull-up/Pull-down Resistors are Included
HIBVTX	LVC MOS	None
HIBVP#TX	LVC MOS	Pull-up resistor
HIBVD#TX	LVC MOS	Pull-down resistor

Notes *1: The # denotes 1 or 2, with the pull-up/pull-down resistance values corresponding to Type 1 and Type 2, respectively (for details, refer to Table 4-51).

*2: In addition to the configurations shown in Table 4-72, the Cutoff input buffers may be configured without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-73 Cutoff Cell Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVC MOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBBV#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBBV#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-55).

*2: In addition to the configurations shown in Table 4-73, the Cutoff bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.
Customers desiring to use such configurations should direct inquiries to Epson.

Table 4-74 N Channel Open Drain Cutoff Cell Bi-directional Buffers List

Input Level	Function	I _{OH} /I _{OL}	Cell Name ^{*1, *2}
LVCMOS	Bi-directional output for high speed	Type 1 Type 2 Type 3 Type 4	HBDV#ATX
	Bi-directional output for low noise	Type 1 Type 2 Type 3 Type 4	HBDV#BTX

Notes *1: The # denotes 1, 2, 3, or 4, with the I_{OH}/I_{OL} values corresponding to Type 1, Type 2, Type 3, and Type 4, respectively (for details, refer to Table 4-57).

*2: In addition to the configurations shown in Table 4-74, the Cutoff bi-directional buffers may be configured with pull-up/pull-down resistors or without test pins.

Customers desiring to use such configurations should direct inquiries to Epson.

4.6 Dual Power Supplies Guidelines

The S1K/S1X70000 series allows each input/output buffer to be interfaced with 3.3-V, 2.5-V, 1.8-V, or 1.5-V signals as desired, using a dual-power-supply system. The internal cell area operates using a 1.8-V or 1.5-V single power supply.

4.6.1 Method of Adapting to Dual Power Supplies

The S1K/S1X70000 series allows input/output buffers to be interfaced with the signals of voltages that differ from the internal operating voltage. There are two methods for interfacing with different power-supply voltages.

- For a single power supply

In a single-power-supply system, it is possible to apply input signals of voltages higher than the power supply voltage, using N channel open drain-type buffers or Fail Safe cells. However, high-voltage signals above the power-supply voltage cannot be output. This problem can be solved through the combined use of N channel open drain-type buffers and external pull-up resistors.

- For dual power supplies

By using input buffers designed exclusively for operation with dual power supplies, it is possible to apply input signals of voltages higher than the internal operating voltage. Similarly, high-voltage signals above the internal operating voltage can be output using dual-power-supply output buffers.

4.6.2 Power Supplies for Dual Power Operation

If your circuit is to be operated using two different power supplies, use two power-supply cells: HV_{DD} and LV_{DD} . Specifically, HV_{DD} may be used for HV_{DD} input/output buffers, and LV_{DD} may be used for LV_{DD} input/output buffers and internal cells.

The power-supply voltages must always satisfy the equation below.

$$HV_{DD} \geq LV_{DD}$$

If $HV_{DD} < LV_{DD}$, operation of the internal circuit cannot be guaranteed. The operating conditions specified below are recommended.

- * $HV_{DD} = 3.3 \text{ V}$, $LV_{DD} = 2.5 \text{ V}$
- * $HV_{DD} = 3.3 \text{ V}$, $LV_{DD} = 1.8 \text{ V}$
- * $HV_{DD} = 3.3 \text{ V}$, $LV_{DD} = 1.5 \text{ V}$

$$HV_{DD} = 2.5 \text{ V}, LV_{DD} = 1.8 \text{ V}$$

$$HV_{DD} = 2.5 \text{ V}, LV_{DD} = 1.5 \text{ V}$$

Those marked with * are effective only when 3.3-V (Y type) input/output buffers are used.

4.6.3 Turning On/Off Dual Power Supplies

For chips designed to dual-power-supply specifications, make sure the power is turned on and off in the order specified below.

When turning on: LV_{DD} (internal) → HV_{DD} (I/O section) → input signals applied

When turning off: Input signals off → HV_{DD} (I/O section) → LV_{DD} (internal)

Note 1: Avoid keeping only HV_{DD} turned on (for 10 sec or more) while LV_{DD} is turned off, so as not to degrade the chip's reliability.

Note 2: When turning HV_{DD} back on after it was off, always be sure to initialize the circuit following power-on. This is necessary to ensure the internal-circuit state in the event of power-supply noise or the like.

Chapter 5 Memory Blocks

The S1K/S1X70000 supports memory blocks. The types and features of the memory blocks are described in this chapter.

5.1 Basic Cell-Type RAM

The Basic Cell-type RAM comes in two types: clock-synchronized 1-port RAM and clock-synchronized 2-port RAM. The chip-select, write-enable, address, and data-input parts contain a latch circuit, making the RAM capable of the clock-synchronized, high-speed operation.

5.1.1 Features

- Available as clock-synchronized 1-port RAM or clock-synchronized 2-port RAM
- The chip-select, write-enable, address, and data-input parts contain a latch circuit, making the RAM capable of the clock-synchronized, high-speed operation.
- The data-input port and data-output port are separate.
- The data-output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.
- The RAM can be configured with 16 words to 256 words in 4-word increments, with word sizes ranging from 1 bit to 32 bits in 1-bit increments.
- Maximum configuration: 8k bits per module
- Libraries using three types of transistors are available: Standard-1, High-Performance, and Low-Leakage types.

5.1.2 Word/Bit Configurations of RAM and Cell Names

The delay parameters of the clock-synchronized RAM vary depending on the word/bit configurations. Therefore, cells are available separately for each word/bit configuration. When using clock-synchronized RAM, please provide Epson with information on whether you are using 1-port or 2-port RAM and how its word and bit are configured.

Tables 5-1 through 5-6 list the cell names corresponding to the typical word/bit configurations of 1-port and 2-port RAMs. RAMs are assigned cell names according to their word/bit configurations.

For any RAM that exceeds the possible configuration range, use two or more pieces of RAM in combination to obtain the desired configuration.

(1) For Standard-1 type

1-port RAM “L1J XXX YY”

2-port RAM “L1K XXX YY” XXX denotes the number of words (hexadecimal)
and YY denotes the number of bits (hexadecimal).

Table 5-1 Relationship between Word/Bit Configurations of 1-port RAM (Standard 1)
and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L1J04008	L1J08008	L1J0C008	L1J10008
16 Bit	L1J04010	L1J08010	L1J0C010	L1J10010
24 Bit	L1J04018	L1J08018	L1J0C018	L1J10018
32 Bit	L1J04020	L1J08020	L1J0C020	L1J10020

Table 5-2 Relationship between Word/Bit Configurations of 2-port RAM (Standard 1)
and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L1K04008	L1K08008	L1K0C008	L1K10008
16 Bit	L1K04010	L1K08010	L1K0C010	L1K10010
24 Bit	L1K04018	L1K08018	L1K0C018	L1K10018
32 Bit	L1K04020	L1K08020	L1K0C020	L1K10020

(2) For High-Performance type

1-port RAM “L2J XXX YY”

2-port RAM “L2K XXX YY” XXX denotes the number of words (hexadecimal)
and YY denotes the number of bits (hexadecimal).

Table 5-3 Relationship between Word/Bit Configurations of 1-port RAM (High-Performance)
and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L2J04008	L2J08008	L2J0C008	L2J10008
16 Bit	L2J04010	L2J08010	L2J0C010	L2J10010
24 Bit	L2J04018	L2J08018	L2J0C018	L2J10018
32 Bit	L2J04020	L2J08020	L2J0C020	L2J10020

Table 5-4 Relationship between Word/Bit Configurations of 2-port RAM (High-Performance)
and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L2K04008	L2K08008	L2K0C008	L2K10008
16 Bit	L2K04010	L2K08010	L2K0C010	L2K10010
24 Bit	L2K04018	L2K08018	L2K0C018	L2K10018
32 Bit	L2K04020	L2K08020	L2K0C020	L2K10020

(3) For Low-Leakage type

1-port RAM “L3J XXX YY”

2-port RAM “L3K XXX YY” XXX denotes the number of words (hexadecimal) and YY denotes the number of bits (hexadecimal).

Table 5-5 Relationship between Word/Bit Configurations of 1-port RAM (Low-Leakage) and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L3J04008	L3J08008	L3J0C008	L3J10008
16 Bit	L3J04010	L3J08010	L3J0C010	L3J10010
24 Bit	L3J04018	L3J08018	L3J0C018	L3J10018
32 Bit	L3J04020	L3J08020	L3J0C020	L3J10020

Table 5-6 Relationship between Word/Bit Configurations of 2-port RAM (Low-Leakage) and Cell Names

	64 Word	128 Word	192 Word	256 Word
8 Bit	L3K04008	L3K08008	L3K0C008	L3K10008
16 Bit	L3K04010	L3K08010	L3K0C010	L3K10010
24 Bit	L3K04018	L3K08018	L3K0C018	L3K10018
32 Bit	L3K04020	L3K08020	L3K0C020	L3K10020

5.1.3 RAM Sizes

To calculate the RAM sizes in the X and Y directions and the number of basic cells used, use the respective equations shown below. Note that the equations shown below apply to all types of transistors: Standard 1, High-Performance, and Low-Leakage.

(1) 1-port RAM

Size in X direction : $RX = (\text{number of words} / 4) \times 7 + 35$

Size in Y direction : $RY = \text{number of bits} \times 2 + 9 + \alpha$

Number of basic cells : $RAMBCS = RX \times RY$

The factor α is 3 when $16 \leq \text{number of words} \leq 32$, or 4 when $36 \leq \text{number of words} \leq 256$.

Table 5-7 Typical Configurations of 1-port RAM and Number of Basic Cells

	64 Word	128 Word	192 Word	256 Word
8 Bit	4263 (147 x 29)	7511 (259 x 29)	10759 (371 x 29)	14007 (483 x 29)
16 Bit	6615 (147 x 45)	11655 (259 x 45)	16695 (371 x 45)	21735 (483 x 45)
24 Bit	8967 (147 x 61)	15799 (259 x 61)	22631 (371 x 61)	29463 (483 x 61)
32 Bit	11319 (147 x 77)	19943 (259 x 77)	28567 (371 x 77)	37191 (483 x 77)

(2) 2-port RAM

Size in X direction : $RX = (\text{number of words} / 4) \times 7 + 32$ Size in Y direction : $RY = \text{number of bits} \times 2 + 9 + \alpha$ Number of basic cells : $RAMBCS = RX \times RY$ The factor α is 4 when $16 \leq \text{number of words} \leq 32$, or 6 when $36 \leq \text{number of words} \leq 256$.**Table 5-8** Typical Configurations of 2-port RAM and Number of Basic Cells

	64 Word	128 Word	192 Word	256 Word
8 Bit	4464 (144 x 31)	7936 (256 x 31)	11408 (368 x 31)	14880 (480 x 31)
16 Bit	6768 (144 x 47)	12032 (256 x 47)	17296 (368 x 47)	22560 (480 x 47)
24 Bit	9072 (144 x 63)	16128 (256 x 63)	23184 (368 x 63)	30240 (480 x 63)
32 Bit	11376 (144 x 79)	20224 (256 x 79)	29072 (368 x 79)	37920 (480 x 79)

5.1.4 Functional Description**5.1.4.1 1-port RAM**

(1) Input/output signals and block diagrams

Table 5-9 Description of 1-port RAM Signals

Input/Output Signal		Functional Description
Symbol	Name	
CK	Clock input	Chip select (XCS), write enable (XWE), address input (A0–An), and data input (D0–Dn) are latched into the RAM on the rising edge (Low-to-High transition) of the clock input (CK).
XCS	Chip select	Latched into the rising edge of the clock input (CK). Memory is activated when the latched value is Low.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
A0–An	Address input	Latched into the rising edge of the clock input (CK).
D0–Dn	Data input	Latched into the rising edge of the clock input (CK). When write enable (XWE) is Low, the data is written to memory cells.
Y0–Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the write data is forwarded to these pins synchronously with CK. Therefore, make sure the previously read data is not retained at these pins before writing.

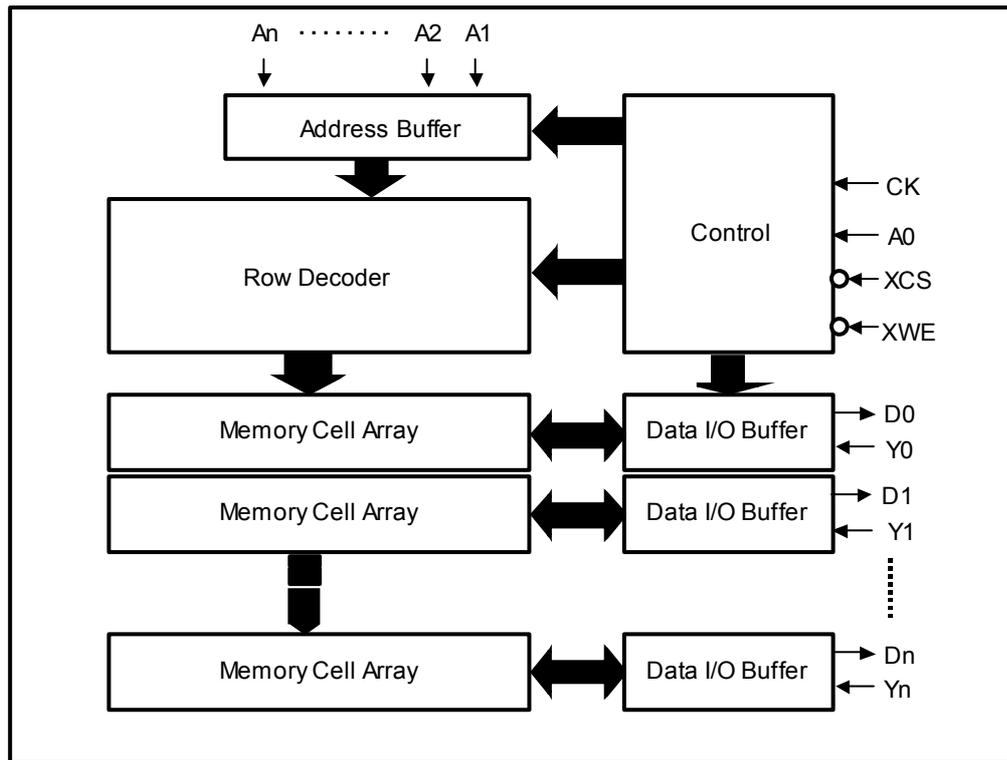


Figure 5-1 Block Diagram of 1-port RAM

(2) Device operation

For writing, assert chip select (XCS) and write enable (XWE) (by pulling them Low), and set the address inputs (A0–An) and data inputs (D0–Dn) before the clock input (CK) goes High. All of the chip-select, write-enable, address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. The write data is output from the data-output pins (Y0–Yn) until the next rise of the clock input.

For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0–An) before the clock input (CK) goes High. All of the chip-select, write-enable, and address-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y0–Yn) a finite access time after the rise of the clock.

Table 5-10 Truth Table for 1-port RAM Operation

CK	XCS	XWE	Output State	Operation Mode
L → H	L	H	Read Data	Read
L → H	L	L	Write Data	Write
L → H	H	L or H	Data Hold	Standby

5.1.4.2 2-port RAM

(1) Output signals and block diagrams

Ports 1 and 2 are used exclusively for writing and reading, respectively. Each port comes equipped with a clock input pin, allowing them to be operated with different frequencies or timing independently of each other.

Be aware that no memory cells can be accessed from two ports at the same time.

If write enable (XWA) for port 1 and read enable (XRB) for port 2 are both latched High, the RAM is in standby state.

Table 5-11 Description of 2-port RAM Signals

Signals for port 1 (write-only)

Input/Output Signal		Functional Description
Symbol	Name	
CKA	Clock input	Write enable (XWA), address input (AA0–AA _n), and data input (D0–D _n) are latched into the RAM on the rising edge (Low-to-High transition) of the clock input (CKA).
XWA	Write enable	Latched into the rising edge of the clock input (CKA). When the latched value is Low, memory is activated for write operation.
AA0–AA _n	Address input	Latched into the rising edge of the clock input (CKA).
D0–D _n	Data input	Latched into the rising edge of the clock input (CKA). When write enable (XWA) is Low, data is written to the memory cells.

Signals for port 2 (read-only)

Input/Output Signal		Functional Description
Symbol	Name	
CKB	Clock input	Read enable (XRB) and address input (AB0–AB _n) are latched into the RAM on the rising edge (Low-to-High transition) of the clock input (CKB).
XRB	Read enable	Latched into the rising edge of the clock input (CKB). When the latched value is Low, memory is activated for read operation.
AB0–AB _n	Address input	Latched into the rising edge of the clock input (CKB).
Y0–Y _n	Data output	The data from memory cells is output a finite access time after the rising edge of the clock input (CKB).

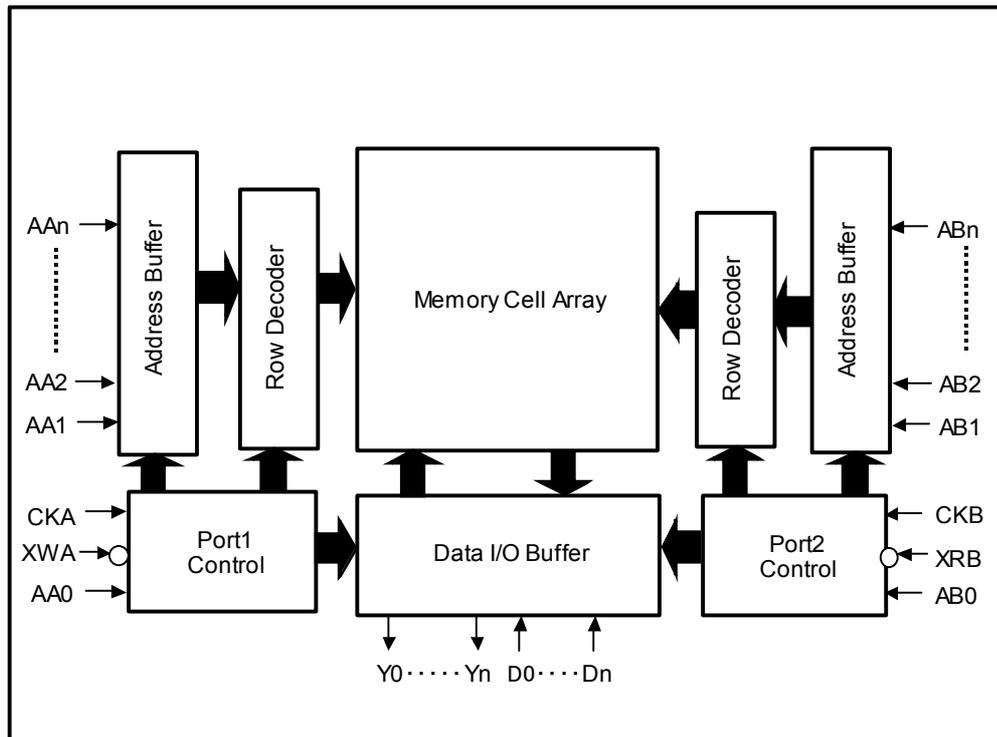


Figure 5-2 Block Diagram of 2-port RAM

(2) Device operation

For writing, assert write enable (XWA) (by pulling it Low), and set the address inputs (AA0–AAn) and data inputs (D0–Dn) before the clock input (CKA) goes High. All of the write-enable (XWA), address-input (AA0–AAn), and data-input (D0–Dn) signals are latched into the rising edge of the clock input (CKA), at which time memory is activated for write operation.

For reading, assert read enable (XRB) (by pulling it Low), and set the address inputs (AB0–ABn) before the clock input (CKB) goes High. All of the read-enable (XRB) and address-input (AB0–ABn) signals are latched into the rising edge of the clock input (CKB), at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y0–Yn) a finite access time after the rise of the clock (CKB).

Table 5-12 Truth Table of 2-port RAM Operation

Truth table for port 1 (write-only)

CKA	XWA	Operation Mode
L → H	H	Standby
L → H	L	Write

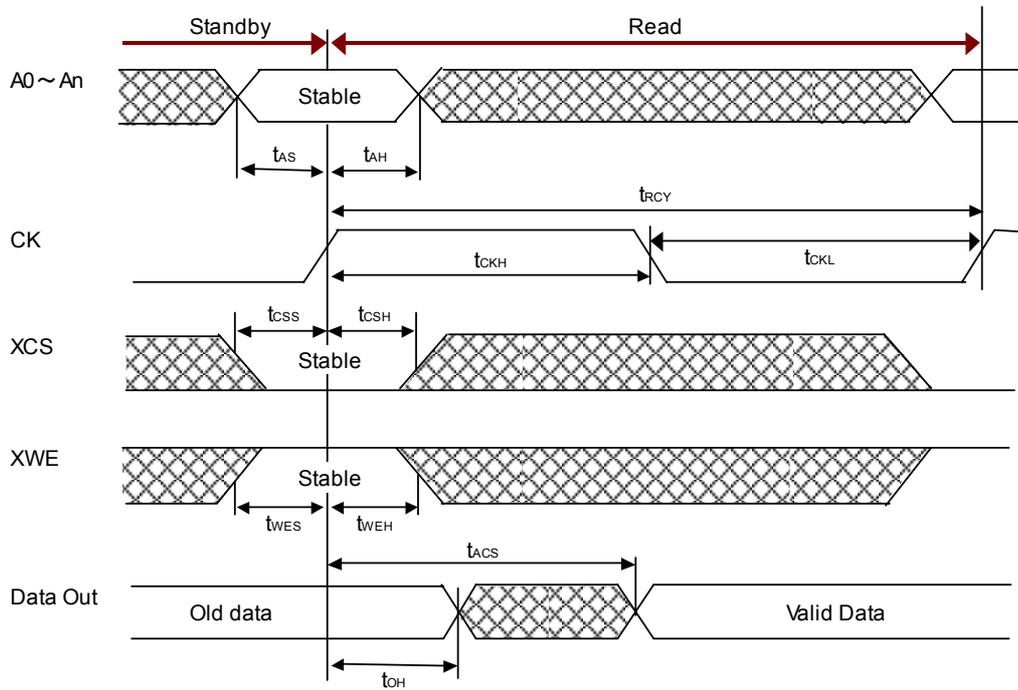
Truth table for port 2 (read-only)

CKB	XRB	Output State	Operation Mode
L → H	H	Data Hold	Standby
L → H	L	Read Data	Read

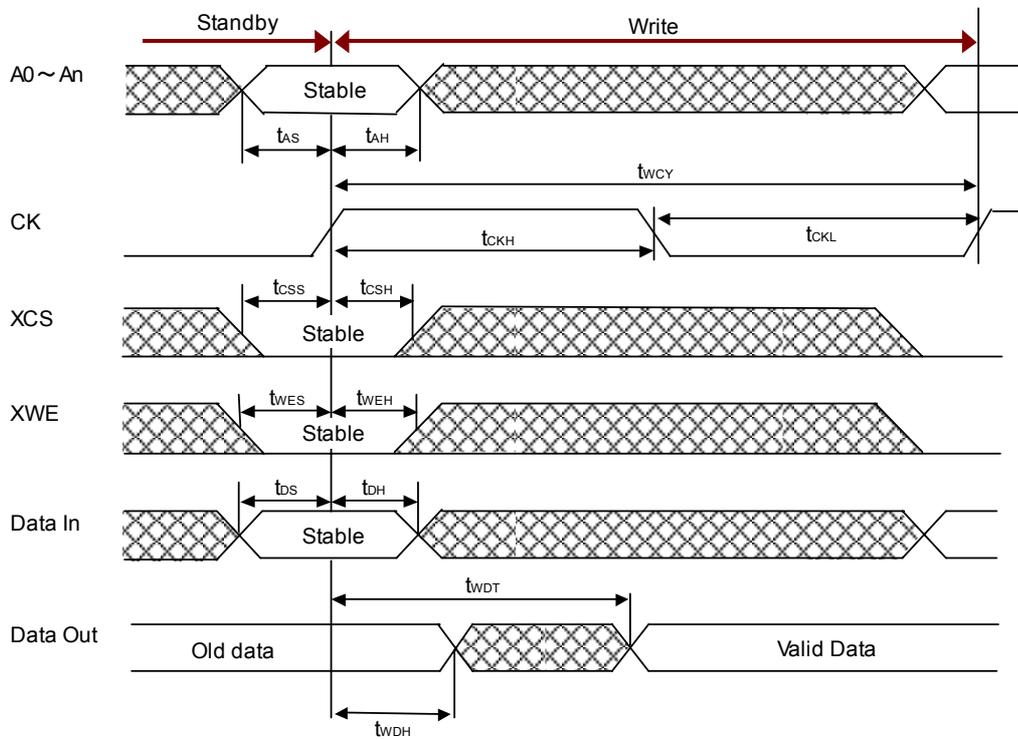
5.1.5 Timing Charts

(1) 1-port RAM

- During reading

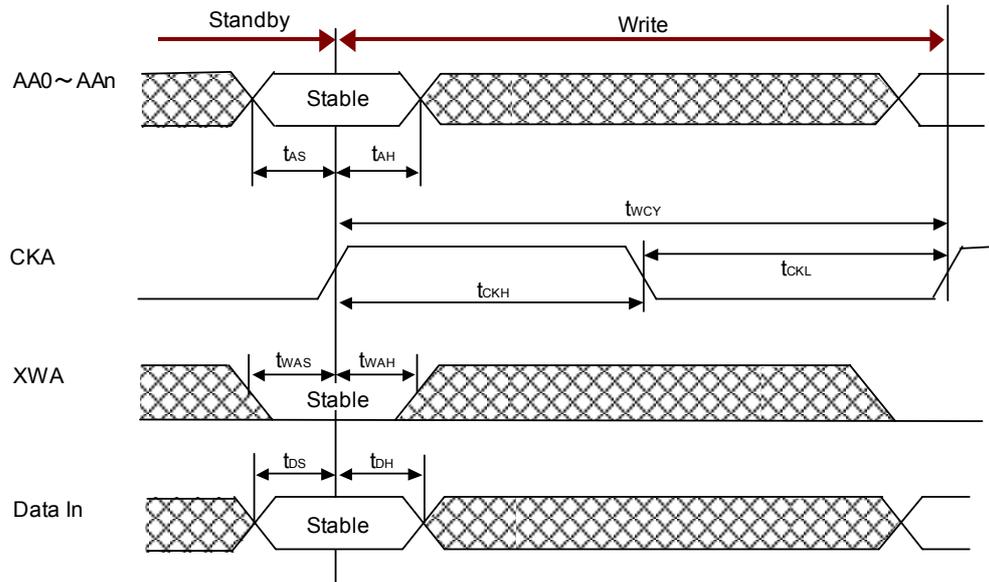


- During writing

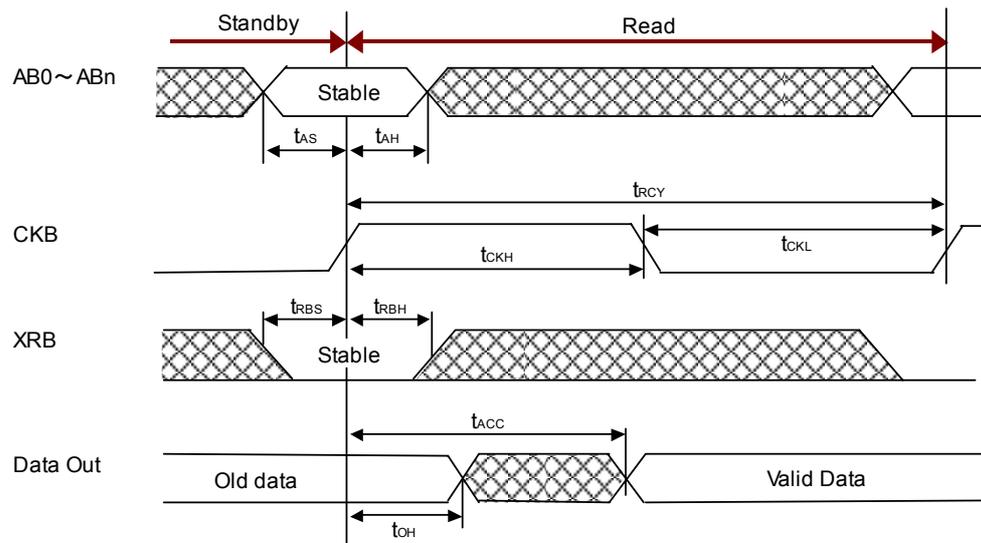


(2) 2-port RAM

• Port 1



• Port 2



5.1.6 Delay Parameters

5.1.6.1 Delay Parameters

(1) Delay parameters for Standard-1 type

1) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 64-word

Table 5-13 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	4.788	—	4.876	—	4.974	—	5.090	ns
Read-Cycle Time	t_{RCY}	4.788	—	4.876	—	4.974	—	5.090	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.681	—	0.695	—	0.709	—	0.721	—	

Table 5-14 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.145	—	4.258	—	4.404	—	4.548	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.330	—	1.380	—	1.428	—	1.471	—	
Write-Data Through Time	t_{WDT}	—	4.145	—	4.258	—	4.404	—	4.548	

2) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-15 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	6.240	—	6.336	—	6.421	—	6.497	ns
Read-Cycle Time	t_{RCY}	6.240	—	6.336	—	6.421	—	6.497	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.685	—	0.700	—	0.715	—	0.727	—	

Table 5-16 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.191	—	4.314	—	4.450	—	4.592	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.377	—	1.424	—	1.471	—	1.517	—	
Write-Data Through Time	t_{WDT}	—	4.191	—	4.314	—	4.450	—	4.592	

3) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = -40^\circ C$ to $+85^\circ C$) 192-word

Table 5-17 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.627	—	7.711	—	7.797	—	7.892	ns
Read-Cycle Time	t_{RCY}	7.627	—	7.711	—	7.797	—	7.892	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.697	—	0.709	—	0.725	—	0.737	—	

Table 5-18 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.235	—	4.371	—	4.494	—	4.638	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.405	—	1.461	—	1.505	—	1.551	—	
Write-Data Through Time	t_{WDT}	—	4.235	—	4.371	—	4.494	—	4.638	

4) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word**Table 5-19** 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	8.862	—	8.954	—	9.033	—	9.130	ns
Read-Cycle Time	t_{RCY}	8.862	—	8.954	—	9.033	—	9.130	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.699	—	0.713	—	0.731	—	0.742	—	

Table 5-20 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.281	—	4.427	—	4.540	—	4.684	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.424	—	1.485	—	1.525	—	1.570	—	
Write-Data Through Time	t_{WDT}	—	4.281	—	4.427	—	4.540	—	4.684	

5) 1.8-V specification ($V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 64-word

Table 5-21 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	4.608	—	4.693	—	4.788	—	4.900	ns
Read-Cycle Time	t_{RCY}	4.608	—	4.693	—	4.788	—	4.900	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.711	—	0.725	—	0.740	—	0.752	—	

Table 5-22 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.990	—	4.098	—	4.239	—	4.378	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.388	—	1.440	—	1.491	—	1.535	—	
Write-Data Through Time	t_{WDT}	—	3.990	—	4.098	—	4.239	—	4.378	

6) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-23 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	6.006	—	6.099	—	6.180	—	6.253	ns
Read-Cycle Time	t_{RCY}	6.006	—	6.099	—	6.180	—	6.253	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.715	—	0.730	—	0.746	—	0.759	—	

Table 5-24 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.034	—	4.152	—	4.283	—	4.420	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.437	—	1.486	—	1.535	—	1.583	—	
Write-Data Through Time	t_{WDT}	—	4.034	—	4.152	—	4.283	—	4.420	

7) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 192-word

Table 5-25 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.341	—	7.422	—	7.505	—	7.596	ns
Read-Cycle Time	t_{RCY}	7.341	—	7.422	—	7.505	—	7.596	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.727	—	0.740	—	0.757	—	0.769	—	

Table 5-26 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.076	—	4.207	—	4.325	—	4.464	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.466	—	1.524	—	1.571	—	1.619	—	
Write-Data Through Time	t_{WDT}	—	4.076	—	4.207	—	4.325	—	4.464	

8) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word

Table 5-27 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	8.530	—	8.618	—	8.694	—	8.787	ns
Read-Cycle Time	t_{RCY}	8.530	—	8.618	—	8.694	—	8.787	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.730	—	0.744	—	0.763	—	0.774	—	

Table 5-28 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	4.120	—	4.261	—	4.369	—	4.508	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.486	—	1.550	—	1.592	—	1.638	—	
Write-Data Through Time	t_{WDT}	—	4.120	—	4.261	—	4.369	—	4.508	

9) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 64-word

Table 5-29 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.639	—	7.757	—	7.899	—	8.058	ns
Read-Cycle Time	t_{RCY}	7.639	—	7.757	—	7.899	—	8.058	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.944	—	0.961	—	0.990	—	1.002	—	

Table 5-30 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.153	—	6.363	—	6.560	—	6.743	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	1.833	—	1.900	—	1.945	—	2.001	—	
Write-Data Through Time	t_{WDT}	—	6.153	—	6.363	—	6.560	—	6.743	

10) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-31 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	10.349	—	10.467	—	10.603	—	10.722	ns
Read-Cycle Time	t_{RCY}	10.349	—	10.467	—	10.603	—	10.722	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.959	—	0.977	—	1.005	—	1.014	—	

Table 5-32 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.271	—	6.486	—	6.687	—	6.868	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	1.891	—	1.954	—	2.003	—	2.102	—	
Write-Data Through Time	t_{WDT}	—	6.271	—	6.486	—	6.687	—	6.868	

11) 1.5-V specification ($V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 192-word

Table 5-33 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	12.822	—	12.949	—	13.063	—	13.186	ns
Read-Cycle Time	t_{RCY}	12.822	—	12.949	—	13.063	—	13.186	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.975	—	0.992	—	1.021	—	1.025	—	

Table 5-34 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.365	—	6.581	—	6.769	—	6.952	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	1.948	—	2.008	—	2.061	—	2.202	—	
Write-Data Through Time	t_{WDT}	—	6.365	—	6.581	—	6.769	—	6.952	

12) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word

Table 5-35 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	15.001	—	15.103	—	15.230	—	15.353	ns
Read-Cycle Time	t_{RCY}	15.001	—	15.103	—	15.230	—	15.353	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.990	—	1.008	—	1.036	—	1.037	—	

Table 5-36 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.432	—	6.632	—	6.826	—	7.011	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	2.006	—	2.062	—	2.118	—	2.302	—	
Write-Data Through Time	t_{WDT}	—	6.432	—	6.632	—	6.826	—	7.011	

13) 1.5-V specification ($V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 64-word

Table 5-37 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.448	—	7.563	—	7.702	—	7.856	ns
Read-Cycle Time	t_{RCY}	7.448	—	7.563	—	7.702	—	7.856	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.986	—	1.004	—	1.035	—	1.047	—	

Table 5-38 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J04008/L1K04008		L1J04010/L1K04010		L1J04018/L1K04018		L1J04020/L1K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.000	—	6.204	—	6.396	—	6.574	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	1.915	—	1.985	—	2.032	—	2.091	—	
Write-Data Through Time	t_{WDT}	—	6.000	—	6.204	—	6.396	—	6.574	

14) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-39 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	10.091	—	10.206	—	10.338	—	10.454	ns
Read-Cycle Time	t_{RCY}	10.091	—	10.206	—	10.338	—	10.454	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.002	—	1.021	—	1.050	—	1.059	—	

Table 5-40 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J08008/L1K08008		L1J08010/L1K08010		L1J08018/L1K08018		L1J08020/L1K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.115	—	6.324	—	6.520	—	6.696	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	1.975	—	2.041	—	2.092	—	2.196	—	
Write-Data Through Time	t_{WDT}	—	6.115	—	6.324	—	6.520	—	6.696	

15) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 192-word

Table 5-41 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	12.502	—	12.625	—	12.737	—	12.857	ns
Read-Cycle Time	t_{RCY}	12.502	—	12.625	—	12.737	—	12.857	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.018	—	1.036	—	1.067	—	1.071	—	

Table 5-42 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J0C008/L1K0C008		L1J0C010/L1K0C010		L1J0C018/L1K0C018		L1J0C020/L1K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.206	—	6.417	—	6.600	—	6.779	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	2.036	—	2.098	—	2.153	—	2.301	—	
Write-Data Through Time	t_{WDT}	—	6.206	—	6.417	—	6.600	—	6.779	

16) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word**Table 5-43** 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	14.626	—	14.725	—	14.849	—	14.969	ns
Read-Cycle Time	t_{RCY}	14.626	—	14.725	—	14.849	—	14.969	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.700	—	1.700	—	1.700	—	1.700	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.034	—	1.053	—	1.082	—	1.083	—	

Table 5-44 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L1J10008/L1K10008		L1J10010/L1K10010		L1J10018/L1K10018		L1J10020/L1K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.271	—	6.466	—	6.655	—	6.835	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.700	—	1.700	—	1.700	—	1.700	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Setup Time	t_{WES}	1.700	—	1.700	—	1.700	—	1.700	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.700	—	1.700	—	1.700	—	1.700	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.700	—	1.700	—	1.700	—	1.700	—	
Write-Data Hold Time	t_{WDH}	2.096	—	2.154	—	2.213	—	2.405	—	
Write-Data Through Time	t_{WDT}	—	6.271	—	6.466	—	6.655	—	6.835	

(2) Delay parameters for the High-Performance type

1) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 64-word

Table 5-45 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	3.086	—	3.144	—	3.212	—	3.283	ns
Read-Cycle Time	t_{RCY}	3.086	—	3.144	—	3.212	—	3.283	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.455	—	0.462	—	0.471	—	0.476	—	

Table 5-46 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.896	—	3.003	—	3.109	—	3.214	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	0.958	—	0.979	—	1.004	—	1.021	—	
Write-Data Through Time	t_{WDT}	—	2.896	—	3.003	—	3.109	—	3.214	

2) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-47 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	3.976	—	4.038	—	4.092	—	4.154	ns
Read-Cycle Time	t_{RCY}	3.976	—	4.038	—	4.092	—	4.154	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.460	—	0.468	—	0.476	—	0.484	—	

Table 5-48 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.970	—	3.072	—	3.168	—	3.271	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	0.983	—	1.004	—	1.027	—	1.047	—	
Write-Data Through Time	t_{WDT}	—	2.970	—	3.072	—	3.168	—	3.271	

3) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 192-word

Table 5-49 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	4.805	—	4.883	—	4.927	—	4.985	ns
Read-Cycle Time	t_{RCY}	4.805	—	4.883	—	4.927	—	4.985	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.471	—	0.477	—	0.484	—	0.489	—	

Table 5-50 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.003	—	3.102	—	3.198	—	3.292	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	0.998	—	1.021	—	1.040	—	1.062	—	
Write-Data Through Time	t_{WDT}	—	3.003	—	3.102	—	3.198	—	3.292	

4) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word**Table 5-51** 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	5.536	—	5.596	—	5.647	—	5.703	ns
Read-Cycle Time	t_{RCY}	5.536	—	5.596	—	5.647	—	5.703	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.471	—	0.478	—	0.485	—	0.491	—	

Table 5-52 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.017	—	3.110	—	3.211	—	3.311	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	1.009	—	1.033	—	1.049	—	1.073	—	
Write-Data Through Time	t_{WDT}	—	3.017	—	3.110	—	3.211	—	3.311	

5) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 64-word

Table 5-53 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	2.970	—	3.026	—	3.092	—	3.160	ns
Read-Cycle Time	t_{RCY}	2.970	—	3.026	—	3.092	—	3.160	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.474	—	0.482	—	0.492	—	0.497	—	

Table 5-54 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.787	—	2.890	—	2.992	—	3.094	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	0.999	—	1.021	—	1.047	—	1.065	—	
Write-Data Through Time	t_{WDT}	—	2.787	—	2.890	—	2.992	—	3.094	

6) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-55 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	3.827	—	3.887	—	3.939	—	3.998	ns
Read-Cycle Time	t_{RCY}	3.827	—	3.887	—	3.939	—	3.998	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.480	—	0.488	—	0.497	—	0.505	—	

Table 5-56 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.858	—	2.957	—	3.050	—	3.148	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	1.026	—	1.048	—	1.071	—	1.093	—	
Write-Data Through Time	t_{WDT}	—	2.858	—	2.957	—	3.050	—	3.148	

7) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 192-word

Table 5-57 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	4.625	—	4.700	—	4.742	—	4.798	ns
Read-Cycle Time	t_{RCY}	4.625	—	4.700	—	4.742	—	4.798	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.491	—	0.498	—	0.505	—	0.511	—	

Table 5-58 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.890	—	2.985	—	3.078	—	3.168	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	1.041	—	1.065	—	1.085	—	1.108	—	
Write-Data Through Time	t_{WDT}	—	2.890	—	2.985	—	3.078	—	3.168	

8) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word

Table 5-59 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	5.328	—	5.386	—	5.435	—	5.489	ns
Read-Cycle Time	t_{RCY}	5.328	—	5.386	—	5.435	—	5.489	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.000	—	1.000	—	1.000	—	1.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.492	—	0.498	—	0.506	—	0.512	—	

Table 5-60 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	2.904	—	2.994	—	3.090	—	3.187	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.000	—	1.000	—	1.000	—	1.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Setup Time	t_{WES}	1.000	—	1.000	—	1.000	—	1.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.000	—	1.000	—	1.000	—	1.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.000	—	1.000	—	1.000	—	1.000	—	
Write-Data Hold Time	t_{WDH}	1.053	—	1.078	—	1.095	—	1.119	—	
Write-Data Through Time	t_{WDT}	—	2.904	—	2.994	—	3.090	—	3.187	

9) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 64-word

Table 5-61 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	3.990	—	4.070	—	4.151	—	4.244	ns
Read-Cycle Time	t_{RCY}	3.990	—	4.070	—	4.151	—	4.244	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.550	—	0.568	—	0.580	—	0.593	—	

Table 5-62 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.570	—	3.689	—	3.809	—	3.929	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.131	—	1.158	—	1.186	—	1.213	—	
Write-Data Through Time	t_{WDT}	—	3.570	—	3.689	—	3.809	—	3.929	

10) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-63 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	5.192	—	5.265	—	5.332	—	5.414	ns
Read-Cycle Time	t_{RCY}	5.192	—	5.265	—	5.332	—	5.414	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.559	—	0.575	—	0.590	—	0.598	—	

Table 5-64 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J04008/L2K04008		L2J04010/L2K04010		L2J04018/L2K04018		L2J04020/L2K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.637	—	3.770	—	3.904	—	3.997	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.172	—	1.201	—	1.227	—	1.252	—	
Write-Data Through Time	t_{WDT}	—	3.637	—	3.770	—	3.904	—	3.997	

11) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 192-word

Table 5-65 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	6.331	—	6.405	—	6.477	—	6.549	ns
Read-Cycle Time	t_{RCY}	6.331	—	6.405	—	6.477	—	6.549	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.572	—	0.586	—	0.598	—	0.613	—	

Table 5-66 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.677	—	3.825	—	3.943	—	4.045	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.197	—	1.224	—	1.250	—	1.276	—	
Write-Data Through Time	t_{WDT}	—	3.677	—	3.825	—	3.943	—	4.045	

12) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word

Table 5-67 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.347	—	7.408	—	7.489	—	7.556	ns
Read-Cycle Time	t_{RCY}	7.347	—	7.408	—	7.489	—	7.556	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.574	—	0.588	—	0.600	—	0.615	—	

Table 5-68 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.696	—	3.830	—	3.964	—	4.064	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.216	—	1.237	—	1.265	—	1.291	—	
Write-Data Through Time	t_{WDT}	—	3.696	—	3.830	—	3.964	—	4.064	

13) 1.5-V specification ($V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 64-word

Table 5-69 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	3.891	—	3.968	—	4.047	—	4.138	ns
Read-Cycle Time	t_{RCY}	3.891	—	3.968	—	4.047	—	4.138	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.575	—	0.594	—	0.606	—	0.620	—	

Table 5-70 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J08008/L2K08008		L2J08010/L2K08010		L2J08018/L2K08018		L2J08020/L2K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.481	—	3.597	—	3.714	—	3.831	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.182	—	1.210	—	1.239	—	1.267	—	
Write-Data Through Time	t_{WDT}	—	3.481	—	3.597	—	3.714	—	3.831	

14) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-71 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	5.063	—	5.133	—	5.198	—	5.279	ns
Read-Cycle Time	t_{RCY}	5.063	—	5.133	—	5.198	—	5.279	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.584	—	0.601	—	0.616	—	0.625	—	

Table 5-72 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J0C008/L2K0C008		L2J0C010/L2K0C010		L2J0C018/L2K0C018		L2J0C020/L2K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.546	—	3.676	—	3.807	—	3.898	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.224	—	1.255	—	1.282	—	1.308	—	
Write-Data Through Time	t_{WDT}	—	3.546	—	3.676	—	3.807	—	3.898	

15) 1.5-V specification ($V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 192-word

Table 5-73 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	6.173	—	6.245	—	6.315	—	6.386	ns
Read-Cycle Time	t_{RCY}	6.173	—	6.245	—	6.315	—	6.386	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.597	—	0.612	—	0.625	—	0.640	—	

Table 5-74 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.585	—	3.729	—	3.844	—	3.944	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.251	—	1.279	—	1.306	—	1.333	—	
Write-Data Through Time	t_{WDT}	—	3.585	—	3.729	—	3.844	—	3.944	

16) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word

Table 5-75 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	7.163	—	7.223	—	7.302	—	7.367	ns
Read-Cycle Time	t_{RCY}	7.163	—	7.223	—	7.302	—	7.367	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	1.200	—	1.200	—	1.200	—	1.200	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	0.599	—	0.614	—	0.627	—	0.643	—	

Table 5-76 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L2J10008/L2K10008		L2J10010/L2K10010		L2J10018/L2K10018		L2J10020/L2K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	3.604	—	3.735	—	3.865	—	3.963	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	1.200	—	1.200	—	1.200	—	1.200	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Setup Time	t_{WES}	1.200	—	1.200	—	1.200	—	1.200	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	1.200	—	1.200	—	1.200	—	1.200	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	1.200	—	1.200	—	1.200	—	1.200	—	
Write-Data Hold Time	t_{WDH}	1.271	—	1.293	—	1.322	—	1.348	—	
Write-Data Through Time	t_{WDT}	—	3.604	—	3.735	—	3.865	—	3.963	

(3) Delay parameters for the Low-Leakage type

1) 1.8-V specification ($V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 64-word

Table 5-77 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	8.772	—	8.950	—	9.128	—	9.305	ns
Read-Cycle Time	t_{RCY}	8.772	—	8.950	—	9.128	—	9.305	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.228	—	1.250	—	1.277	—	1.300	—	

Table 5-78 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.279	—	7.512	—	7.748	—	7.983	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.406	—	2.497	—	2.574	—	2.654	—	
Write-Data Through Time	t_{WDT}	—	7.279	—	7.512	—	7.748	—	7.983	

2) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-79 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	11.837	—	11.980	—	12.132	—	12.275	ns
Read-Cycle Time	t_{RCY}	11.837	—	11.980	—	12.132	—	12.275	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.231	—	1.257	—	1.281	—	1.307	—	

Table 5-80 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.414	—	7.585	—	7.857	—	8.032	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.478	—	2.565	—	2.646	—	2.725	—	
Write-Data Through Time	t_{WDT}	—	7.414	—	7.585	—	7.857	—	8.032	

3) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = -40^\circ C$ to $+85^\circ C$) 192-word

Table 5-81 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	14.544	—	14.689	—	14.838	—	14.983	ns
Read-Cycle Time	t_{RCY}	14.544	—	14.689	—	14.838	—	14.983	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.272	—	1.297	—	1.317	—	1.344	—	

Table 5-82 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.428	—	7.658	—	7.867	—	8.063	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.562	—	2.634	—	2.710	—	2.782	—	
Write-Data Through Time	t_{WDT}	—	7.428	—	7.658	—	7.867	—	8.063	

4) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word

Table 5-83 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	17.341	—	17.480	—	17.618	—	17.757	ns
Read-Cycle Time	t_{RCY}	17.341	—	17.480	—	17.618	—	17.757	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.291	—	1.314	—	1.337	—	1.360	—	

Table 5-84 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.512	—	7.734	—	7.948	—	8.168	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.623	—	2.698	—	2.775	—	2.844	—	
Write-Data Through Time	t_{WDT}	—	7.512	—	7.734	—	7.948	—	8.168	

5) 1.8-V specification ($V_{DD} = 1.8 V \pm 0.15 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 64-word

Table 5-85 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	8.424	—	8.594	—	8.765	—	8.936	ns
Read-Cycle Time	t_{RCY}	8.424	—	8.594	—	8.765	—	8.936	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.281	—	1.304	—	1.332	—	1.356	—	

Table 5-86 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	6.990	—	7.213	—	7.441	—	7.666	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.511	—	2.605	—	2.686	—	2.770	—	
Write-Data Through Time	t_{WDT}	—	6.990	—	7.213	—	7.441	—	7.666	

6) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-87 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	11.366	—	11.504	—	11.650	—	11.788	ns
Read-Cycle Time	t_{RCY}	11.366	—	11.504	—	11.650	—	11.788	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.284	—	1.312	—	1.337	—	1.363	—	

Table 5-88 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.119	—	7.284	—	7.545	—	7.713	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.586	—	2.677	—	2.761	—	2.843	—	
Write-Data Through Time	t_{WDT}	—	7.119	—	7.284	—	7.545	—	7.713	

7) 1.8-V specification ($V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 192-word

Table 5-89 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	13.966	—	14.106	—	14.249	—	14.388	ns
Read-Cycle Time	t_{RCY}	13.966	—	14.106	—	14.249	—	14.388	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.327	—	1.353	—	1.374	—	1.402	—	

Table 5-90 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.133	—	7.353	—	7.554	—	7.743	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.673	—	2.749	—	2.827	—	2.903	—	
Write-Data Through Time	t_{WDT}	—	7.133	—	7.353	—	7.554	—	7.743	

8) 1.8-V specification ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word

Table 5-91 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	16.652	—	16.785	—	16.918	—	17.051	ns
Read-Cycle Time	t_{RCY}	16.652	—	16.785	—	16.918	—	17.051	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.000	—	2.000	—	2.000	—	2.000	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.347	—	1.371	—	1.395	—	1.419	—	

Table 5-92 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	7.213	—	7.427	—	7.633	—	7.844	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.000	—	2.000	—	2.000	—	2.000	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Setup Time	t_{WES}	2.000	—	2.000	—	2.000	—	2.000	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.000	—	2.000	—	2.000	—	2.000	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.000	—	2.000	—	2.000	—	2.000	—	
Write-Data Hold Time	t_{WDH}	2.737	—	2.816	—	2.895	—	2.967	—	
Write-Data Through Time	t_{WDT}	—	7.213	—	7.427	—	7.633	—	7.844	

9) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 64-word

Table 5-93 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	14.298	—	14.588	—	14.878	—	15.168	ns
Read-Cycle Time	t_{RCY}	14.298	—	14.588	—	14.878	—	15.168	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.800	—	1.832	—	1.872	—	1.905	—	

Table 5-94 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	11.864	—	12.243	—	12.630	—	13.012	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.528	—	3.661	—	3.774	—	3.892	—	
Write-Data Through Time	t_{WDT}	—	11.864	—	12.243	—	12.630	—	13.012	

10) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 128-word

Table 5-95 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	19.294	—	19.526	—	19.776	—	20.008	ns
Read-Cycle Time	t_{RCY}	19.294	—	19.526	—	19.776	—	20.008	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.804	—	1.843	—	1.878	—	1.916	—	

Table 5-96 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	12.084	—	12.363	—	12.807	—	13.093	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.634	—	3.762	—	3.880	—	3.995	—	
Write-Data Through Time	t_{WDT}	—	12.084	—	12.363	—	12.807	—	13.093	

11) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = -40^{\circ}C$ to $+85^{\circ}C$) 192-word

Table 5-97 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	23.707	—	23.943	—	24.186	—	24.422	ns
Read-Cycle Time	t_{RCY}	23.707	—	23.943	—	24.186	—	24.422	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.864	—	1.901	—	1.931	—	1.970	—	

Table 5-98 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	12.108	—	12.482	—	12.823	—	13.142	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.756	—	3.863	—	3.973	—	4.079	—	
Write-Data Through Time	t_{WDT}	—	12.108	—	12.482	—	12.823	—	13.142	

12) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 256-word

Table 5-99 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	28.266	—	28.492	—	28.717	—	28.943	ns
Read-Cycle Time	t_{RCY}	28.266	—	28.492	—	28.717	—	28.943	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.893	—	1.926	—	1.960	—	1.994	—	

Table 5-100 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	12.243	—	12.606	—	12.956	—	13.314	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.846	—	3.957	—	4.069	—	4.170	—	
Write-Data Through Time	t_{WDT}	—	12.243	—	12.606	—	12.956	—	13.314	

13) 1.5-V specification ($V_{DD} = 1.5 V \pm 0.1 V$, $T_a = 0^\circ C$ to $+70^\circ C$) 64-word

Table 5-101 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	13.920	—	14.202	—	14.484	—	14.766	ns
Read-Cycle Time	t_{RCY}	13.920	—	14.202	—	14.484	—	14.766	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.880	—	1.915	—	1.955	—	1.991	—	

Table 5-102 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J04008/L3K04008		L3J04010/L3K04010		L3J04018/L3K04018		L3J04020/L3K04020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	11.550	—	11.919	—	12.295	—	12.668	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.686	—	3.825	—	3.943	—	4.066	—	
Write-Data Through Time	t_{WDT}	—	11.550	—	11.919	—	12.295	—	12.668	

14) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 128-word

Table 5-103 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	18.783	—	19.009	—	19.252	—	19.478	ns
Read-Cycle Time	t_{RCY}	18.783	—	19.009	—	19.252	—	19.478	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.885	—	1.926	—	1.962	—	2.001	—	

Table 5-104 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J08008/L3K08008		L3J08010/L3K08010		L3J08018/L3K08018		L3J08020/L3K08020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	11.764	—	12.036	—	12.467	—	12.746	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.797	—	3.930	—	4.054	—	4.174	—	
Write-Data Through Time	t_{WDT}	—	11.764	—	12.036	—	12.467	—	12.746	

15) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 192-word

Table 5-105 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	23.079	—	23.309	—	23.545	—	23.775	ns
Read-Cycle Time	t_{RCY}	23.079	—	23.309	—	23.545	—	23.775	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRBS Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRBS Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.948	—	1.986	—	2.017	—	2.058	—	

Table 5-106 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J0C008/L3K0C008		L3J0C010/L3K0C010		L3J0C018/L3K0C018		L3J0C020/L3K0C020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	11.787	—	12.151	—	12.483	—	12.794	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	3.925	—	4.036	—	4.151	—	4.261	—	
Write-Data Through Time	t_{WDT}	—	11.787	—	12.151	—	12.483	—	12.794	

16) 1.5-V specification ($V_{DD} = 1.5 \text{ V} \pm 0.1 \text{ V}$, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$) 256-word

Table 5-107 1-port RAM and 2-port RAM Read-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Access Time	t_{ACS}, t_{ACC}	—	27.517	—	27.737	—	27.957	—	28.176	ns
Read-Cycle Time	t_{RCY}	27.517	—	27.737	—	27.957	—	28.176	—	
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XRB Setup Time	t_{RBS}	2.800	—	2.800	—	2.800	—	2.800	—	
XRB Hold Time	t_{RBH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Output Hold Time	t_{OH}	1.977	—	2.012	—	2.048	—	2.083	—	

Table 5-108 1-port RAM and 2-port RAM Write-Cycle AC Characteristics Table

Parameter	Symbol	L3J10008/L3K10008		L3J10010/L3K10010		L3J10018/L3K10018		L3J10020/L3K10020		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write-Cycle Time	t_{WCY}	11.919	—	12.272	—	12.612	—	12.961	—	ns
Clock High Pulse Width	t_{CKH}	0.500	—	0.500	—	0.500	—	0.500	—	
Clock Low Pulse Width	t_{CKL}	0.500	—	0.500	—	0.500	—	0.500	—	
XCS Setup Time	t_{CSS}	2.800	—	2.800	—	2.800	—	2.800	—	
XCS Hold Time	t_{CSH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Setup Time	t_{AS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Setup Time	t_{WES}	2.800	—	2.800	—	2.800	—	2.800	—	
XWE Hold Time	t_{WEH}	0.000	—	0.000	—	0.000	—	0.000	—	
XWA Setup Time	t_{WAS}	2.800	—	2.800	—	2.800	—	2.800	—	
XWA Hold Time	t_{WAH}	0.000	—	0.000	—	0.000	—	0.000	—	
Address Hold Time	t_{AH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Hold Time	t_{DH}	0.000	—	0.000	—	0.000	—	0.000	—	
Data Setup Time	t_{DS}	2.800	—	2.800	—	2.800	—	2.800	—	
Write-Data Hold Time	t_{WDH}	4.019	—	4.134	—	4.251	—	4.356	—	
Write-Data Through Time	t_{WDT}	—	11.919	—	12.272	—	12.612	—	12.961	

5.1.7 Power Consumption of RAM

Tables 5-109 through 5-120 list the power-consumption values for the primary products of Basic Cell-type RAMs in the S1K/S1X70000 series.

For the power-consumption values of Basic Cell-type RAMs not shown here, use those of the RAM with the most similar configuration in the S1K/S1X70000 series. If more detailed power-consumption values are required, use the calculation formula shown below.

Note that “W” and “B” in each calculation formula denote the number of words and the number of bits, respectively.

(1) Standard-1 type

1) 1-port RAM

- For operation with $V_{DD} = 1.8 \text{ V}$
 $(-5 \times 10^{-5} \times W^2 + 0.0254 \times W + 5.97 + (0.0051 \times W + 0.755) \times B) \times 1.8 \text{ } [\mu\text{W/MHz}]$

Table 5-109 Typical Power-Consumption Values for Standard-1 1-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	28.88	35.40	41.18	46.22	μW/MHz
16 Bit	44.45	55.67	66.15	75.90	
24 Bit	60.02	75.94	91.12	105.57	
32 Bit	75.59	96.21	116.10	135.24	

- For operation with $V_{DD} = 1.5 \text{ V}$
 $(-4 \times 10^{-5} \times W^2 + 0.0204 \times W + 4.74 + (0.0043 \times W + 0.6) \times B) \times 1.5 \text{ } [\mu\text{W/MHz}]$

Table 5-110 Typical Power-Consumption Values for Standard-1 1-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	19.33	23.85	27.88	31.42	μW/MHz
16 Bit	29.83	37.65	44.99	51.83	
24 Bit	40.33	51.46	62.09	72.24	
32 Bit	50.83	65.26	79.20	92.65	

2) 2-port RAM

- For operation with $V_{DD} = 1.8 \text{ V}$
 $(-1 \times 10^{-4} \times W^2 + 0.0508 \times W + 11.88 + (0.0102 \times W + 1.51) \times B) \times 1.8 \text{ } [\mu\text{W/MHz}]$

Table 5-111 Typical Power-Consumption Values for Standard-1 2-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	57.75	70.79	82.36	92.45	μW/MHz
16 Bit	88.90	111.34	132.30	151.79	
24 Bit	120.04	151.88	182.25	211.14	
32 Bit	151.18	192.43	232.19	270.49	

- For operation with $V_{DD} = 1.5\text{ V}$
 $(-8 \times 10^{-5} \times W^2 + 0.0408 \times W + 9.48 + (0.0086 \times W + 1.2) \times B) \times 1.5 [\mu\text{W}/\text{MHz}]$

Table 5-112 Typical Power-Consumption Values for Standard-1
2-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	38.65	47.70	55.76	62.84	μW/MHz
16 Bit	59.65	75.31	89.98	103.66	
24 Bit	80.66	102.92	124.19	144.48	
32 Bit	101.66	130.53	158.40	185.30	

(2) High-Performance type

1) 1-port RAM

- For operation with $V_{DD} = 1.8\text{ V}$
 $(-8 \times 10^{-5} \times W^2 + 0.0406 \times W + 6.377 + (0.0052 \times W + 1.2235) \times B) \times 1.8 [\mu\text{W}/\text{MHz}]$

Table 5-113 Typical Power-Consumption Values for High-Performance
1-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	37.98	45.68	52.20	57.54	μW/MHz
16 Bit	60.39	72.88	84.19	94.33	
24 Bit	82.80	100.08	116.19	131.11	
32 Bit	105.21	127.29	148.18	167.90	

- For operation with $V_{DD} = 1.5\text{ V}$
 $(-5 \times 10^{-5} \times W^2 + 0.0287 \times W + 5.3405 + (0.0049 \times W + 0.087) \times B) \times 1.5 [\mu\text{W}/\text{MHz}]$

Table 5-114 Typical Power-Consumption Values for High-Performance
1-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	15.27	20.86	25.85	30.21	μW/MHz
16 Bit	20.07	29.43	38.18	46.31	
24 Bit	24.88	38.00	50.51	62.41	
32 Bit	29.69	46.57	62.85	78.50	

2) 2-port RAM

- For operation with $V_{DD} = 1.8 \text{ V}$

$$(-1.6 \times 10^{-4} \times W^2 + 0.0812 \times W + 12.754 + (0.0104 \times W + 2.447) \times B) \times 1.8 \text{ } [\mu\text{W}/\text{MHz}]$$

Table 5-115 Typical Power-Consumption Values for High-Performance 2-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	75.95	91.35	104.39	115.08	μW/MHz
16 Bit	120.77	145.76	168.38	188.65	
24 Bit	165.60	200.17	232.38	262.23	
32 Bit	210.42	254.57	296.37	335.80	

- For operation with $V_{DD} = 1.5 \text{ V}$

$$(-1 \times 10^{-4} \times W^2 + 0.0574 \times W + 10.681 + (0.0098 \times W + 0.174) \times B) \times 1.5 \text{ } [\mu\text{W}/\text{MHz}]$$

Table 5-116 Typical Power-Consumption Values for High-Performance 2-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	30.53	41.73	51.69	60.43	μW/MHz
16 Bit	40.15	58.87	76.36	92.62	
24 Bit	49.76	76.01	101.02	124.81	
32 Bit	59.38	93.15	125.69	157.01	

(3) Low-Leakage type

1) 1-port RAM

- For operation with $V_{DD} = 1.8 \text{ V}$

$$(-6 \times 10^{-5} \times W^2 + 0.0267 \times W + 7.2597 + (0.0057 \times W + 0.6055) \times B) \times 1.8 \text{ } [\mu\text{W}/\text{MHz}]$$

Table 5-117 Typical Power-Consumption Values for Low-Leakage 1-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	29.67	36.68	42.79	48.02	μW/MHz
16 Bit	43.65	55.90	67.27	77.76	
24 Bit	57.62	75.13	91.75	107.49	
32 Bit	71.59	94.35	116.23	137.22	

- For operation with $V_{DD} = 1.5\text{ V}$
 $(-6 \times 10^{-5} \times W^2 + 0.0289 \times W + 4.8242 + (0.0055 \times W + 0.4265) \times B) \times 1.5\text{ }[\mu\text{W}/\text{MHz}]$

Table 5-118 Typical Power-Consumption Values for Low-Leakage
1-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	18.98	24.88	30.03	34.45	μW/MHz
16 Bit	28.33	38.44	47.82	56.46	
24 Bit	37.67	52.01	65.61	78.48	
32 Bit	47.01	65.57	83.40	100.49	

2) 2-port RAM

- For operation with $V_{DD} = 1.8\text{ V}$
 $(-1.2 \times 10^{-4} \times W^2 + 0.0534 \times W + 14.5194 + (0.0114 \times W + 1.211) \times B) \times 1.8\text{ }[\mu\text{W}/\text{MHz}]$

Table 5-119 Typical Power-Consumption Values for Low-Leakage
2-port RAMs Operating at 1.8 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	59.35	73.35	85.58	96.05	μW/MHz
16 Bit	87.29	111.80	134.54	155.51	
24 Bit	115.24	150.25	183.50	214.98	
32 Bit	143.18	188.70	232.46	274.44	

- For operation with $V_{DD} = 1.5\text{ V}$
 $(-1.2 \times 10^{-4} \times W^2 + 0.0578 \times W + 9.6484 + (0.011 \times W + 0.853) \times B) \times 1.5\text{ }[\mu\text{W}/\text{MHz}]$

Table 5-120 Typical Power-Consumption Values for Low-Leakage
2-port RAMs Operating at 1.5 V

	64 Word	128 Word	192 Word	256 Word	Unit
8 Bit	37.97	49.75	60.06	68.90	μW/MHz
16 Bit	56.65	76.89	95.64	112.93	
24 Bit	75.34	104.02	131.22	156.96	
32 Bit	94.02	131.15	166.80	200.98	

Table 5-121 Description of High-Density-Type 1-port RAM Signals

Input/Output Signal		Functional Description
Symbol	Name	
CK	Clock input	Chip select (XCS), write enable (XWE), byte write enable (XBWEn), address input (A0–An), and data input (D0–Dn) are latched into the rising edge (Low-to-High transition) of the clock input (CK). Memory is activated when the latched chip select signal is Low. While memory is active, data is written to memory when the latched write-enable signal is Low, or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCS	Chip select	Latched into the rising edge of the clock input (CK). When the latched value is Low, memory is activated.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low, or for read operation when the latched value is High.
XBWEn	Byte write enable	Latched into the rising edge of the clock input (CK). Each byte of data is assigned one byte write-enable signal. Only data bytes with Low byte write enable (XBWEn) when write enable (XWE) is Low, are written to memory. XBWE0 for D0–D7 XBWE1 for D8–D15 XBWE2 for D16–D23 XBWE3 for D24–D31
A0–An	Address input	Latched into the rising edge of the clock input (CK).
D0–Dn	Data input	The write data is latched into the rising edge of the clock input (CK) and written to memory cells.
Y0–Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the latched write data is output from these pins.

5.2.4 Truth Table of Device Operation

For writing, assert chip select (XCS), write enable (XWE), and byte write enable (XBWE0–XBWE3) (by pulling them Low), and set the address inputs (A0–An) and data inputs (D0–Dn) before the clock input (CK) goes High. All of the chip-select, write-enable, byte write-enable, address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data-output pins (Y0–Yn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0–An) before the clock input (CK) goes High. All of the chip-select, write-enable, and address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y0–Yn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either reading or writing, data appears at the data-output pins even after the operation has been completed and the memory is placed in standby state.

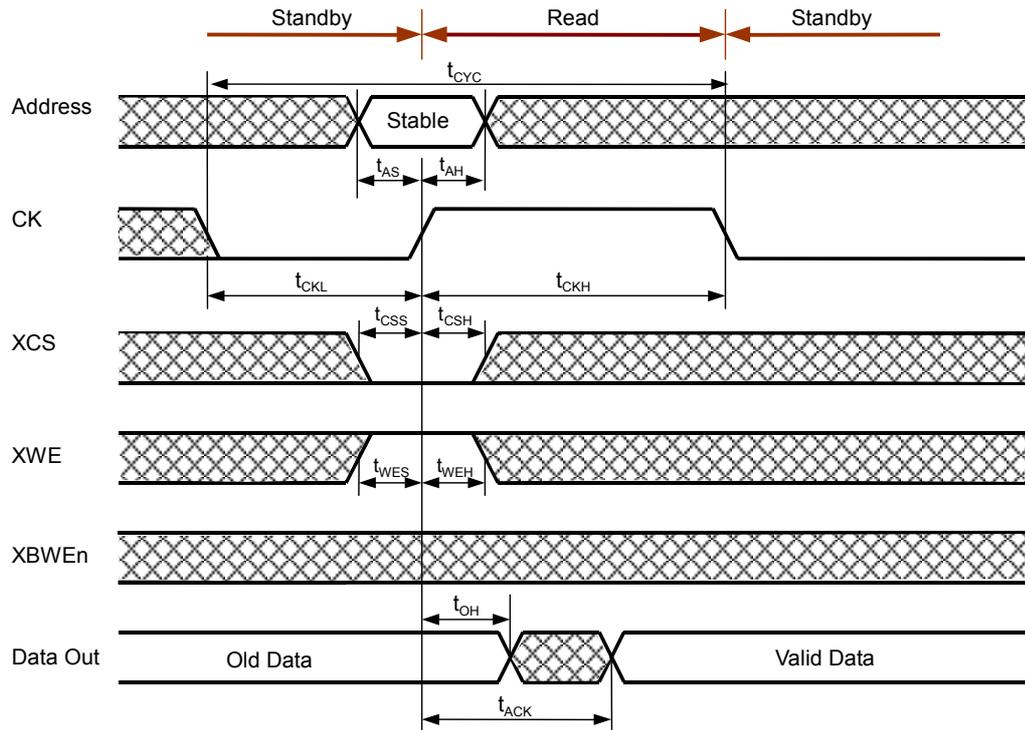
Table 5-122 Truth Table of High-Density-Type 1-port RAM Operation

CK	XCS	XWE	XBWE0	XBWE1	XBWE2	XBWE3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data Hold	Standby
L→H	L	H	X	X	X	X	—	Read Data	Read
L→H	L	L	L	L	L	L	D0-D31	Write Data	Write all bytes
L→H	L	L	L	H	H	H	D0-D7	Write Data ^(*)	Write 1st byte
L→H	L	L	H	L	H	H	D8-D15	Write Data ^(*)	Write 2nd byte
L→H	L	L	H	H	L	H	D16-D23	Write Data ^(*)	Write 3rd byte
L→H	L	L	H	H	H	L	D24-D31	Write Data ^(*)	Write 4th byte
L→H	L	L	H	H	H	H	—	Write Data ^(*)	Unable to write
L→H	H	X	X	X	X	X	—	Data Hold	Standby
H→L	X	X	X	X	X	X	—	Data Hold	Standby

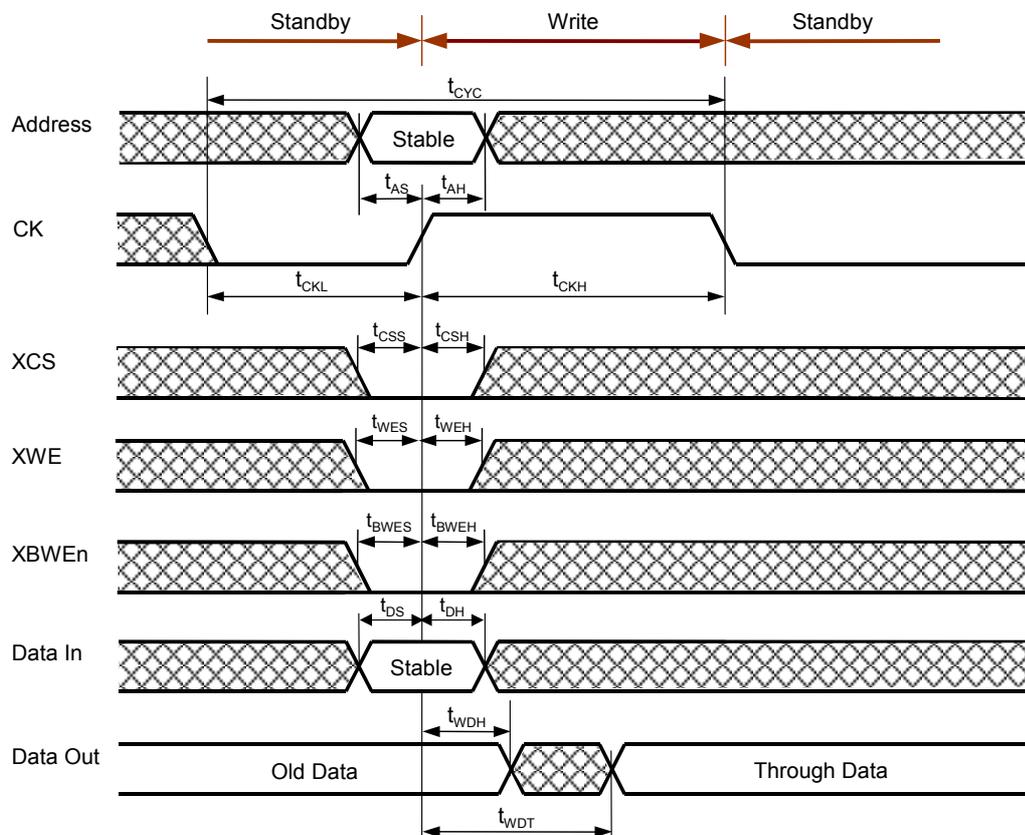
Note *1: The state of the data outputs (Y0–Yn) reflects the values supplied to the data inputs (D0–Dn). However, only the data bytes selected using byte write enable (XBWE0–XBWE3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

5.2.5 Timing Charts

- During reading



- During writing



5.2.6 Electrical Characteristics

5.2.6.1 AC Characteristics

Table 5-123 Electrical Characteristics (Memory Configuration: 4k Words x 16 Data)

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	142	—	—	98	MHz
CK Access Time	t_{ACK}	—	3.3	5.4	—	4.7	8.0	ns
CK High Pulse Width	t_{CKH}	3.5	—	—	5.1	—	—	ns
CK Low Pulse Width	t_{CKL}	2.9	—	—	3.9	—	—	ns
Cycle Time	t_{CYC}	7.0	—	—	10.2	—	—	ns
CS Setup Time	t_{CSS}	2.8	—	—	3.6	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.8	—	—	3.6	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.8	—	—	3.6	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.8	—	—	3.6	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	0.6	—	—	0.8	—	—	ns
Data Setup Time	t_{DS}	2.8	—	—	3.6	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	1.3	—	—	2.8	ns

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	156	—	—	100	MHz
CK Access Time	t_{ACK}	—	3.3	5.3	—	4.7	7.9	ns
CK High Pulse Width	t_{CKH}	3.2	—	—	5.0	—	—	ns
CK Low Pulse Width	t_{CKL}	2.8	—	—	3.8	—	—	ns
Cycle Time	t_{CYC}	6.4	—	—	10.0	—	—	ns
CS Setup Time	t_{CSS}	2.6	—	—	3.5	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.6	—	—	3.5	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.6	—	—	3.5	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.6	—	—	3.5	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	0.4	—	—	0.8	—	—	ns
Data Setup Time	t_{DS}	2.6	—	—	3.5	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	1.8	—	—	2.8	ns

5.2.7 Power Consumption

The power consumption of high-density-type 1-port RAMs varies in a complicated manner depending on the word/bit configurations. For detailed information on the power consumption, please contact the sales division of Epson.

5.3 High-Density-Type Dual-Port RAM

5.3.1 Features

- This type of RAM is exclusively designed as dual-port RAM in order to reduce the area that it occupies.
- Can be configured in a wide range of memory capacities (1k to 64k bits), and provides superior flexibility for selection of the height-to-width ratio of the layout shape. Furthermore, if large-capacity memory is required, multiple pieces of memory macros may be used.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- The chip-select, write-enable, byte write-enable, address, and data-input/output parts contain a latch circuit, making the RAM capable of clock-synchronized, high-speed operation.
- The data-input port and data-output port are separated.
- A byte write function is included, allowing the bits of write data to be selected in byte units.
- The data-output part contains a latch circuit, so that readout data is output continuously until the next read cycle.
- Libraries are available that use Standard-1-type transistors.

5.3.2 RAM Sizes

The sizes of high-density-type dual-port RAMs vary in a complicated manner depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

5.3.3 Input Signals and Block Diagrams

Ports 1 and 2 are each capable of performing read and write operations. Each port comes equipped with a clock input pin, allowing them to be operated with different frequencies or timing independently of each other.

Be aware that no memory cells can be accessed from two ports at the same time. If arbitration facilities, busy signals, or the like are required to resolve conflicts, configure a necessary circuit in the gate-array section external to the macro. (If accessed at the same time, the read or write operation in that cycle and the data in the accessed memory cell become indeterminate.)

Table 5-124 Description of High-Density-Type Dual-Port RAM Signals

Port-1 signals (read/write)

Input/Output Signal		Functional Description
Symbol	Name	
CKA	Clock input	Chip select (XCSA), write enable (XWEA), byte write enable (XBWEAn), address input (AA0–AA _n), and data input (DA0–DA _n) are latched into the rising edge (Low-to-High transition) of the clock input (CKA). Memory is activated when the latched chip-select signal is Low. While the memory is active, data is written to memory when the latched write-enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCSA	Chip select	Latched into the rising edge of the clock input (CKA). Memory is activated when the latched value is Low.
XWEA	Write enable	Latched into the rising edge of the clock input (CKA). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEAn	Byte write enable	Latched into the rising edge of the clock input (CKA). Each byte of data is assigned one byte write-enable signal. Only data bytes with Low byte write enable (XBWEAn) when write enable (XWEA) is Low are written to memory. XBWEA0 for DA0–DA7 XBWEA1 for DA8–DA15 XBWEA2 for DA16–DA23 XBWEA3 for DA24–DA31
AA0–AA _n	Address input	Latched into the rising edge of the clock input (CKA).
DA0–DA _n	Data input	The write data is latched into the rising edge of the clock input (CKA) and written to memory cells.
YA0–YA _n	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CKA). During writing, the latched write data is output from these pins.

Port-2 signals (read/write)

Input/Output Signal		Functional Description
Symbol	Name	
CKB	Clock input	Chip select (XCSB), write enable (XWEB), byte write enable (XBWEBn), address input (AB0–ABn), and data input (DB0–DBn) are latched into the rising edge (Low-to-High transition) of the clock input (CKB). Memory is activated when the latched chip-select signal is Low. While the memory is active, data is written to memory when the latched write-enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCSB	Chip select	Latched into the rising edge of the clock input (CKB). Memory is activated when the latched value is Low.
XWEB	Write enable	Latched into the rising edge of the clock input (CKB). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEBn	Byte write enable	Latched into the rising edge of the clock input (CKB). Each byte of data is assigned one byte write-enable signal. Only data bytes with Low byte write enable (XBWEBn) when write enable (XWEB) is Low are written to memory. XBWEB0 for DB0–DB7 XBWEB1 for DB8–DB15 XBWEB2 for DB16–DB23 XBWEB3 for DB24–DB31
AB0–ABn	Address input	Latched into the rising edge of the clock input (CKB).
DB0–DBn	Data input	The write data is latched into the rising edge of the clock input (CKB) and written to memory cells.
YB0–YBn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CKB). During writing, the latched write data is output from these pins.

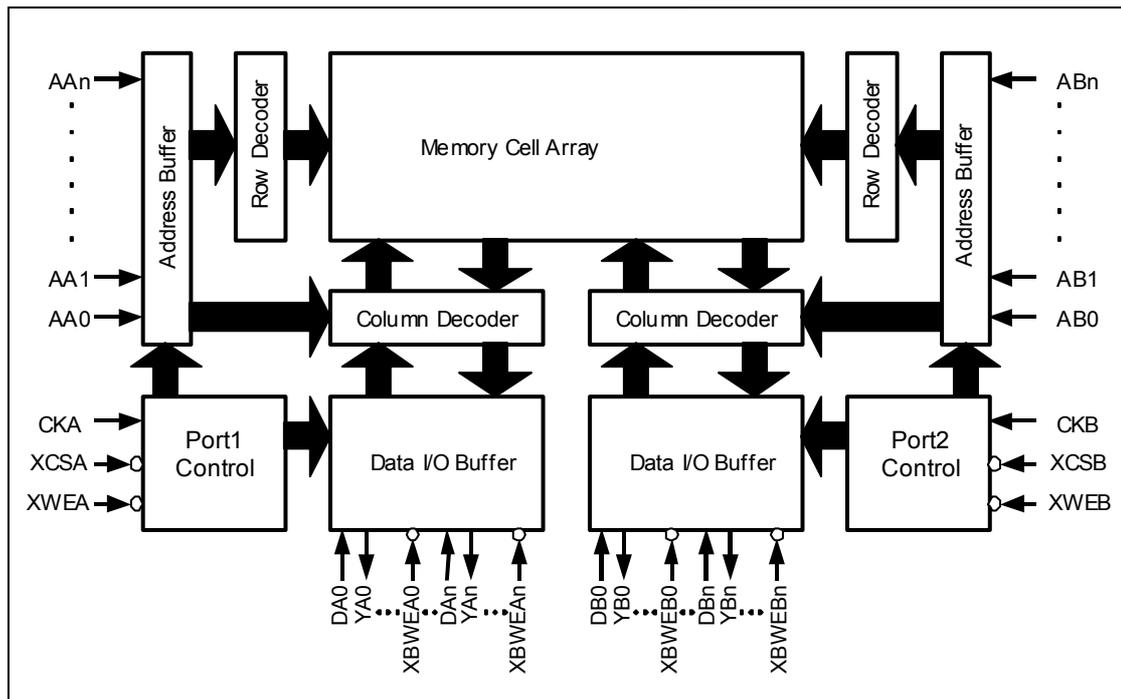


Figure 5-4 Block Diagram of High-Density-Type Dual-Port RAM

5.3.4 Truth Table of Device Operation

For writing, assert chip select (XCSA or XCSB), write enable (XWEA or XWEB), and byte write enable (XBWEA0–XBWEA3 or XBWEB0–XBWEB3) (by pulling them Low), and set the address inputs (AA0–AA_n or AB0–AB_n) and data inputs (DA0–DA_n or DB0–DB_n) before the clock input (CKA or CKB) goes High. All of the chip-select, write-enable, byte write-enable, address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data-output pins (YA0–YA_n or YB0–YB_n). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

For reading, assert chip select (XCSA or XCSB) and deassert write enable (XWEA or XWEB) (by pulling XCSA or XCSB Low and XWEA or XWEB High), and set the address inputs (AA0–AA_n or AB0–AB_n) before the clock input (CKA or CKB) goes High. All of the chip-select, write-enable, and address-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the output pins (YA0–YA_n or YB0–YB_n) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either read or write, data appears at the data-output pins even after the operation has completed and the memory is placed in standby state.

Table 5-125 Truth Table of High-Density-Type Dual-Port RAM Operation

Port-1 truth table

CKA	XCSA	XWEA	XBWEA0	XBWEA1	XBWEA2	XBWEA3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data Hold	Standby
L→H	L	H	X	X	X	X	—	Read Data	Read
L→H	L	L	L	L	L	L	DA0-DA31	Write Data	Write all bytes
L→H	L	L	L	H	H	H	DA0-DA7	Write Data ^(*)	Write 1st byte
L→H	L	L	H	L	H	H	DA8-DA15	Write Data ^(*)	Write 2nd byte
L→H	L	L	H	H	L	H	DA16-DA23	Write Data ^(*)	Write 3rd byte
L→H	L	L	H	H	H	L	DA24-DA31	Write Data ^(*)	Write 4th byte
L→H	L	L	H	H	H	H	—	Write Data ^(*)	Unable to write
L→H	H	X	X	X	X	X	—	Data Hold	Standby
H→L	X	X	X	X	X	X	—	Data Hold	Standby

Port-2 truth table

CKB	XCSB	XWEB	XBWEB0	XBWEB1	XBWEB2	XBWEB3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data Hold	Standby
L→H	L	H	X	X	X	X	—	Read Data	Read
L→H	L	L	L	L	L	L	DB0-DB31	Write Data	Write all bytes
L→H	L	L	L	H	H	H	DB0-DB7	Write Data ^(*)	Write 1st byte
L→H	L	L	H	L	H	H	DB8-DB15	Write Data ^(*)	Write 2nd byte
L→H	L	L	H	H	L	H	DB16-DB23	Write Data ^(*)	Write 3rd byte
L→H	L	L	H	H	H	L	DB24-DB31	Write Data ^(*)	Write 4th byte
L→H	L	L	H	H	H	H	—	Write Data ^(*)	Unable to write
L→H	H	X	X	X	X	X	—	Data Hold	Standby
H→L	X	X	X	X	X	X	—	Data Hold	Standby

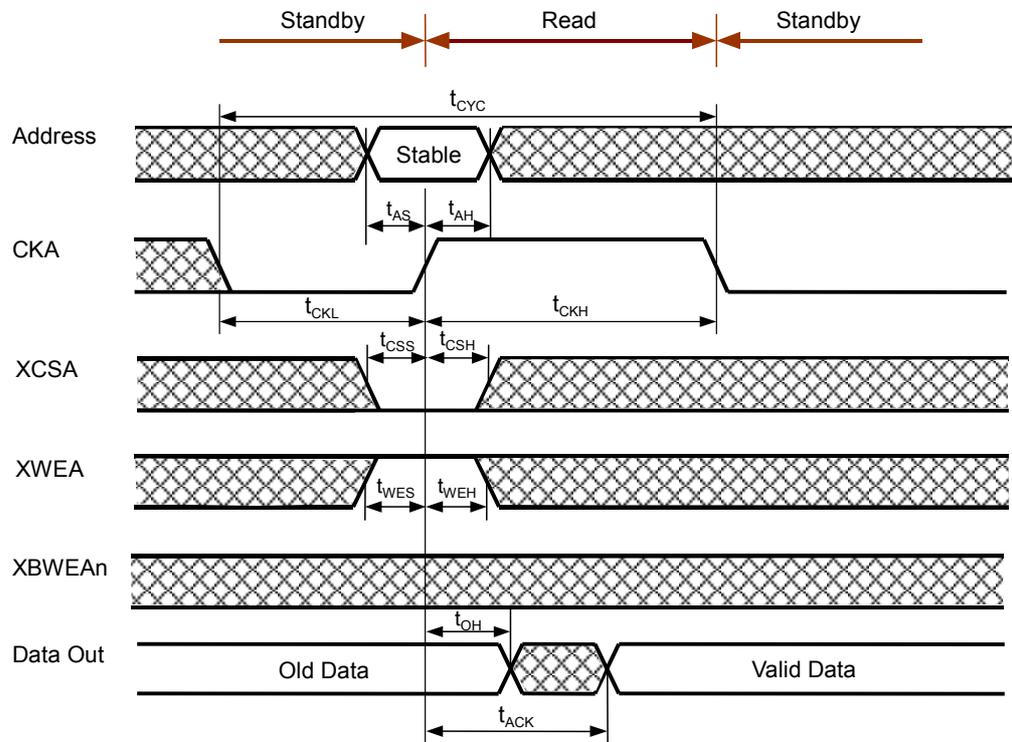
Note *1: The state of the data outputs (YA0–YAn or YB0–YBn) reflects the values supplied to the data inputs (DA0–DAn or DB0–DBn).

However, only the data bytes selected using byte write enable (XBWEA0–XBWEA3 or XBWEB0–XBWEB3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

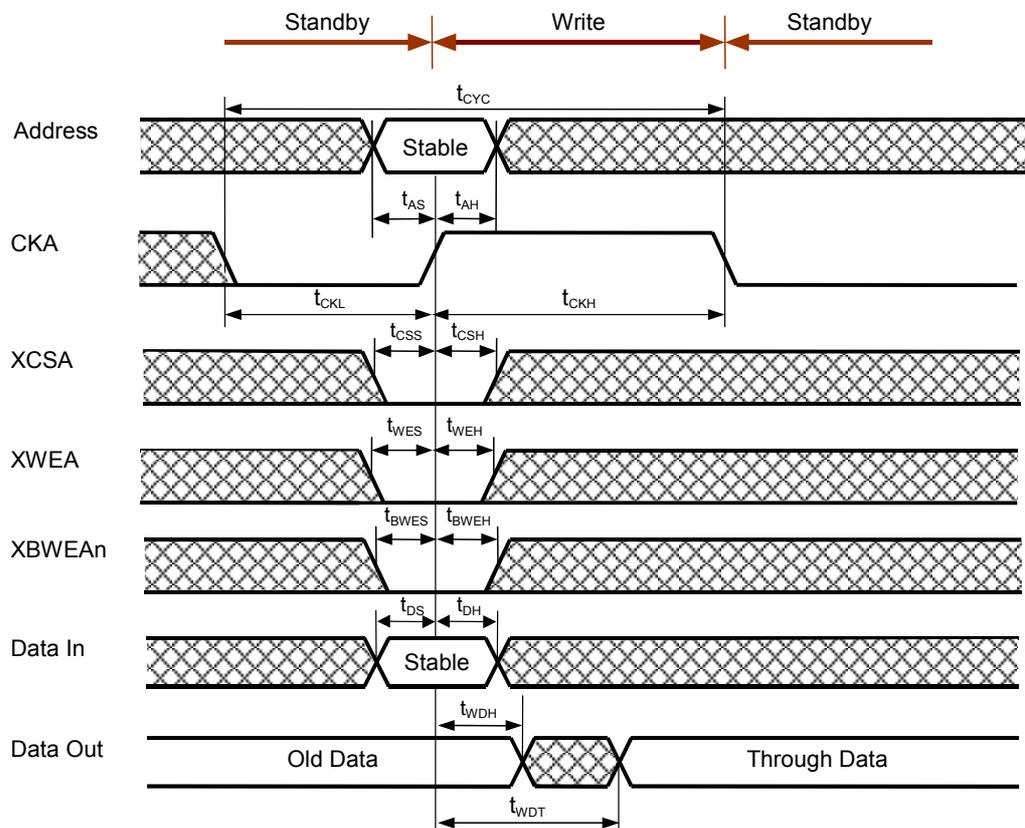
5.3.5 Timing Charts

(1) 1-port RAM

- During reading

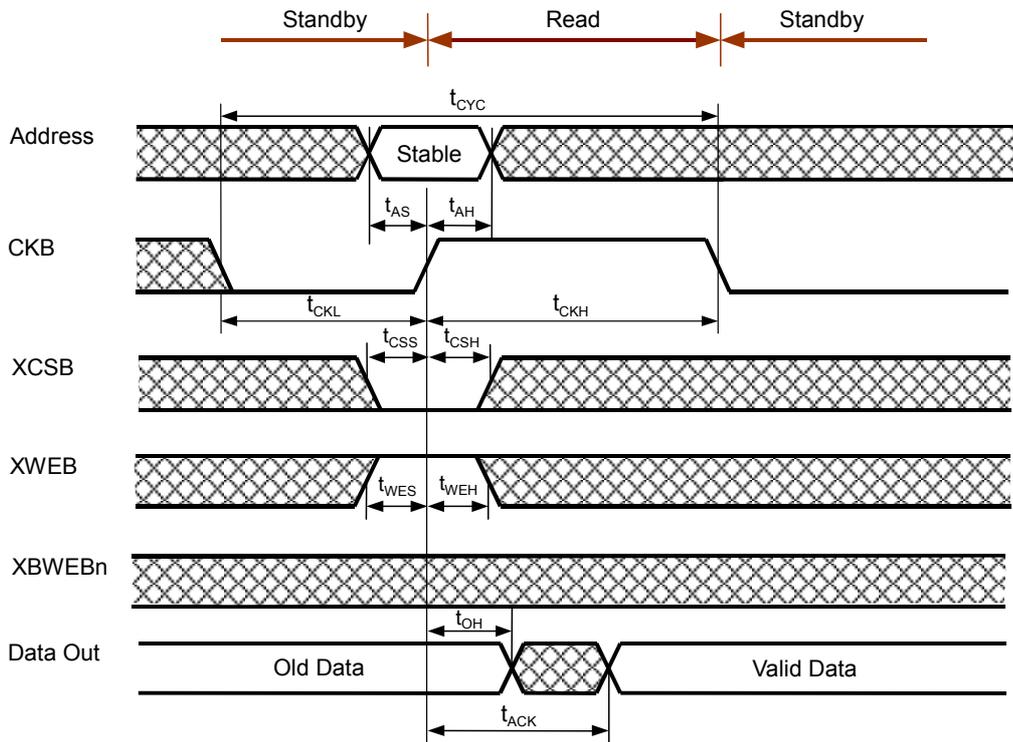


- During writing

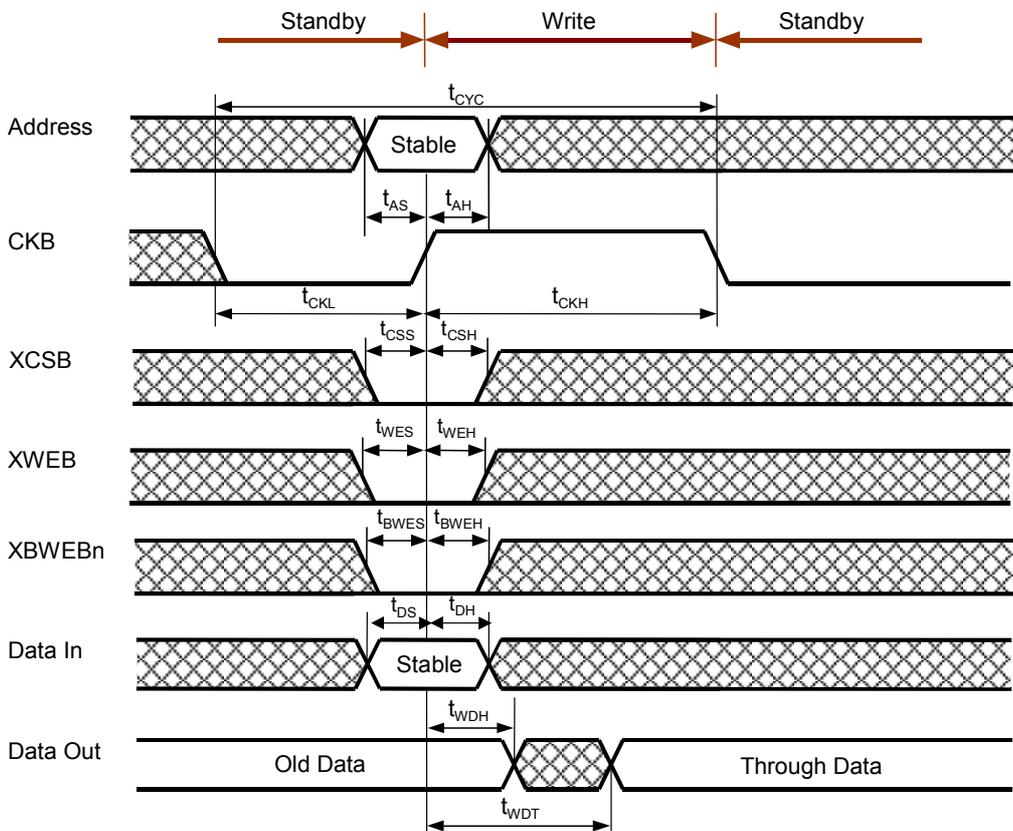


(2) Dual-port RAM

- Port 1



- Port 2



5.3.6 Electrical Characteristics

5.3.6.1 AC Characteristics

Table 5-126 Electrical Characteristics (Memory Configuration: 4k Words x 16 Data)

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	138	—	—	94	MHz
CK Access Time	t_{ACK}	—	3.5	5.9	—	3.7	9.0	ns
CK High Pulse Width	t_{CKH}	3.6	—	—	5.3	—	—	ns
CK Low Pulse Width	t_{CKL}	3.6	—	—	4.9	—	—	ns
Cycle Time	t_{CYC}	7.2	—	—	10.6	—	—	ns
CS Setup Time	t_{CSS}	2.8	—	—	3.6	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.8	—	—	3.6	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.8	—	—	3.6	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.8	—	—	3.6	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	0.5	—	—	0.8	—	—	ns
Data Setup Time	t_{DS}	2.8	—	—	3.6	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	2.1	—	—	3.5	ns

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	142	—	—	96	MHz
CK Access Time	t_{ACK}	—	3.5	5.7	—	5.0	8.7	ns
CK High Pulse Width	t_{CKH}	3.3	—	—	5.2	—	—	ns
CK Low Pulse Width	t_{CKL}	3.5	—	—	4.7	—	—	ns
Cycle Time	t_{CYC}	7.0	—	—	10.4	—	—	ns
CS Setup Time	t_{CSS}	2.6	—	—	3.5	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.6	—	—	3.5	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.6	—	—	3.5	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.6	—	—	3.5	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	0.5	—	—	0.8	—	—	ns
Data Setup Time	t_{DS}	2.6	—	—	3.5	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.2	—	—	ns
Write Data Through Time	t_{WDT}	—	—	2.1	—	—	3.5	ns

5.3.7 Power Consumption

The power consumption of high-density-type dual-port RAMs varies in a complicated manner depending on the word/bit configurations. For detailed information on the power consumption, please contact the sales division of Epson.

5.4 Large-Capacity-Type 1-port RAM

5.4.1 Features

- For this type of RAM, the circuit and layout pattern are exclusively designed as 1-port RAM in order to reduce the area that the RAM occupies.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- The chip-select, write-enable, address, data and byte write-enable input parts contain a latch circuit, making the RAM capable of clock-synchronized, high-speed operation.
- The data-input port and data-output port are separated.
- A byte-write function is included, allowing the bits of write data to be selected in byte units.
- The data-output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.
- Libraries are available that use Standard-1-type transistors.

5.4.2 RAM Sizes

The sizes of large-capacity-type 1-port RAMs vary in a complicated manner, depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

5.4.3 Input/Output Signals and Block Diagrams

Table 5-127 Description of Large-Capacity-Type 1-port RAM Signals

Input/Output Signal		Functional Description
Symbol	Name	
CK	Clock input	Chip select (XCS), write enable (XWE), byte write enable (XBWEn), address input (A0–An), and data input (D0–Dn) are latched into the rising edge (Low-to-High transition) of the clock input (CK). Memory is activated when the latched chip-select signal is Low. While the memory is active, data is written to memory when the latched write-enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCS	Chip select	Latched into the rising edge of the clock input (CK). Memory is activated when the latched value is Low.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEn	Byte write enable	Latched into the rising edge of the clock input (CK). Each byte of data is assigned one byte write-enable signal. Only data bytes with Low XBWEn when XWE is Low are written to memory. XBWE0 for D0–D7 XBWE1 for D8–D15 XBWE2 for D16–D23 XBWE3 for D24–D31
A0–An	Address input	Latched into the rising edge of the clock input (CK).
D0–Dn	Data input	The write data is latched into the rising edge of the clock input (CK) and written to memory cells.
Y0–Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the latched write data is output from these pins.

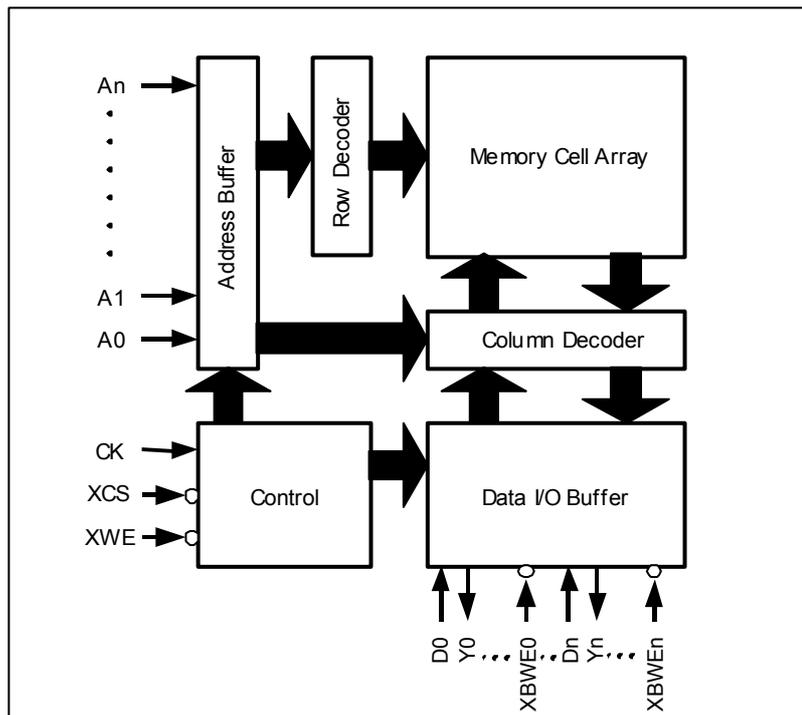


Figure 5-5 Block Diagram of the Large-Capacity-Type 1-port RAM

5.4.4 Truth Table of Device Operation

For writing, assert chip select (XCS), write enable (XWE), and byte write enable (XBWE0–XBWE3) (by pulling them Low), and set the address inputs (A0–An) and data inputs (D0–Dn) before the clock input (CK) goes High. All of the chip-select, write-enable, byte write-enable, address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data-output pins (Y0–Yn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0–An) before the clock input (CK) goes High. All of the chip-select, write-enable, and address-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y0–Yn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either read or write, data appears at the data-output pins even after the operation has completed and the memory is placed in standby state.

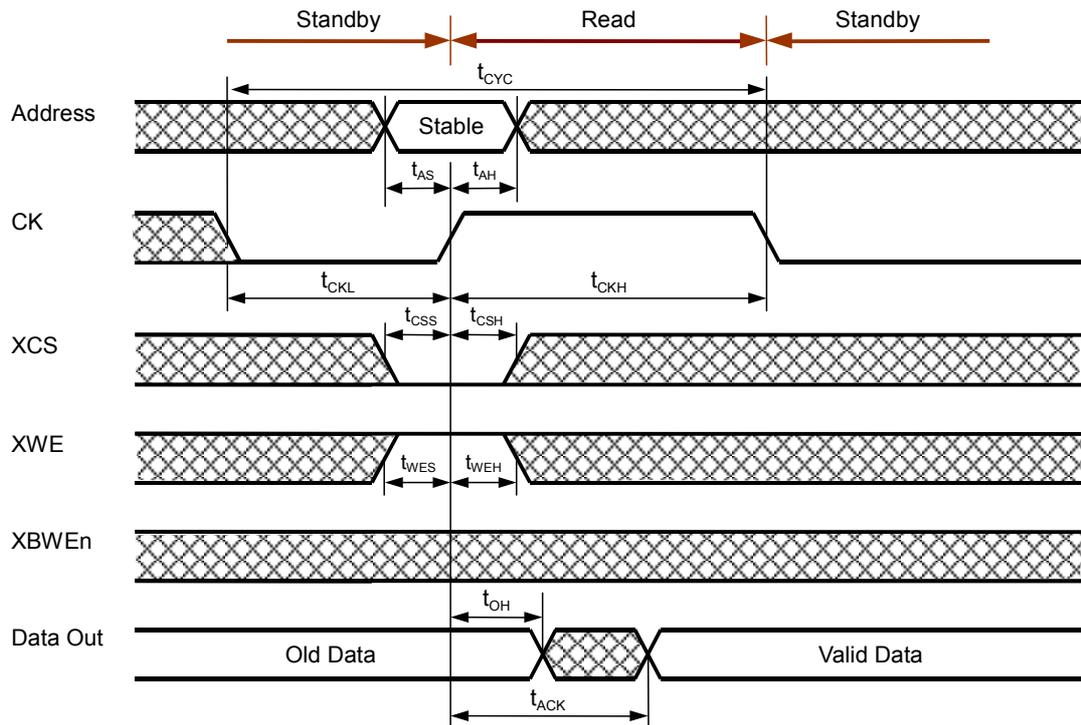
Table 5-128 Truth Table of Large-Capacity-Type 1-port RAM Operation

CK	XCS	XWE	XBWE0	XBWE1	XBWE2	XBWE3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L→H	L	H	X	X	X	X	—	Read Data	Read
L→H	L	L	L	L	L	L	D0-D31	Write Data	Write all bytes
L→H	L	L	L	H	H	H	D0-D7	Write Data ^(*)	Write 1st byte
L→H	L	L	H	L	H	H	D8-D15	Write Data ^(*)	Write 2nd byte
L→H	L	L	H	H	L	H	D16-D23	Write Data ^(*)	Write 3rd byte
L→H	L	L	H	H	H	L	D24-D31	Write Data ^(*)	Write 4th byte
L→H	L	L	H	H	H	H	—	Write Data ^(*)	Unable to write
L→H	H	X	X	X	X	X	—	Data hold	Standby
H→L	X	X	X	X	X	X	—	Data hold	Standby

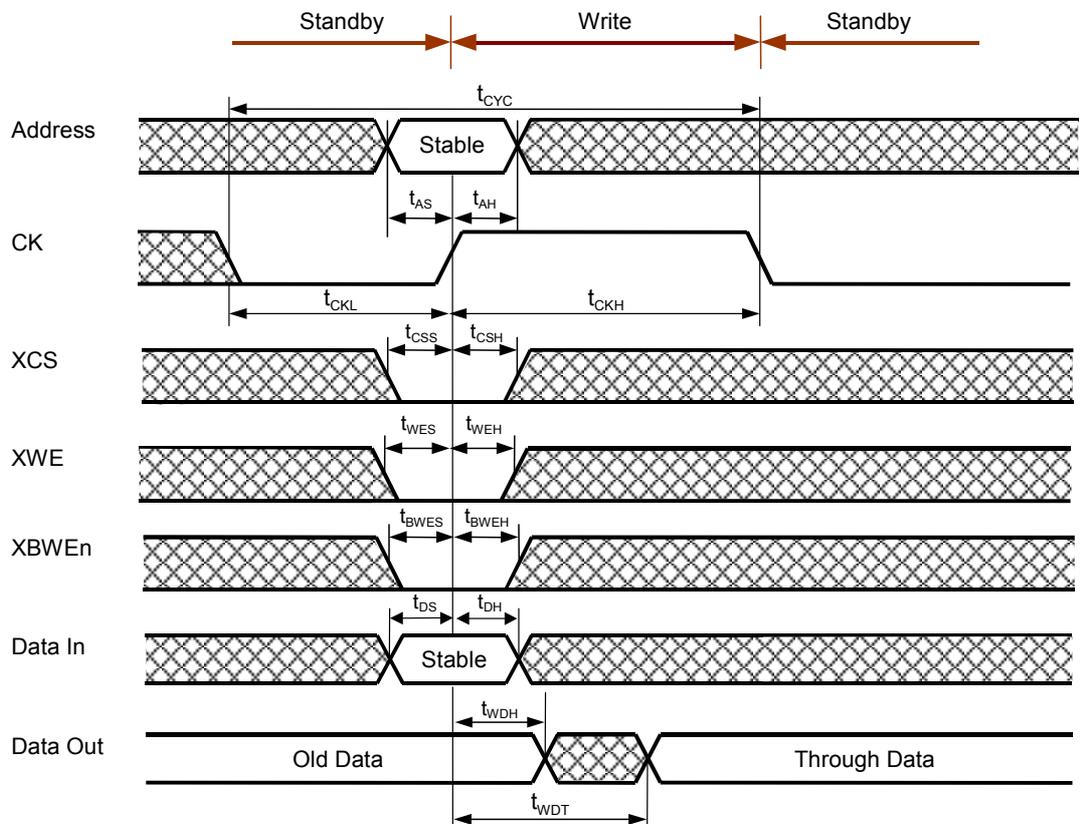
Note *1: The state of data outputs (Y0–Yn) reflects the values supplied to data inputs (D0–Dn).
 However, only the data bytes selected using byte write enable (XBWE0–XBWE3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

5.4.5 Timing Charts

- During reading



- During writing



5.4.6 Electrical Characteristics

5.4.6.1 AC Characteristics

Table 5-129 Electrical Characteristics (Memory Configuration: 64k Words x 16 Data)

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	46	—	—	32	MHz
CK Access Time	t_{ACK}	—	8.3	14.4	—	11.9	20.7	ns
CK High Pulse Width	t_{CKH}	10.7	—	—	15.2	—	—	ns
CK Low Pulse Width	t_{CKL}	2.9	—	—	3.3	—	—	ns
Cycle Time	t_{CYC}	21.4	—	—	30.4	—	—	ns
CS Setup Time	t_{CSS}	2.9	—	—	3.8	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.9	—	—	3.8	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.9	—	—	3.8	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.9	—	—	3.8	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	3.2	—	—	4.6	—	—	ns
Data Setup Time	t_{DS}	2.9	—	—	3.8	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.5	—	—	ns
Write Data Through Time	t_{WDT}	—	—	4.0	—	—	6.1	ns

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	49	—	—	33	MHz
CK Access Time	t_{ACK}	—	8.3	13.8	—	11.9	20.0	ns
CK High Pulse Width	t_{CKH}	10.2	—	—	14.8	—	—	ns
CK Low Pulse Width	t_{CKL}	2.7	—	—	3.1	—	—	ns
Cycle Time	t_{CYC}	20.4	—	—	29.6	—	—	ns
CS Setup Time	t_{CSS}	2.7	—	—	3.6	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.7	—	—	3.6	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
WE Setup Time	t_{WES}	2.7	—	—	3.6	—	—	ns
WE Hold Time	t_{WEH}	0.0	—	—	0.0	—	—	ns
BWE Setup Time	t_{BWES}	2.7	—	—	3.6	—	—	ns
BWE Hold Time	t_{BWEH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	3.2	—	—	4.6	—	—	ns
Data Setup Time	t_{DS}	2.7	—	—	3.6	—	—	ns
Data Hold Time	t_{DH}	0.0	—	—	0.0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.2	—	—	0.5	—	—	ns
Write Data Through Time	t_{WDT}	—	—	3.9	—	—	6.0	ns

5.4.7 Power Consumption

The power consumption of large-capacity-type 1-port RAMs varies in a complicated manner, depending on the word/bit configurations. For detailed information on the power consumption, please contact the sales division of Epson.

5.5 High-Density Large-Capacity-Type 1-port RAM

5.5.1 Features

- For this type of RAM, the size of the memory cells has been reduced and the layout pattern is exclusively designed in order to further reduce the area that the RAM occupies.
- Can be accessed at High speed and consumes less current than other RAMs of the same class.
- The chip-select, write-enable, address, data and byte write-enable input parts contain a latch circuit, making the RAM capable of clock-synchronized, high-speed operation.
- The data-input port and data-output port are separated.
- A byte-write function is included, allowing the bits of write data to be selected in byte units.
- The data-output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.
- Libraries are available that use Standard-1-type transistors.

5.5.2 RAM Sizes

The sizes of high-density large-capacity-type 1-port RAMs vary in a complicated manner, depending on the word/bit configurations. For detailed information on RAM sizes, please contact the sales division of Epson.

5.5.3 Input/Output Signals and Block Diagrams

Table 5-130 Description of High-Density Large-Capacity-Type 1-port RAM Signals

Input/Output Signal		Functional Description
Symbol	Name	
CK	Clock input	Chip select (XCS), write enable (XWE), byte write enable (XBWEn), address input (A0–An), and data input (D0–Dn) are latched into the rising edge (Low-to-High transition) of the clock input (CK). Memory is activated when the latched chip-select signal is Low. While the memory is active, data is written to memory when the latched write-enable signal is Low or read from memory when the signal is High. Operation finishes on the next fall of the clock.
XCS	Chip select	Latched into the rising edge of the clock input (CK). Memory is activated when the latched value is Low.
XWE	Write enable	Latched into the rising edge of the clock input (CK). Memory is activated for write operation when the latched value is Low or for read operation when the latched value is High.
XBWEn	Byte write enable	Latched into the rising edge of the clock input (CK). Each byte of data is assigned one byte write-enable signal. Only data bytes with Low XBWEn when XWE is Low are written to memory. XBWE0 for D0–D7 XBWE1 for D8–D15 XBWE2 for D16–D23 XBWE3 for D24–D31
A0–An	Address input	Latched into the rising edge of the clock input (CK).
D0–Dn	Data input	The write data is latched into the rising edge of the clock input (CK) and written to memory cells.
Y0–Yn	Data output	During reading, the data from memory cells is output a finite access time after the rising edge of the clock input (CK). During writing, the latched write data is output from these pins.

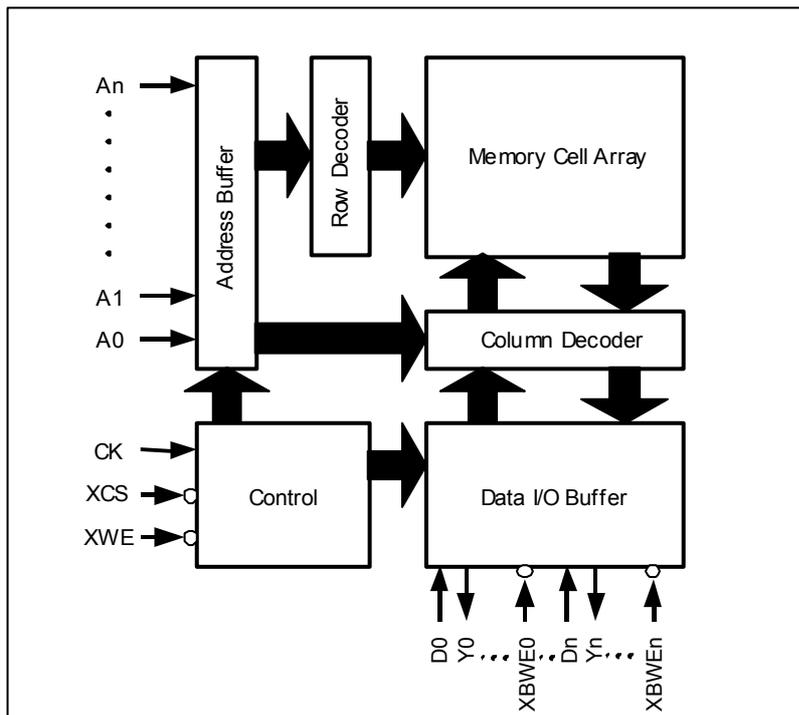


Figure 5-6 Block Diagram of the High-Density Large-Capacity-Type 1-port RAM

5.5.4 Truth Table of Device Operation

For writing, assert chip select (XCS), write enable (XWE), and byte write enable (XBWE0–XBWE3) (by pulling them Low), and set the address inputs (A0–An) and data inputs (D0–Dn) before the clock input (CK) goes High. All of the chip-select, write-enable, byte write-enable, address-input, and data-input signals are latched into the rising edge of the clock input, at which time memory is activated for write operation. During this period, the data being written is output from the data-output pins (Y0–Yn). The write operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state.

For reading, assert chip select (XCS) and deassert write enable (XWE) (by pulling XCS Low and XWE High), and set the address inputs (A0–An) before the clock input (CK) goes High. All of the chip-select, write-enable, and address-input signals are latched into the rising edge of the clock input, at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y0–Yn) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. For either read or write, data appears at the data-output pins even after the operation has completed and the memory is placed in standby state.

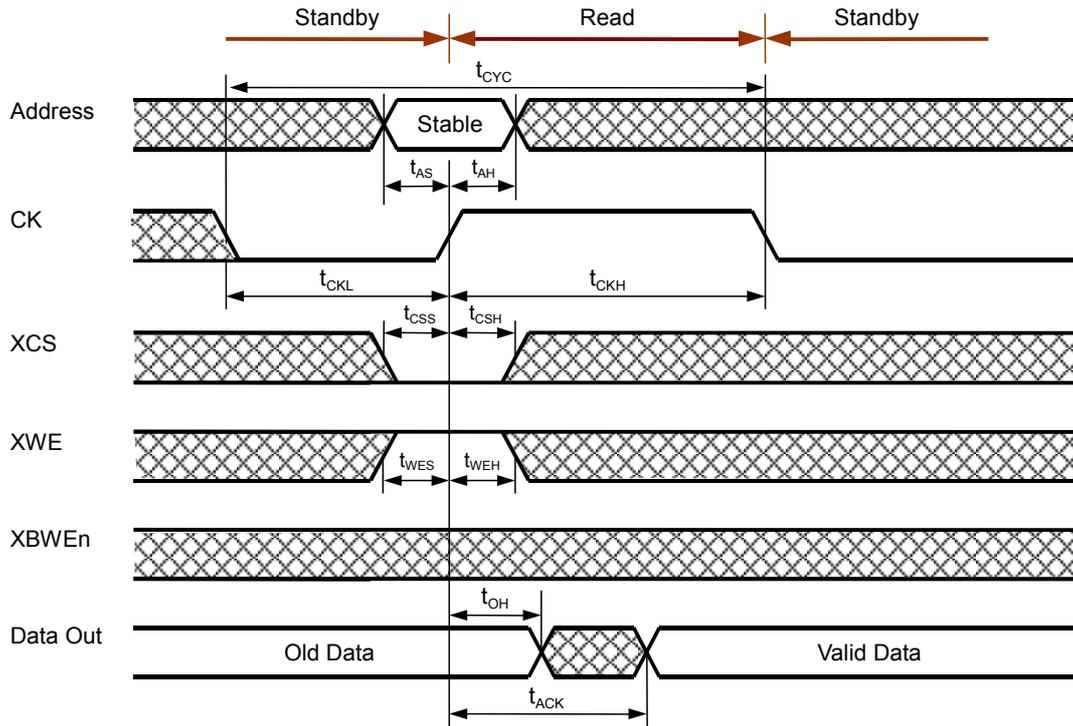
Table 5-131 Truth Table of Large-Capacity-Type 1-port RAM Operation

CK	XCS	XWE	XBWE0	XBWE1	XBWE2	XBWE3	Write	Output State	Operation Mode
L	X	X	X	X	X	X	—	Data hold	Standby
L→H	L	H	X	X	X	X	—	Read Data	Read
L→H	L	L	L	L	L	L	D0-D31	Write Data	Write all bytes
L→H	L	L	L	H	H	H	D0-D7	Write Data ^(*)	Write 1st byte
L→H	L	L	H	L	H	H	D8-D15	Write Data ^(*)	Write 2nd byte
L→H	L	L	H	H	L	H	D16-D23	Write Data ^(*)	Write 3rd byte
L→H	L	L	H	H	H	L	D24-D31	Write Data ^(*)	Write 4th byte
L→H	L	L	H	H	H	H	—	Write Data ^(*)	Unable to write
L→H	H	X	X	X	X	X	—	Data hold	Standby
H→L	X	X	X	X	X	X	—	Data hold	Standby

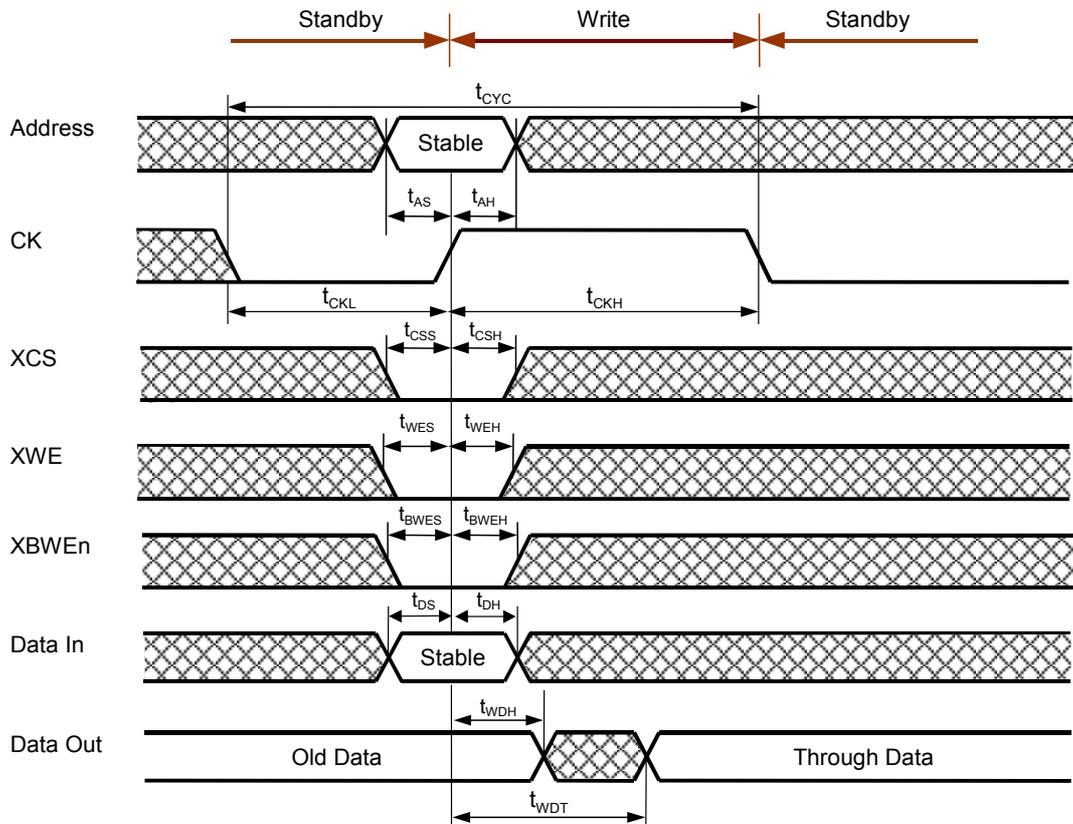
Note *1: The state of data outputs (Y0–Yn) reflects the values supplied to data inputs (D0–Dn).
 However, only the data bytes selected using byte write enable (XBWE0–XBWE3) are written to memory. Data bytes unselected using byte write enable are not written to memory.

5.5.5 Timing Charts

- During reading



- During writing



5.5.6 Electrical Characteristics

5.5.6.1 AC Characteristics

Table 5-132 Electrical Characteristics (Memory Configuration: 64k Words x 16 Data)

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_C	—	—	79.3	—	—	56.8	MHz
CK Access Time	t_{ACK}	—	5.7	9.3	—	7.9	13.5	ns
CK High Pulse Width	t_{CKH}	6.3	—	—	8.8	—	—	ns
CK Low Pulse Width	t_{CKL}	6.3	—	—	8.8	—	—	ns
Cycle Time	t_{CYC}	12.6	—	—	17.6	—	—	ns
CS Setup Time	t_{CSS}	3.1	—	—	4.0	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	3.1	—	—	4.0	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
WE Setup Time	t_{WES}	3.1	—	—	4.0	—	—	ns
WE Hold Time	t_{WEH}	0	—	—	0	—	—	ns
BWE Setup Time	t_{BWES}	3.1	—	—	4.0	—	—	ns
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	3.1	—	—	4.2	—	—	ns
Data Setup Time	t_{DS}	3.1	—	—	4.0	—	—	ns
Data Hold Time	t_{DH}	0	—	—	0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.6	—	—	0.9	—	—	ns
Write Data Through Time	t_{WDT}	—	—	2.7	—	—	3.9	ns

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	81.9	—	—	57.5	MHz
CK Access Time	t_{ACK}	—	5.7	9.0	—	7.9	13.1	ns
CK High Pulse Width	t_{CKH}	6.1	—	—	8.7	—	—	ns
CK Low Pulse Width	t_{CKL}	6.1	—	—	8.7	—	—	ns
Cycle Time	t_{CYC}	12.2	—	—	17.4	—	—	ns
CS Setup Time	t_{CSS}	3.0	—	—	3.8	—	—	ns
CS Hold Time	t_{CSH}	0	—	—	0	—	—	ns
Address Setup Time	t_{AS}	3.0	—	—	3.8	—	—	ns
Address Hold Time	t_{AH}	0	—	—	0	—	—	ns
WE Setup Time	t_{WES}	3.0	—	—	3.8	—	—	ns
WE Hold Time	t_{WEH}	0	—	—	0	—	—	ns
BWE Setup Time	t_{BWES}	3.0	—	—	3.8	—	—	ns
BWE Hold Time	t_{BWEH}	0	—	—	0	—	—	ns
Output Hold Time	t_{OH}	3.1	—	—	4.2	—	—	ns
Data Setup Time	t_{DS}	3.0	—	—	3.8	—	—	ns
Data Hold Time	t_{DH}	0	—	—	0	—	—	ns
Write-Data Hold Time	t_{WDH}	0.6	—	—	0.9	—	—	ns
Write Data Through Time	t_{WDT}	—	—	2.6	—	—	3.8	ns

5.5.7 Power Consumption

The power consumption of large-capacity-type 1-port RAMs varies in a complicated manner, depending on the word/bit configurations. For detailed information on the power consumption, please contact the sales division of Epson.

5.6 ROM

5.6.1 Features

- Exclusively designed as mask ROM in order to reduce the area that it occupies
- Because data is programmed into memory at nearly the end of the manufacturing process, TAT can be reduced.
- Can be accessed at High speed and consumes less current than other ROMs of the same class.
- Can be configured in a wide range of memory capacities (1k to 512k bits), and provides superior flexibility for selection of the height-to-width ratio of the layout shape. Furthermore, if large-capacity memory is required, multiple pieces of memory macros may be used.
- Can operate with Low voltage over a wide voltage range.
- The chip-select and address-input parts contain a latch circuit, making the ROM capable of clock-synchronized, high-speed operation.
- The data-output part contains a latch circuit, allowing readout data to be output continuously until the next read cycle.
- Libraries are available that use Standard-1-type transistors.

5.6.2 ROM Sizes

The ROM sizes vary in a complicated manner depending on the word/bit configurations. For detailed information on ROM sizes, please contact the sales division of Epson.

5.6.3 Input/Output Signals and Block Diagrams

Table 5-133 Description of ROM Signals

Input/Output Signal		Functional Description
Symbol	Name	
CK	Clock input	Chip select (XCS) and address input (A0–An) are latched into the rising edge (Low-to-High transition) of the clock input (CK). When the latched chip-select signal is Low, memory is activated for read operation.
XCS	Chip select	Latched into the rising edge of the clock input (CK). When this latched value is Low, memory is activated for read operation.
A0–An	Address input	Latched into the rising edge of the clock input (CK).
Y0–Yn	Data output	The data readout from memory cells is output from these pins a finite access time after the rising edge of the clock input (CK).

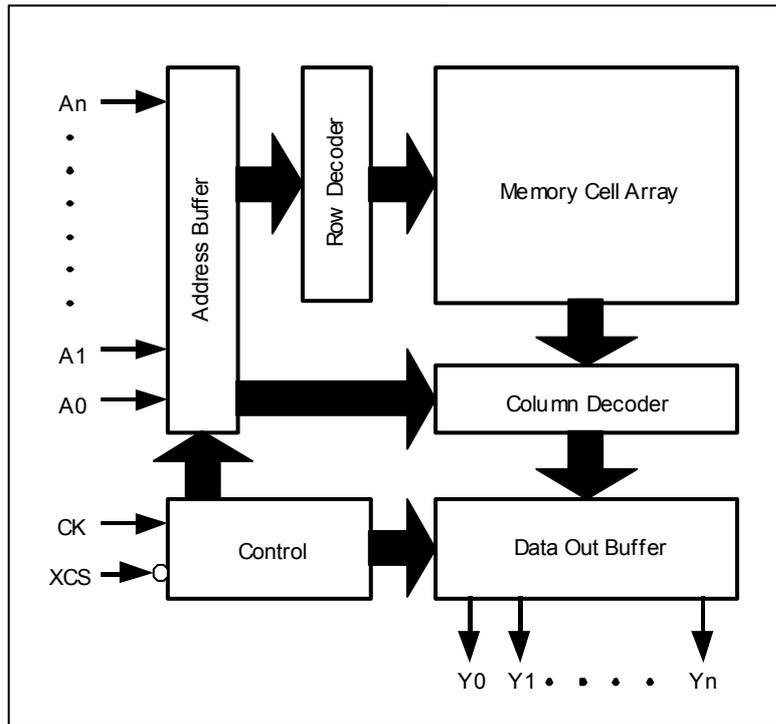


Figure 5-7 Block Diagram of ROM

5.6.4 Truth Table of Device Operation

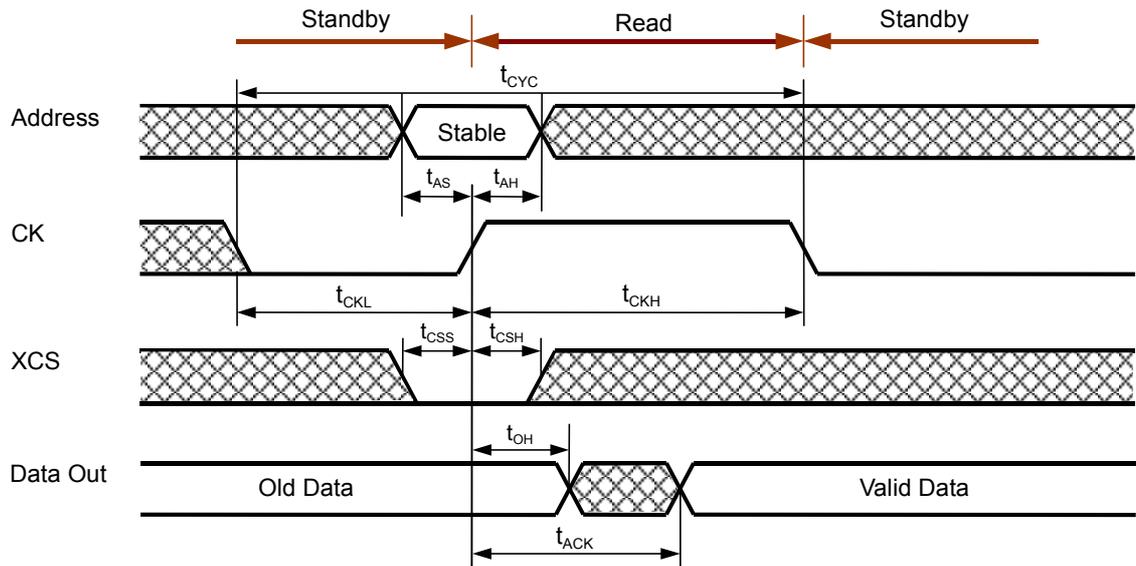
For reading, assert chip select (XCS) (by pulling it Low), and set the address inputs (A_0 – A_n) before the clock input (CK) goes High. The chip-select and address-input signals are latched into the rising edge of the clock, at which time memory is activated for read operation. During this period, data is output from the data-output pins (Y_0 – Y_n) a finite access time after the rise of the clock. The read operation finishes at the fall of the clock, with the input signals unlatched and the memory placed in standby state. Even after the read operation has completed and the memory is placed in standby state, data remains displayed at the data-output pins.

Table 5-134 Truth Table of ROM Operation

CK	XCS	Output State	Operation Mode
L	X	Data Hold	Standby
L→H	L	Read Data	Read
L→H	H	Data Hold	Standby
H→L	X	Data Hold	Standby

5.6.5 Timing Charts

- During reading



5.6.6 Electrical Characteristics

5.6.6.1 AC Characteristics

Table 5-135 Electrical Characteristics (Memory Configuration: 32k Words x 16 Data)

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = -40 \text{ to } +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	67	—	—	48	MHz
CK Access Time	t_{ACK}	—	5.1	8.2	—	7.3	11.9	ns
CK High Pulse Width	t_{CKH}	7.4	—	—	10.3	—	—	ns
CK Low Pulse Width	t_{CKL}	1.4	—	—	1.5	—	—	ns
Cycle Time	t_{CYC}	14.8	—	—	20.6	—	—	ns
CS Setup Time	t_{CSS}	2.4	—	—	2.9	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.4	—	—	2.9	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	1.6	—	—	2.4	—	—	ns

Parameter	Symbol	$V_{DD} = 1.8 V \pm 0.15 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			$V_{DD} = 1.5 V \pm 0.10 V$ $T_a = 0 \text{ to } +70^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_c	—	—	70	—	—	49	MHz
CK Access Time	t_{ACK}	—	5.1	7.9	—	7.3	11.5	ns
CK High Pulse Width	t_{CKH}	7.1	—	—	10.1	—	—	ns
CK Low Pulse Width	t_{CKL}	1.4	—	—	1.5	—	—	ns
Cycle Time	t_{CYC}	14.2	—	—	20.2	—	—	ns
CS Setup Time	t_{CSS}	2.2	—	—	2.8	—	—	ns
CS Hold Time	t_{CSH}	0.0	—	—	0.0	—	—	ns
Address Setup Time	t_{AS}	2.2	—	—	2.8	—	—	ns
Address Hold Time	t_{AH}	0.0	—	—	0.0	—	—	ns
Output Hold Time	t_{OH}	1.6	—	—	2.4	—	—	ns

5.6.7 Power Consumption

The power consumption of ROM varies in a complicated manner depending on the word/bit configurations. For detailed information on the power consumption, please contact the sales division of Epson.

5.7 Access to Nonexistent Addresses Inhibited

When some RAMs with an intermediate word configuration (e.g., 48 or 88 words) are used, there is a possibility of accessing nonexistent addresses.

In the actual IC, if nonexistent addresses are accessed for reading, the target word lines do not exist and all word lines are turned off, resulting in all bit lines being placed in a floating state. For this reason, the following problems may occur:

- (1) Because read operation is performed while all bit lines are left floating, all bits of RAM output become “indeterminate.”
- (2) Because read operation is performed while all bit lines are left floating, a path is created in part of the circuit through which current can flow. Although the amount of this current depends on the RAM configuration and size, it causes the operating and quiescent currents of the entire IC to vary.

Therefore, we recommend that access to nonexistent addresses be inhibited.

In logic simulation, the presence of nonexistent addresses is checked synchronously with the rising edge of the clock during read/write operation and, when access to any nonexistent address is attempted, a timing error is output.

Chapter 6 Estimating Various Characteristic Values

Virtually no current flows through the chip of a CMOS LSI when it is not in operation. However, during operation it consumes an amount of power corresponding to its operating frequency. The greater the power consumption, the higher the LSI chip temperature. An excessively high chip temperature adversely affects LSI quality.

Therefore, the power consumption of LSI chips must be calculated to verify whether it is within the range of the chip's permissible power consumption.

This chapter describes the procedure for calculating the power consumption of all chips in the S1K/S1X70000 series of products.

6.1 Calculation of Power Consumption

The power consumption of CMOS circuits generally depends on the circuit's operating frequency, load capacitance, and power-supply voltage (this does not include special products such as analog circuits in which a steady-state current flows in the chip).

To calculate the power consumption of the entire chip, first find the power consumption of each block of the internal circuit, and then find the sum total for all blocks of the internal circuit. Next, find the power consumption of the input and output buffers. The sum total of these is the total amount of power consumption to be obtained.

The total amount of power consumption, P_{total} , is calculated using the equation below.

$$P_{total} = P_{int} + P_i + P_o$$

where, P_{int} : power consumption of the internal circuit
 P_i : power consumption of the input buffers
 P_o : power consumption of the output buffers

6.1.1 Internal Cells (P_{int})

Because it is difficult to calculate the power consumption of the entire internal circuit area, here we calculate the power consumption of each circuit block and then define the sum total of all blocks as the power consumption of the internal circuit, P_{int} .

$$P_{int} = P_{BC} + P_{CB} + P_{BM} + P_{CM} + P_{IP}$$

where, P_{BC} : power consumption of the Basic Cell-type area
 P_{CB} : power consumption of the Cell-Based-type area
 P_{BM} : power consumption of the Basic Cell-type RAM
 P_{CM} : power consumption of the Cell-Based-type memory cell
 P_{IP} : power consumption of the other circuit blocks

6.1.1.1 Power Consumption of the Basic Cell Part (P_{BC}) or Cell-Based Part (P_{CB})

The power consumption of the Basic Cell part (P_{BC}) or Cell-Based part (P_{CB}) is calculated using the equation below.

$$P_{BC} \text{ (or } P_{CB}) = \sum_{i=1}^K (N_b \times f_i \times S_{pi} \times K_{pint}) \quad [\mu W]$$

where, N_b : total number of BCs in the circuit operating at f_i [MHz]
 f_i : operating frequency [MHz]
 S_{pi} : ratio of BCs to N_b that are operating concurrently at f_i [MHz]
 Example: If all circuit blocks operate concurrently at f_i [MHz], S_{pi} is 1.0;
 if 50% of the circuit blocks operate concurrently at f_i [MHz], S_{pi} is 0.5.
 K_{pint} : power consumption per BC

Table 6-1 lists the power-consumption values per BC (K_{pint}) in the S1K70000 series of products.

Table 6-1 Power Consumption per BC (K_{pint}) of the S1K/S1X70000 Series

Type of Transistor	$V_{DD} = 1.8\text{ V}$		$V_{DD} = 1.5\text{ V}$		Unit
	Basic Cell Type	Cell Based Type	Basic Cell Type	Cell Based Type	
Standard 1	0.077	0.054	0.058	0.040	$\mu\text{W}/\text{MHz}$
Standard 2	0.082	0.056	0.059	0.041	
High-Performance	0.090	0.058	0.060	0.042	
Low-Leakage	0.092	0.060	0.061	0.043	

6.1.1.2 Power Consumption of the Basic Cell-Type RAM (P_{BM})

Refer to Section 5.1.7, "Power Consumption of RAM," for details on and the equations for calculating the power-consumption values for the primary products of Basic Cell-type RAMs in the S1K/S1X70000 series.

6.1.1.3 Power Consumption of the Cell-Based-Type RAM (P_{CM})

For the power-consumption values of Cell-Based-type RAMs in the S1K/S1X70000 series, please contact the sales division of Epson.

6.1.1.4 Power Consumption of Other Circuit Blocks (P_{IP})

When you will be using other circuit blocks, contact the sales division of Epson for details on the power-consumption value of each circuit block.

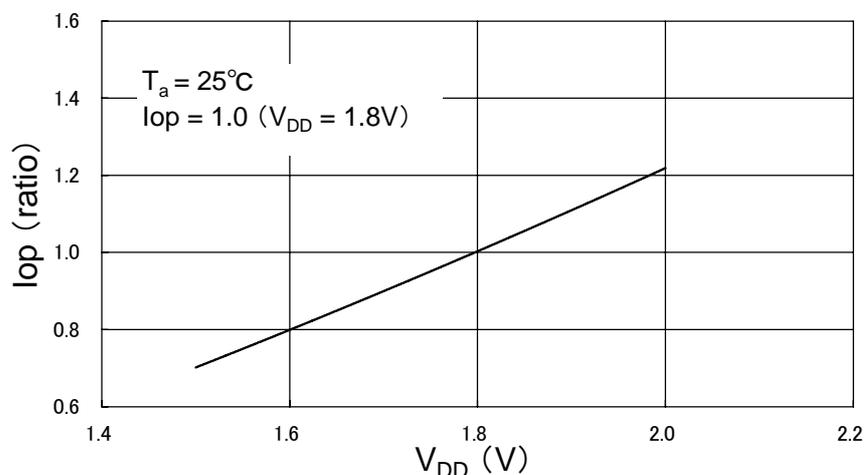


Figure 6-1 Voltage Characteristics of the Power Consumption of MSI

6.1.2 Input Buffers (P_i)

The power consumption of input buffers is obtained as the sum total of the frequencies of the input signals supplied to the respective buffers, f [MHz], multiplied by K_{pi} [$\mu\text{W}/\text{MHz}$].

$$P_i = \sum_{i=1}^K (K_{pi} \times f_i) \quad [\mu\text{W}]$$

where, f_i : operating frequency [MHz]

K_{pi} : voltage coefficient of the input buffer (see Table 6-2)

Table 6-2 K_{pi} for Input Cells in the S1K70000 Series

V_{DD} (Typ.)	3.3-V Buffers (Y Type)	2.5-V Buffers (X Type)	Unit
$HV_{DD} = 3.3 \text{ V}$	2.57	—	$\mu\text{W}/\text{MHz}$
$HV_{DD} = 2.5 \text{ V}$	1.16	1.57	
V_{DD} or $LV_{DD} = 1.8 \text{ V}$	0.62	0.68	
V_{DD} or $LV_{DD} = 1.5 \text{ V}$	0.43	0.45	

6.1.3 Output Buffers (P_o)

The power consumption of output buffers differs between DC load (e.g., resistive load or when connected to TTL devices) and AC load (e.g., capacitive load or when connected to CMOS devices).

If the DC power consumption and AC power consumption are assumed to be P_{DC} and P_{AC} , respectively, then the power consumption of the output buffers to be obtained, P_o , is expressed by the equation below.

$$P_o = P_{AC} + P_{DC}$$

6.1.3.1 AC Power Consumption (P_{AC})

With an AC load, the power consumption of the output buffers can be roughly calculated using the equation below.

$$P_{AC} = \sum_{i=1}^K \{f_i \times C_L \times (V_{DD})^2\}$$

where, f_i : operating frequency of the output buffer [Hz]

C_L : output load capacitance [F]

V_{DD} : power-supply voltage [V]

6.1.3.2 DC Power Consumption (P_{DC})

With a DC load, the power consumption of the output buffers can be roughly calculated using the equation below.

$$P_{DC} = P_{DCH} + P_{DCL}$$

where, $P_{DCH} = |I_{OH}| \times (V_{DD} - V_{OH})$

$P_{DCL} = I_{OL} \times V_{OL}$

Here, the ratio of P_{DCH} to P_{DCL} is determined by the duty cycle of the output signal.

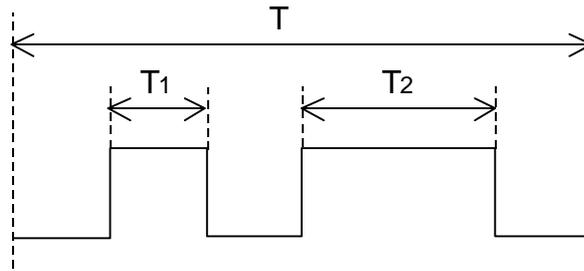


Figure 6-2 Example of a Duty Cycle

Using Figure 6-2 as an example, we find

$$\text{Duty H} = (T_1 + T_2) / T$$

$$\text{Duty L} = (T - T_1 - T_2) / T$$

From the above,

$$P_{DC} = P_{DCH} + P_{DCL}$$

$$= \sum_{i=1}^K \{ (V_{DD}^* - V_{OHi}) \times I_{OHi} \times \text{Duty H} \} + \sum_{i=1}^K [V_{OLi} \times I_{OLi} \times \text{Duty L}]$$

* For dual power supplies, V_{DD} represents HV_{DD} or LV_{DD} .

6.1.4 Example of Calculation of the Approximate Amount of Power Consumption

Calculate the approximate amount of power consumption under the conditions specified below.

- Power-supply voltage : $HV_{DD} / LV_{DD} = 3.3 \text{ V} / 1.8 \text{ V}$
- Type of transistor used : Standard 1
- I/O cells (Y type, all connected to CMOS)
 - Number of HV input cells : 30, operating at 66 MHz
 - Number of HV output cells : 40, operating at 33 MHz, $C_L = 15 \text{ pF}$
(However, 50% operating rate within the same cycle)
 - Number of HV bi-directional cells : 40
(Separated for calculation purposes)
Input-cell equivalent 20, operating at 66 MHz
Output-cell equivalent 20, operating at 33 MHz,
 $C_L = 15 \text{ pF}$
 - Number of LV input cells : 30, operating at 40 MHz
 - Number of LV output cells : 10, operating at 20 MHz, $C_L = 30 \text{ pF}$
- Basic Cell-type 2-port RAM : 256 words x 16 bits, 4 pcs., operating at 66 MHz
128 words x 8 bits, 6 pcs., operating at 66 MHz
- Cell-Based Logic : 640k
300k, operating at 66 MHz, circuit operation rate: 30%
340k, operating at 50 MHz, circuit operation rate: 30%

First calculate the power consumption in the HV_{DD} block of the circuit.

In the example circuit used here, the power consumption in the HV_{DD} block consists entirely of the power consumed by the I/O cells. First, we'll calculate the power consumption of the input buffers.

From Table 6-2, K_{pi} = 2.57 [μW/MHz] when HV_{DD} = 3.3 V. Therefore,

$$\begin{aligned}
 P_i &= 2.57 \text{ [}\mu\text{W/MHz]} \times 66 \text{ [MHz]} \times (30 + 20) \\
 &= 8481 \text{ [}\mu\text{W]} \\
 &= 8.481 \text{ [mW]} \dots\dots\dots (1)
 \end{aligned}$$

Next, calculate the power consumption of the output buffers.

Because all of the circuit is connected to CMOS Interface, calculate the approximate amount of power consumption in terms of AC power consumption (P_{AC}).

$$\begin{aligned}
 P_o &= 33 \times 10^6 \text{ [Hz]} \times 15 \times 10^{-12} \text{ [F]} \times 3.3^2 \times (40 \times 0.5) + 33 \times 10^6 \text{ [Hz]} \times 15 \times 10^{-12} \text{ [F]} \\
 &\quad \times 3.3^2 \times 20 \\
 &= 0.2156 \text{ [W]} \\
 &= 215.6 \text{ [mW]} \dots\dots\dots (2)
 \end{aligned}$$

Therefore, the approximate amount of power consumption in the HV_{DD} block of the circuit, P_(HVDD), is

$$\begin{aligned}
 P_{(HVDD)} &= P_i + P_o = (1) + (2) \\
 &= 8.481 + 215.6 \\
 &= 224.081 \\
 &\cong 224 \text{ [mW]} \dots\dots\dots (I)
 \end{aligned}$$

Next, calculate the approximate amount of power consumption in the LV_{DD} block of the circuit, P_(LVDD), by following the procedure described below.

(1) Power consumption of the Cell-Based area

Because the 300k-gate area and 340k-gate area operate at 66 MHz and 50 MHz, respectively, and because their circuit operation rates are 30%, the power consumption of the Cell-Based area to be obtained, P_{CB}, is expressed by the equation below. (For the Standard-1 Cell-Based part, K_{pint} = 0.054 [μW/MHz/BC])

$$\begin{aligned}
 P_{CB} &= \sum_{i=1}^K (N_b \times f_i \times S_{pi} \times K_{pint}) \text{ [}\mu\text{W]} \\
 &= (300000 \times 66 \times 0.3 \times 0.054) + (340000 \times 50 \times 0.3 \times 0.054) \text{ [}\mu\text{W]} \\
 &= 320.67 \text{ [mW]} + 275.4 \text{ [mW]} \\
 &= 596.16 \text{ [mW]} \dots\dots\dots (1)
 \end{aligned}$$

(2) Power Consumption of Basic Cell-Type 2-Port RAM

From Table 5-111 in Chapter 5, "Power Consumption of RAM," the power consumption of 2-port RAM is

- 151.79 [μW/MHz] for 256 words x 16 bits
- 70.79 [μW/MHz] for 128 words x 8 bits

Therefore, the power consumption of RAM, P_{BM}, is obtained by the equation below.

$$\begin{aligned}
 P_{BM} &= 151.79 \times 66 \times 4 + 70.79 \times 66 \times 6 \text{ [}\mu\text{W]} \\
 &= 40.07 \text{ [mW]} = 28.03 \text{ [mW]} \\
 &= 68.1 \text{ [mW]}
 \end{aligned}$$

(3) Power consumption in I/O cells

First, calculate the power consumption of the input buffers.

From Table 6-2, $K_{pi} = 0.62$ [$\mu\text{W}/\text{MHz}$] for $\text{LV}_{\text{DD}} = 1.8$ V. Therefore,

$$\begin{aligned} P_i &= 0.62 \text{ } [\mu\text{W}/\text{MHz}] \times 40 \text{ } [\text{MHz}] \times 30 \\ &= 744 \text{ } [\mu\text{W}] \\ &= 0.744 \text{ } [\text{mW}] \dots\dots\dots (3) \end{aligned}$$

Next, calculate the power consumption of the output buffers.

Because the entire circuit is connected to CMOS Interface, calculate the approximate amount of power consumption in terms of AC power consumption (P_{AC}).

$$\begin{aligned} P_o &= 20 \times 10^6 \text{ } [\text{Hz}] \times 30 \times 10^{-12} \text{ } [\text{F}] \times 1.8^2 \times 10 \\ &= 0.01944 \text{ } [\text{W}] \\ &= 19.4 \text{ } [\text{mW}] \dots\dots\dots (4) \end{aligned}$$

Therefore, the approximate amount of power consumption in the LV_{DD} block of the circuit, $P_{(\text{LVDD})}$, is

$$\begin{aligned} P_{(\text{LVDD})} &= (1) + (2) + (3) + (4) \\ &= 596.16 + 68.1 + 0.744 + 19.4 \\ &= 684.4 \text{ } [\text{mW}] \end{aligned}$$

As a result, the approximate amount of power consumed in this circuit is as follows:

$P_{(\text{HV}_{\text{DD}} = 3.3 \text{ V})}$	224 [mW]
$P_{(\text{LV}_{\text{DD}} = 1.8 \text{ V})}$	684 [mW]

6.1.5 Limitations on Power Consumption

The chip temperature of LSIs increases according to their power consumption. When encapsulated in a package, the LSI's chip temperature may be calculated from its ambient temperature, T_a , the thermal resistance of the package, θ_{j-a} , and the power dissipation of the LSI, PD.

$$\text{Chip temperature } (T_j) = T_a + (\text{PD} \times \theta_{j-a}) \text{ } [^\circ\text{C}]$$

When used under normal conditions, make sure the chip temperature (T_j) is 125°C or less.

See Table 6-3 for the thermal resistance of each type of package. The thermal-resistance values shown in this table vary significantly depending on how the chip is mounted on the board and whether it is forcibly air-cooled.

Table 6-3 Thermal Resistance of Each Type of Package (Suspended Singly)

ALLOY42

Package Type	Pin Counts	0m/sec	1m/sec	2m/sec	3m/sec
		θ_{j-a}	θ_{j-a}	θ_{j-a}	θ_{j-a}
QFP5	100	110(°C/W)	75	60	55
QFP5	128	110	75	60	55
QFP8	128	65	—	—	—
QFP8	208	45	—	—	—
QFP12	48	230	—	—	—
QFP13	64	170	—	—	—
QFP14	80	110	—	—	—
QFP15	100	115	50	45	35
QFP20	144	85	70	50	40
TQFP14	80	100	—	—	—
TQFP14	100	100	—	—	—
TQFP15	100	110	—	—	—

Cu-L/F

Package Type	Pin Counts	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θ_{j-a}	θ_{j-a}	θ_{j-a}	θ_{j-a}
QFP5	80	85(°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	160	45	32	25	23
QFP8	256	50	—	—	—
QFP10	304	35	20	16	—
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	—	—	—
QFP15	100	90	—	—	—
QFP20	184	65	—	—	—
QFP21	176	55	—	—	—
QFP21	216	55	—	—	—
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	—	—	—
QFP23	240	40	—	—	—
TQFP12	48	165	—	—	—
TQFP13	64	140	—	—	—
TQFP15	128	105	—	—	—
TQFP24	144	80	—	—	—
HQFP5	128	60	—	—	—
HQFP8	160	32	19	12	10
H2QFP8	208	34	—	—	—
H2QFP23	240	30	—	—	—
H3QFP15	128	85	—	—	—

CFLGA (mounted on the board, free of wind)

Package Type	Customer's Board Size	Chip Size		
		3.82 mm x 3.82 mm	5.73 mm x 5.73 mm	9.55 mm x 9.55 mm
CFLGA424	75mm	44.0(°C/W)	32.9	24.6
	50mm	46.9	36.4	27.8
	30mm	61.1	50.1	42.1
CFLGA307	75mm	44.0	33.1	24.9
	50mm	47.1	37.4	28.5
	30mm	61.7	51.5	43.1
CFLGA239	75mm	44.0	33.1	25.1
	50mm	47.3	38.3	29.2
	30mm	62.2	52.9	43.9
CFLGA152	75mm	44.8	34.4	—
	50mm	48.8	39.7	—
	30mm	63.3	53.9	—
CFLGA104	75mm	45.5	35.6	—
	50mm	50.3	41.1	—
	30mm	64.3	54.9	—

PBGA

Package Type	Pin Counts	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θ_{j-a}	θ_{j-a}	θ_{j-a}	θ_{j-a}
PBGA	225	72(°C/W)	46	37	—
PBGA	256	53	33	25	—
PBGA	388	45	—	—	—

6.2 Propagation Delay Time

6.2.1 Accuracy of the Propagation Delay Time

The propagation delay time, T_{pd} , varies with the LSI's power-supply voltage, ambient temperature, and process conditions. It also varies with circuit configurations such as the output load (e.g., wiring capacitance or fan-out counts), distorted input waveforms, input logic levels, and mirror effects.

For the S1K/S1X70000 series, a delay calculator has been introduced that helps minimize these fluctuating factors, in order to provide a highly accurate delay-time calculation environment. Therefore, be aware that the results obtained using this delay calculator do not necessarily match the propagation delay times calculated by customers from the values listed in the "S1K70000-/S1X70000-Series Cell Library" by following the simplified calculation procedure described below.

6.2.2 Calculating the Propagation Delay Time

The calculation formulas shown below provide a simple means of calculating the propagation delay time. This calculation formula is such that the larger the load capacitance, the greater the delay error, so that the resulting values are smaller than those obtained using the delay calculator. Therefore, the values calculated here can only be used as a guide.

(1) Delay time of input cells and internal cells

The delay time of input cells and internal cells, T_{pd} , is calculated as the sum total of the cell's inherent delay time when nonloaded, T_0 , and the load delay caused by the wiring load capacitance and input load capacitance connected to the cell outputs. Consequently, the propagation delay time, T_{pd} , is calculated using the equation below.

$$T_{pd} = T_0 + K \times (\Sigma \text{Load A} + \text{Load B}) \dots\dots\dots \text{(Equation 6-1)}$$

where, T_0 : cell's inherent delay when nonloaded [ps]
 K : load delay coefficient [ps/LU]
 Load A : input capacitance of the connected cell [LU]
 Load B : wiring load capacitance [LU]

Note 1: The values of T_0 and K vary with the LSI's operating voltage, ambient temperature, and process conditions. For these parameters, use the values listed in the "S1K70000-/S1X70000-Series Cell Library."

Note 2: The unit "LU" stands for Load Unit. In the S1K70000 series, the gate capacitance at the input pin of the inverter cell (L1INX1) is defined as 1 LU.

(2) Delay time of the output cells

The delay time of the output cells, T_{pd} , is calculated from the output cell's inherent delay time when nonloaded, T_0 , and the load capacitance connected to the external output pins, C_L , by using the equation below.

$$T_{pd} = T_0 + K \times C_L / 10 \dots\dots\dots \text{(Equation 6-2)}$$

where, T_0 : output cell's inherent delay when nonloaded [ps]
 K : output cell's load delay coefficient [ps/10 pF]
 C_L : load capacitance connected to the external output pins [pF]

6.2.3 Virtual Wiring Capacitance

As placement and routing performed in the circuit design phase are not based on the circuit's connection information, the length of the wiring connected as a load to the circuit has not yet been determined. For this reason, in the pre-placement and routing stages, the propagation delay time is calculated using the wiring capacitances (referred to as the "virtual wiring capacitances") that have been prepared through statistical processing.

For the S1K/S1X70000 series, this information is provided for each type of transistor as the virtual wiring capacitances per branch of output in each wiring layer, classified by gate or grid counts. These virtual wiring capacitances are listed in Tables 6-4 through 6-6.

Table 6-4 Virtual Wiring Capacitances per Branch when Using L1/L2/L4-Type Transistors
(Unit: LU)

Gate counts	3-layer wiring	4-layer wiring	5-layer wiring	6-layer wiring
1000	2.107	2.131	2.208	2.249
5000	2.113	2.138	2.215	2.256
10000	2.122	2.146	2.224	2.265
20000	2.138	2.163	2.241	2.283
40000	2.171	2.197	2.276	2.318
60000	2.205	2.230	2.311	2.354
80000	2.238	2.264	2.346	2.389
100000	2.271	2.297	2.381	2.425
200000	2.437	2.465	2.555	2.602
400000	2.769	2.801	2.903	2.957
600000	3.101	3.137	3.251	3.311
800000	3.433	3.473	3.599	3.666
1000000	3.765	3.809	3.947	4.020
1200000	4.098	4.145	4.295	4.375
1400000	4.430	4.481	4.643	4.729
1600000	4.762	4.817	4.991	5.084
1800000	5.094	5.153	5.339	5.438
2000000	5.426	5.489	5.688	5.793

Table 6-5 Virtual Wiring Capacitances per Branch when Using an L3-Type Transistor (Unit: LU)

Gate counts	3-layer wiring	4-layer wiring	5-layer wiring	6-layer wiring
1000	2.160	2.180	2.249	2.273
5000	2.167	2.187	2.256	2.280
10000	2.175	2.196	2.265	2.289
20000	2.192	2.213	2.282	2.307
40000	2.226	2.247	2.318	2.343
60000	2.260	2.282	2.353	2.378
80000	2.294	2.316	2.389	2.414
100000	2.328	2.350	2.424	2.450
200000	2.499	2.522	2.601	2.629
400000	2.839	2.866	2.956	2.988
600000	3.180	3.210	3.310	3.346
800000	3.520	3.553	3.665	3.704
1000000	3.861	3.897	4.019	4.062
1200000	4.201	4.241	4.374	4.421
1400000	4.542	4.585	4.728	4.779
1600000	4.882	4.928	5.083	5.137
1800000	5.222	5.272	5.437	5.495
2000000	5.563	5.616	5.792	5.854

Table 6-6 Virtual Wiring Capacitances per Branch when Using K1/K2/K3/K4-Type Transistors (Unit: LU)

Gate counts	3-layer wiring	4-layer wiring	5-layer wiring	6-layer wiring
3000	2.321	2.353	2.388	2.393
15000	2.329	2.360	2.396	2.400
30000	2.338	2.369	2.405	2.410
60000	2.356	2.388	2.424	2.429
120000	2.393	2.425	2.461	2.466
180000	2.429	2.462	2.499	2.504
240000	2.466	2.499	2.537	2.542
300000	2.502	2.536	2.574	2.580
600000	2.685	2.722	2.763	2.768
1200000	3.051	3.093	3.139	3.145
1800000	3.417	3.463	3.516	3.523
2400000	3.783	3.834	3.892	3.900
3000000	4.149	4.205	4.269	4.277
3600000	4.515	4.576	4.645	4.654
4200000	4.881	4.947	5.021	5.032
4800000	5.247	5.318	5.398	5.409
5400000	5.613	5.689	5.774	5.786
6000000	5.979	6.060	6.151	6.163

Examples of calculation of the propagation delay time

(1) Delay time of input cells and internal cells

The following describes the procedure for calculating the approximate amount of propagation delay time in each path, using the circuits in Figure 6-3 as an example. Table 6-7 lists various characteristic values excerpted from the “S1K70000-/S1X70000-Series Cell Library.” The circuits shown below consist of L1-type transistors, amounting to a total of 20,000 gates in circuit size.

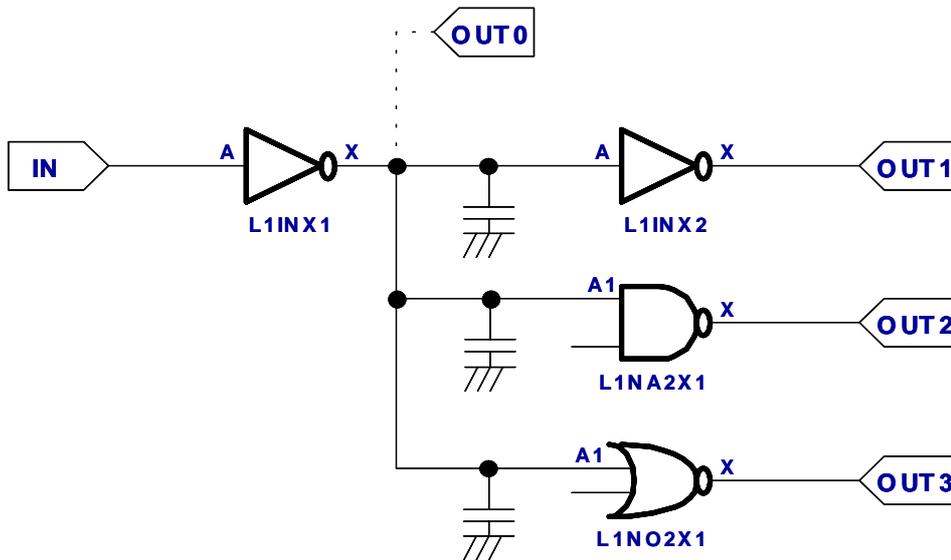


Figure 6-3 Example Circuits for Calculation of the Internal Cell Propagation Delay Time

Table 6-7 Delay Characteristics of Each Cell (Power-Supply Voltage: 1.8 V)

Cell	Input		Output		Delay Characteristics (Typ.)				
	Pin	Fan-in [LU]	Pin	Fan-out [LU]	From	To	Parameter	T ₀ [ps]	K [ps/LU]
L1INX1	A	1.0	X	12.9	A	X	t _{pLH}	33	19.1
							t _{pHL}	19	7.1
L1INX2	A	2.1	X	25.8	A	X	t _{pLH}	43	9.5
							t _{pHL}	22	3.6
L1NA2X1	A1	1.0	X	12.6	A	X	t _{pLH}	54	19.2
							t _{pHL}	32	11.7
L1NO2X1	A1	0.9	X	6.2	A	X	t _{pLH}	79	39.4
							t _{pHL}	23	7.1

L1INX2 (pin A), L1NA2X1 (pin A1), and L1NO2X1 (pin A1) are connected to output pin X of the cell L1INX1. Therefore, from Table 6-7, the total amount of the input load capacitance of the cells, Load A, is found to be as follows:

$$\begin{aligned} \Sigma \text{ Load A} &= \text{L1INX2 (fan-in of pin A)} + \text{L1NA2X1 (fan-in of pin A1)} + \\ &\quad \text{L1NO2X1 (fan-in of pin A1)} \\ &= 2.1 + 1.0 + 0.9 = 4.0 \text{ [LU]} \end{aligned}$$

In addition, the wiring load capacitance, Load B, is calculated using the virtual wiring capacitances. Here, assuming that placement and routing are performed using 3-layer wiring, the virtual wiring capacitances of L1-type transistors 20,000 gates in circuit size are found to be 2.138 [LU] from Table 6-4. Because output pin X of the cell L1INX1 branches to three inputs, the wiring load capacitance, Load B, is calculated as follows:

$$\text{Load B} = 2.138 \times 3 = 6.414 \text{ [LU]}$$

Therefore, the delay in L1INX1 under Typ. conditions is calculated using Equation 6-1 as shown below.

Here, the symbol “↑” denotes the rise, and the symbol “↓” denotes the fall. The rise and fall here refer to the rising and falling transitions at output pin X.

$$\begin{aligned} T_{pd} (A \downarrow \rightarrow X \uparrow) &= T_0 (\uparrow) + K (\uparrow) \times (\Sigma \text{ Load A} + \text{Load B}) \\ &= 33 + 19.1 \times (4.0 + 6.414) \\ &= 231.9 \text{ [ps]} \end{aligned}$$

$$\begin{aligned} T_{pd} (A \uparrow \rightarrow X \downarrow) &= T_0 (\downarrow) + K (\downarrow) \times (\Sigma \text{ Load A} + \text{Load B}) \\ &= 19 + 7.1 \times (4.0 + 6.414) \\ &= 92.9 \text{ [ps]} \end{aligned}$$

Next, calculate the path delay from IN to OUT1, OUT2, and OUT3. In this case, because OUT1, OUT2, and OUT3 are in a nonloaded state, the cell's inherent delay must be added to the above delay value. In the calculation of this path delay, furthermore, care must be taken with respect to the rise and fall of each output.

1) Delay in IN → OUT1 path = L1INX1 (A → X delay) + L1INX2 (A → X delay)

$$\begin{aligned} T_{pd} (IN \uparrow \rightarrow OUT1 \uparrow) &= T_{pd} (IN \uparrow \rightarrow OUT0 \downarrow) + T_{pd} (OUT0 \downarrow \rightarrow OUT1 \uparrow) \\ &= 92.9 + 43 \\ &= 135.9 \text{ [ps]} \end{aligned}$$

$$\begin{aligned} T_{pd} (IN \downarrow \rightarrow OUT1 \downarrow) &= T_{pd} (IN \downarrow \rightarrow OUT0 \uparrow) + T_{pd} (OUT0 \uparrow \rightarrow OUT1 \downarrow) \\ &= 231.9 + 22 \\ &= 253.9 \text{ [ps]} \end{aligned}$$

2) Delay in IN → OUT2 path = L1INX1 (A → X delay) + L1NA2X1 (A1 → X delay)

$$\begin{aligned} T_{pd} (IN \uparrow \rightarrow OUT2 \uparrow) &= T_{pd} (IN \uparrow \rightarrow OUT0 \downarrow) + T_{pd} (OUT0 \downarrow \rightarrow OUT2 \uparrow) \\ &= 92.9 + 54 \\ &= 146.9 \text{ [ps]} \end{aligned}$$

$$\begin{aligned} T_{pd} (IN \downarrow \rightarrow OUT2 \downarrow) &= T_{pd} (IN \downarrow \rightarrow OUT0 \uparrow) + T_{pd} (OUT0 \uparrow \rightarrow OUT2 \downarrow) \\ &= 231.9 + 32 \\ &= 263.9 \text{ [ps]} \end{aligned}$$

3) Delay in IN → OUT3 path = L1INX1 (A → X delay) + L1NO2X1 (A1 → X delay)

$$\begin{aligned} T_{pd} (IN \uparrow \rightarrow OUT3 \uparrow) &= T_{pd} (IN \uparrow \rightarrow OUT0 \downarrow) + T_{pd} (OUT0 \downarrow \rightarrow OUT3 \uparrow) \\ &= 92.9 + 79 \\ &= 171.9 \text{ [ps]} \end{aligned}$$

$$\begin{aligned} T_{pd} (IN \downarrow \rightarrow OUT3 \downarrow) &= T_{pd} (IN \downarrow \rightarrow OUT0 \uparrow) + T_{pd} (OUT0 \uparrow \rightarrow OUT3 \downarrow) \\ &= 231.9 + 23 \\ &= 254.9 \text{ [ps]} \end{aligned}$$

(2) Delay time of output cells

The following describes the procedure for calculating the approximate amount of propagation delay time, using the circuits in Figure 6-4 as an example. The output pin has a capacitance of 100 pF added external to the chip.

Table 6-8 lists various characteristic values of dual-power-supply output cells excerpted from the cell library.

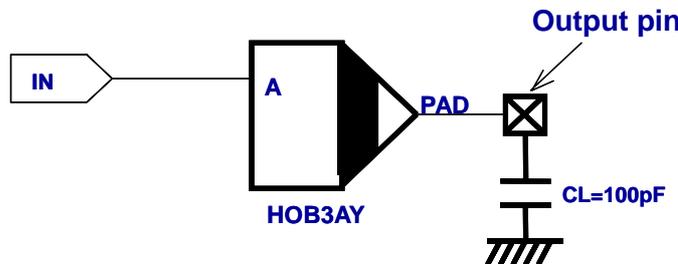


Figure 6-4 Example Circuit for Calculation of the External Cell Propagation Delay Time

Table 6-8 Delay Characteristics of Output Cells (Power Supply HV_{DD} = 3.3 V / LV_{DD} = 1.8 V)

Cell Name	Input		Output		Delay Characteristics (Typ.)				
	Pin	Fan-in [LU]	Pin	Fan-out [LU]	From	To	Parameter	T ₀ [ps]	K [ps/10pF]
HOB3AY	A	10.0	PAD	—	A	PAD	t _{pLH}	984	296.3
							t _{pHL}	1071	332.6

The delay time in the output cell HOB3AY under Typ. conditions is calculated using Equation 6-2, as shown below.

Here, the symbol “↑” denotes a rise, and the symbol “↓” denotes a fall. Here, these refer to the rising and falling transitions at the PAD for the output pin.

$$\begin{aligned}
 T_{pd} (IN\uparrow \rightarrow PAD\uparrow) &= T_0 (\uparrow) + K (\uparrow) \times 100 \text{ (pF)} / 10 \\
 &= 984 + 296.3 \times 100 \text{ (pF)} / 10 \\
 &= 3947 \text{ [ps]}
 \end{aligned}$$

$$\begin{aligned}
 T_{pd} (IN\downarrow \rightarrow PAD\downarrow) &= T_0 (\downarrow) + K (\downarrow) \times 100 \text{ (pF)} / 10 \\
 &= 1071 + 332.6 \times 100 \text{ (pF)} / 10 \\
 &= 4397 \text{ [ps]}
 \end{aligned}$$

6.2.4 Setup and Hold Times of the Flip-Flop (FF)

If the configured circuit is to operate properly with the desired logic, the timing of the signals applied to the sequential circuit of the FF or of an MSI built with FFs is important. The setup and hold times of FFs are closely related to this signal timing. Any data that is supplied after the setup time or that has changed state within the hold time cannot be written into the FF circuit properly. Therefore, these setup and hold times must be taken into consideration in the timing design.

(1) Minimum pulse width

This refers to the minimum length of time or the width from the leading to the trailing edge of an input pulse waveform in an FF or an MSI built with FFs. If a pulse narrower than that value is applied to the input, it may not only have no effect as a signal, but may also cause the FF to operate erratically.

There are the following three definitions of the minimum pulse width:

- Minimum pulse width of a clock signal
- Minimum pulse width of a set signal
- Minimum pulse width of a reset signal

(2) Setup time

For data to be properly read into an FF or an MSI built with FFs, the state of the data must be set before the active edge of the clock pulse changes. The time required for this is referred to as the “setup time.”

(3) Hold time

For data to be properly read into an FF or an MSI built with FFs, the state of the data must be maintained for some time after the active edge of the clock pulse is entered. The time required for this is referred to as the “hold time.”

(4) Release time (setup)

A finite length of time must elapse before the clock pulse can change state after the state of the set/reset input is released in an FF or an MSI built with FFs. This time is referred to as the “release time (setup).”

(5) Removal time (hold)

The state of the set/reset input must be maintained for some time after the clock pulse is entered in an FF or an MSI built with FFs. This time is referred to as the “removal time (hold).”

(6) Set/reset setup time (recovery)

A finite length of time must elapse before the reset input can be driven high after the state of the set input is released in an FF or an MSI built with FFs. This time is referred to as the “set/reset setup time.”

(7) Set/reset hold time (recovery)

The signal state must be maintained for some time before the set signal is driven high after the reset signal is driven high in an FF or an MSI built with FFs. This time is referred to as the “set/reset hold time.”

For details regarding the timing error message during the simulation, refer to the manual of each tool.

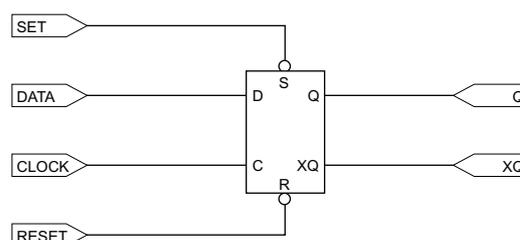


Figure 6-5 L1DFSRX1

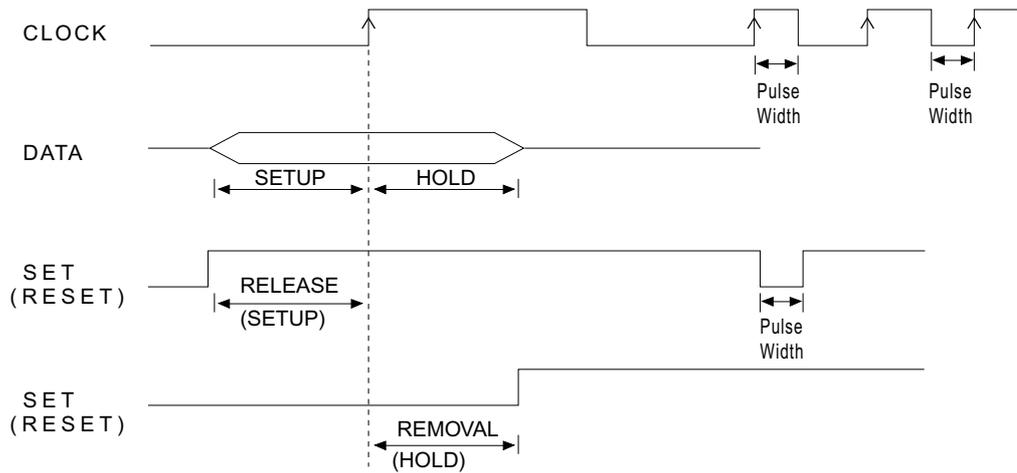


Figure 6-6 Timing Waveform 1 (for Definitions (1) to (5))

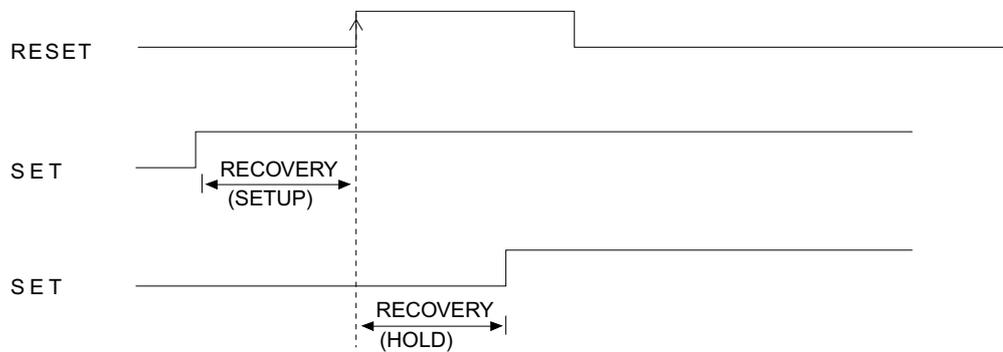


Figure 6-7 Timing Waveform 2 (for Definitions (6) to (7))

The setup/hold times of FFs in the S1K/S1X70000 series are listed in the “S1K70000-/S1X70000-Series MSI Cell Library” in the form shown in Table 6-9. When actually using the S1K70000-series standard cells, please refer to the characteristics of each cell.

Table 6-9 Timing Characteristics of L1DFSRX1 (Reference)

Pin	Setup time (ps)	Hold time (ps)	Pulsewidth (ps)
	Typ. ($V_{DD} = 1.8\text{ V}$)	Typ. ($V_{DD} = 1.8\text{ V}$)	Typ. ($V_{DD} = 1.8\text{ V}$)
C \uparrow to D	370	103	—
C \uparrow to R \uparrow	177	323	—
C \uparrow to S \uparrow	229	223	—
R \uparrow to S \uparrow	203	—	—
S \uparrow to R \uparrow	209	—	—
C \downarrow	—	—	479
C \downarrow	—	—	490
R \downarrow	—	—	362
S \downarrow	—	—	418

Notes P = transition from 0 to 1 level or Positive pulse
 N = transition from 1 to 0 level or Negative pulse
 $T_a = -40$ to $+85^\circ\text{C}$

6.3 Input/Output Buffer Characteristics (3.3-V Buffers: Y Type)

6.3.1 Input Buffer Characteristics

Standard-Cell Input Buffers

- 3.3 V ± 0.3 V

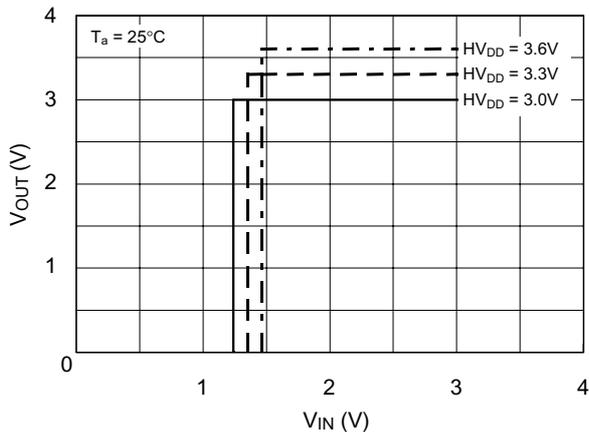


Figure 6-8 Input Characteristics (LVTTTL)

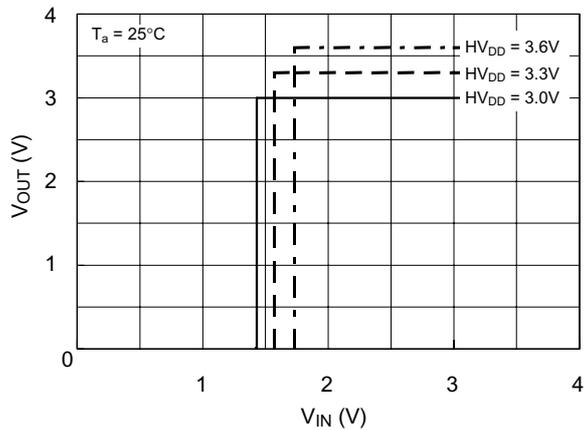


Figure 6-9 Input Characteristics (LVCMOS)

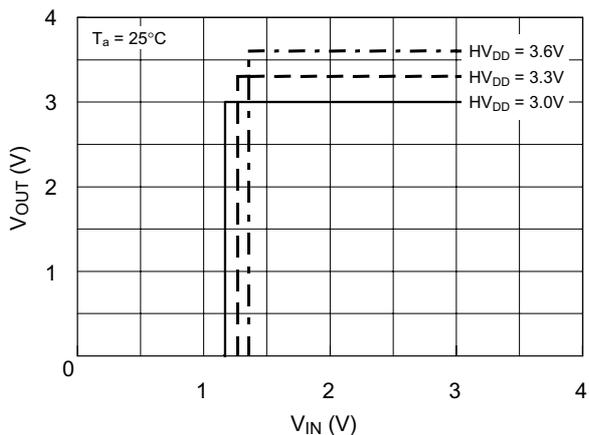


Figure 6-10 Input Characteristics (PCI-3V)

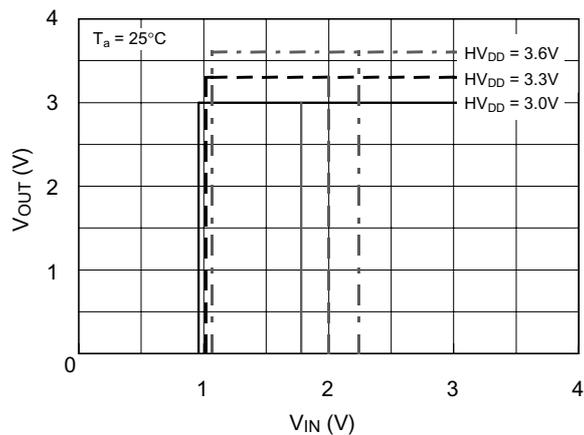


Figure 6-11 Input Characteristics (LVCMOS Schmitt)

● 2.5 V ± 0.2 V

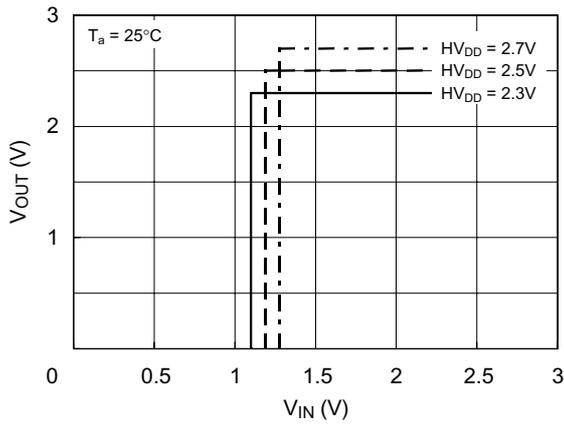


Figure 6-12 Input Characteristics (LVCMOS)

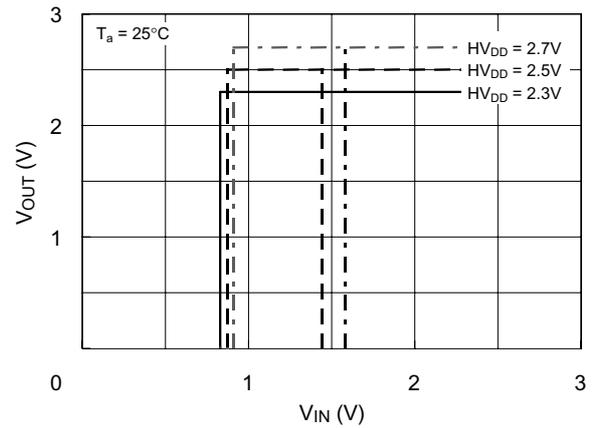


Figure 6-13 Input Characteristics (LVCMOS Schmitt)

● 1.8 V ± 0.15 V

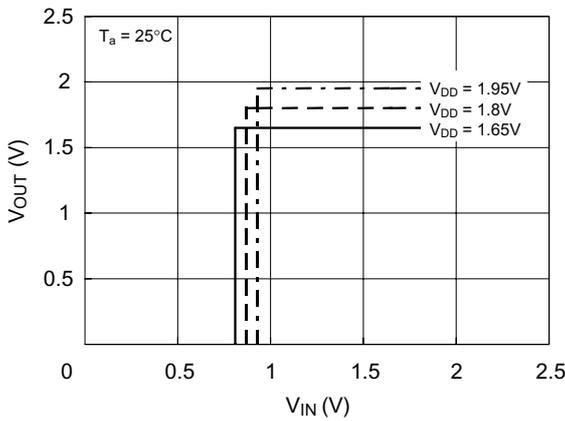


Figure 6-14 Input Characteristics (LVCMOS)

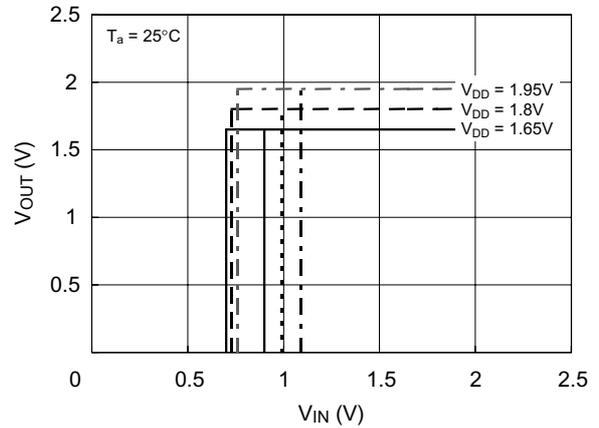


Figure 6-15 Input Characteristics (LVCMOS Schmitt)

● 1.5 V ± 0.1 V

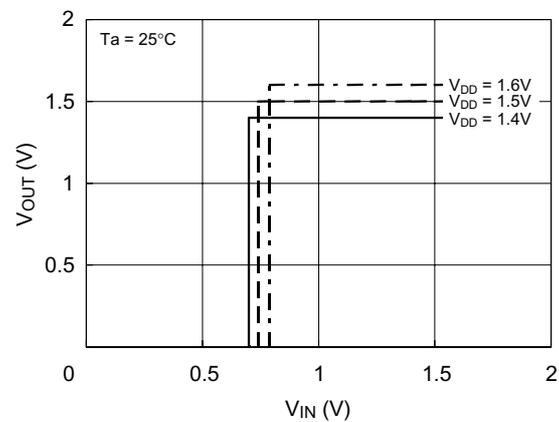


Figure 6-16 Input Characteristics (LVCMOS)

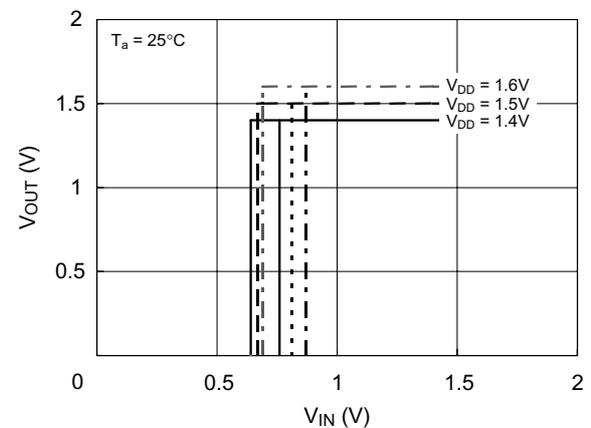


Figure 6-17 Input Characteristics (LVCMOS Schmitt)

6.3.1.1 Input Through Current

- 3.3 V ± 0.3 V

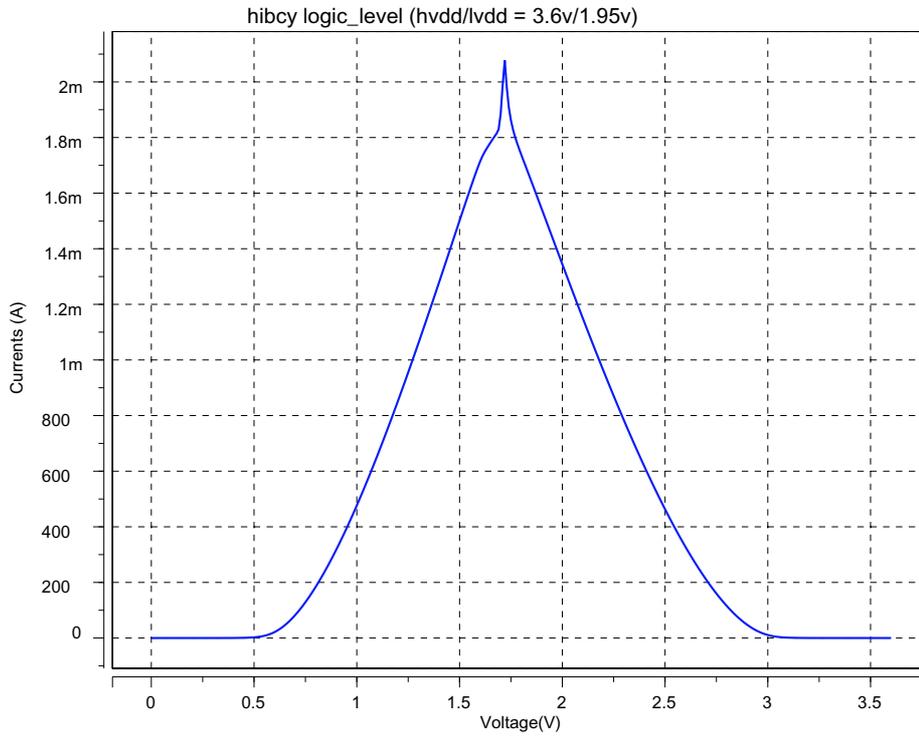


Figure 6-18 Input Through Current (LVC MOS)

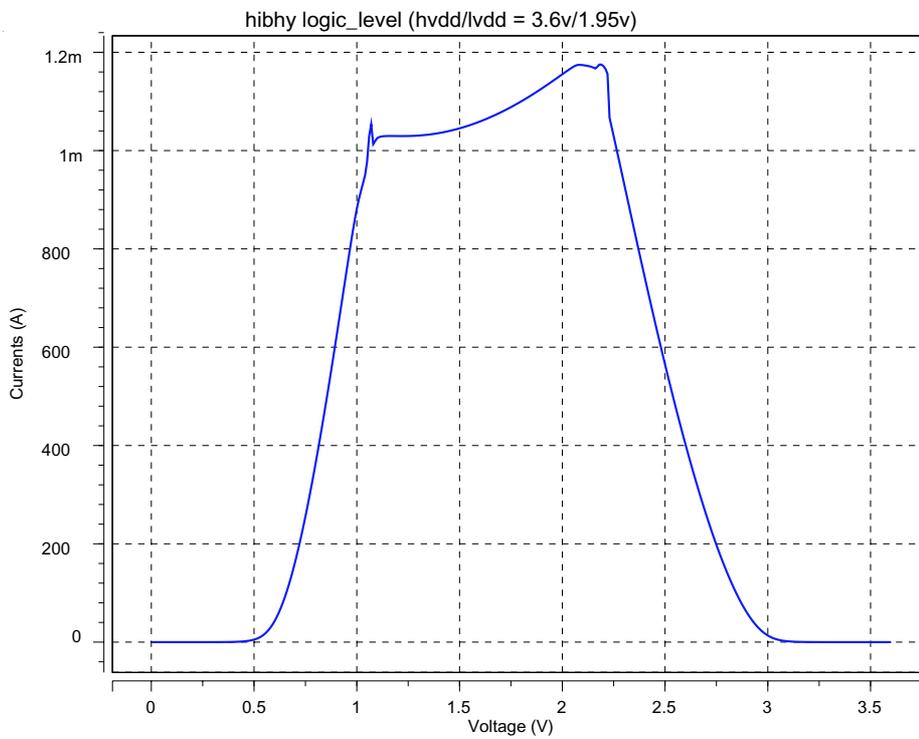


Figure 6-19 Input Through Current (LVC MOS Schmitt)

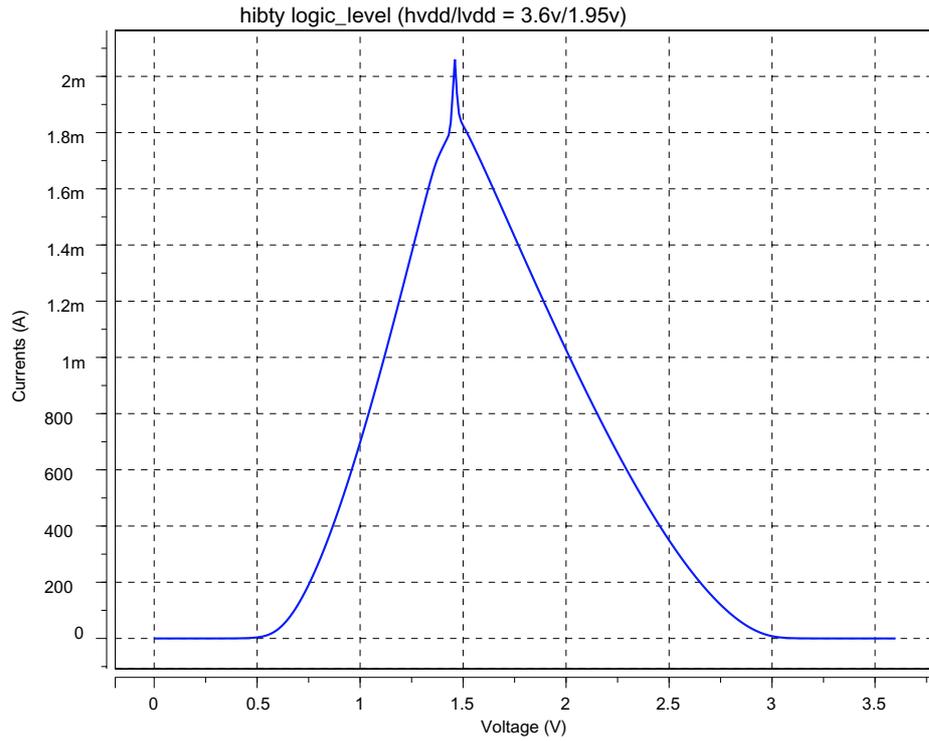


Figure 6-20 Input Through Current (LVTTL)

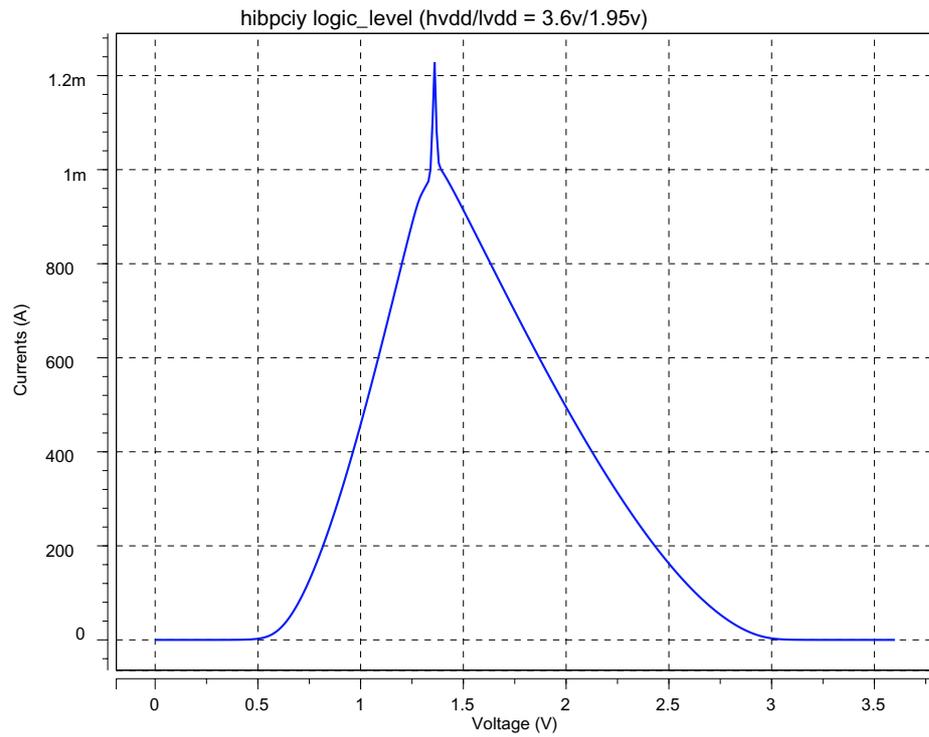


Figure 6-21 Input Through Current (PCI)

- 2.5 V ± 0.2 V

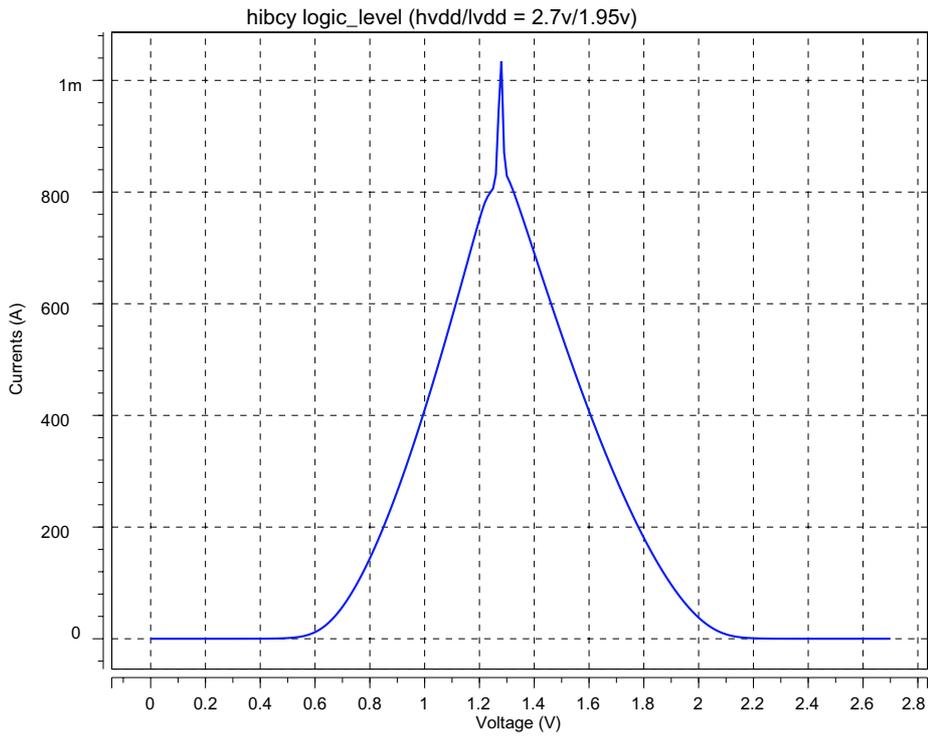


Figure 6-22 Input Through Current (LVCMOS)

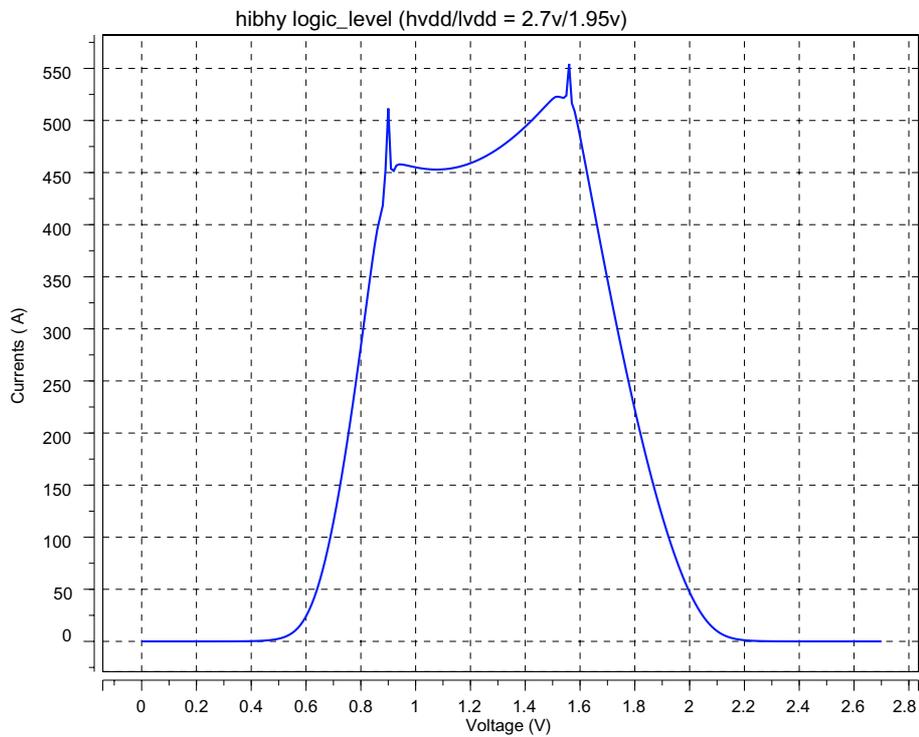


Figure 6-23 Input Through Current (LVCMOS Schmitt)

● $1.8\text{ V} \pm 0.15\text{ V}$

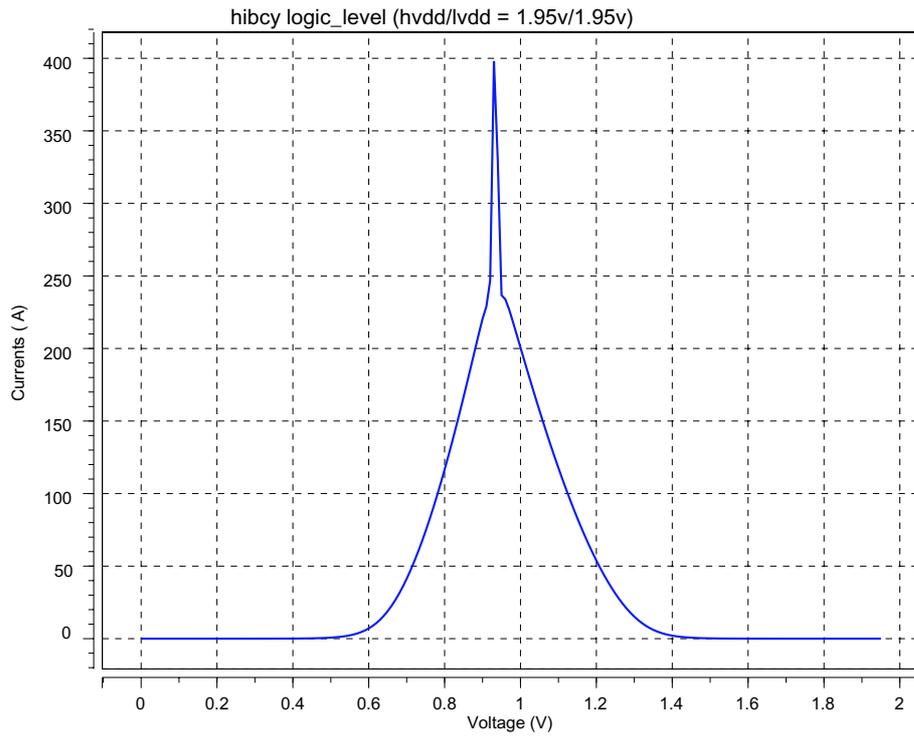


Figure 6-24 Input Through Current (LVCMOS)

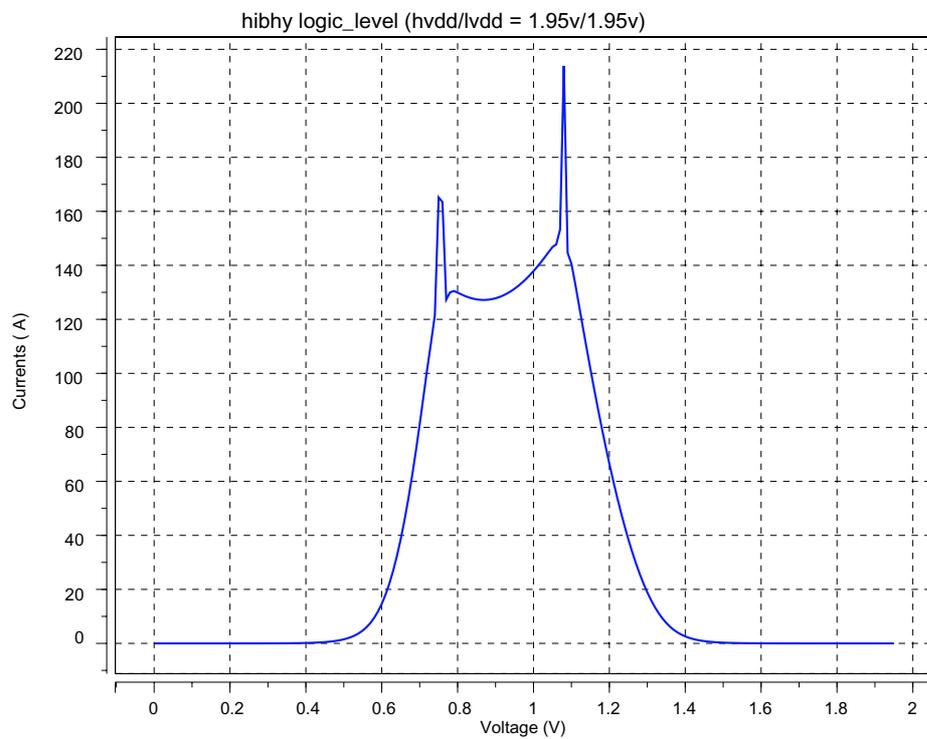


Figure 6-25 Input Through Current (LVCMOS Schmitt)

- 1.5 V \pm 0.1 V

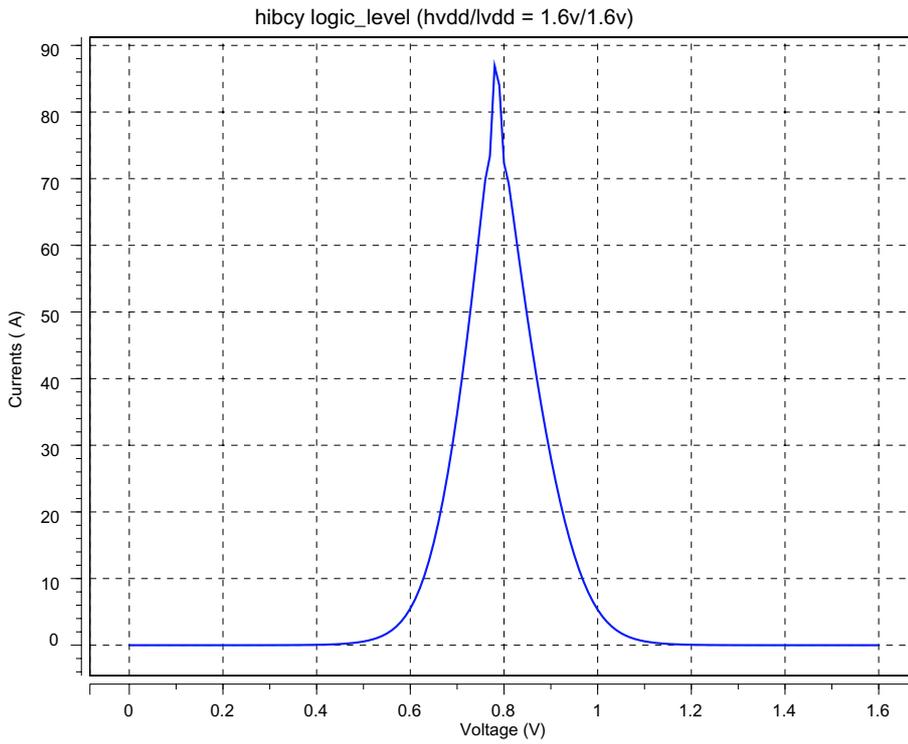


Figure 6-26 Input Through Current (LVCMOS)

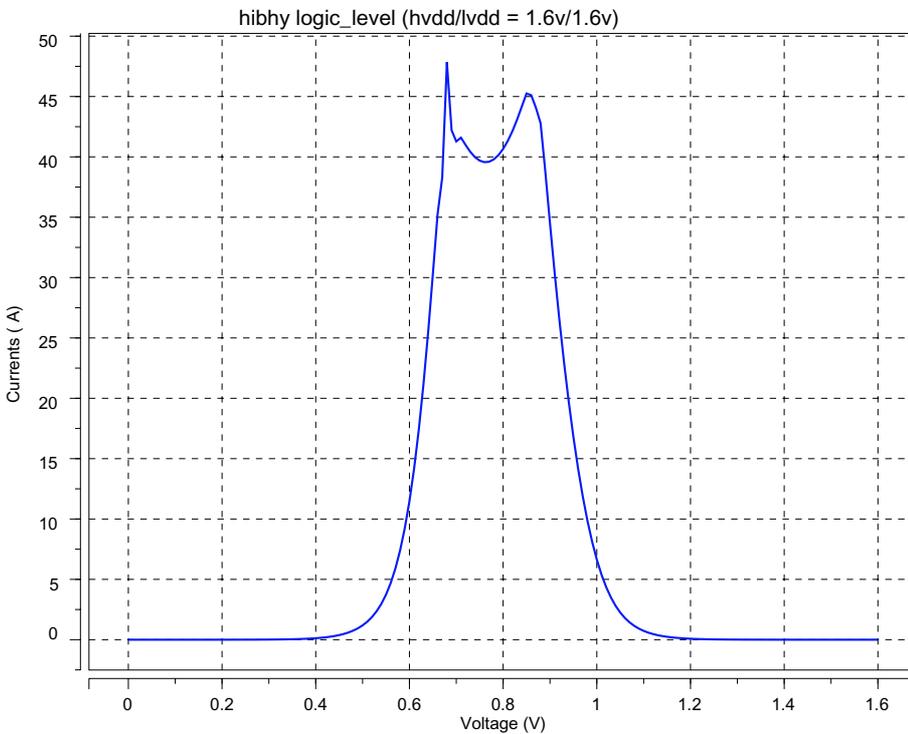


Figure 6-27 Input Through Current (LVCMOS Schmitt)

6.3.2 Output Buffer Characteristics

- (1) List of output buffer specifications

Table 6-10 Output Current Characteristics (Y Type)

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}				Unit
	HV _{DD} = 3.3 V	HV _{DD} = 2.5 V	V _{DD} or LV _{DD} = 1.8 V	V _{DD} or LV _{DD} = 1.5 V	
Type 1	-2/2	-1.5/1.5	-1/1	-0.75/0.75	mA
Type 2	-4/4	-3/3	-2/2	-1.5/1.5	mA
Type 3	-8/8	-6/6	-4/4	-3/3	mA
Type 4	-12/12	-9/9	-6/6	-4.5/4.5	mA

Notes *1: V_{OH} = power-supply voltage - 0.4 V (Power-supply voltage = 3.3 V, 2.5 V, 1.8 V, or 1.5 V)

*2: V_{OL} = 0.4 V (Power-supply voltage = 3.3 V, 2.5 V, 1.8 V, or 1.5 V)

(2) $I_{OL}-V_{OL}$, $I_{OH}-V_{OH}$

$I_{OL}-V_{OL}$

● $3.3\text{ V} \pm 0.3\text{ V}$

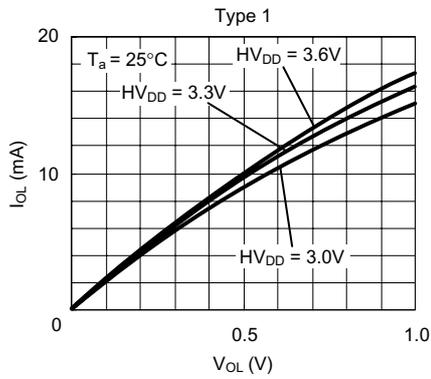


Figure 6-28

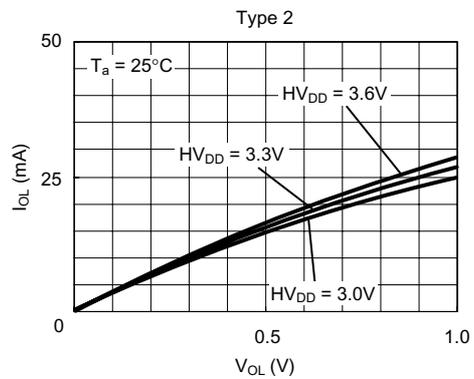


Figure 6-29

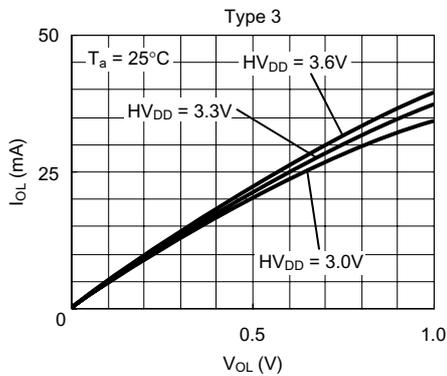


Figure 6-30

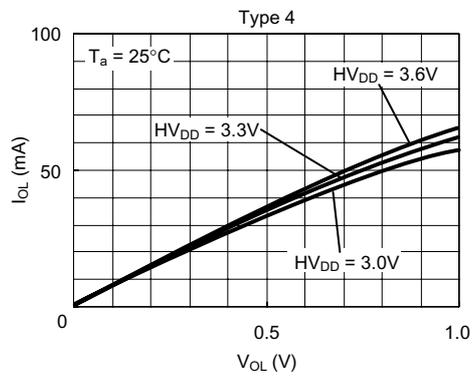


Figure 6-31

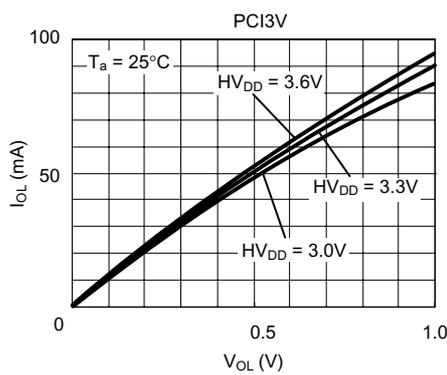


Figure 6-32

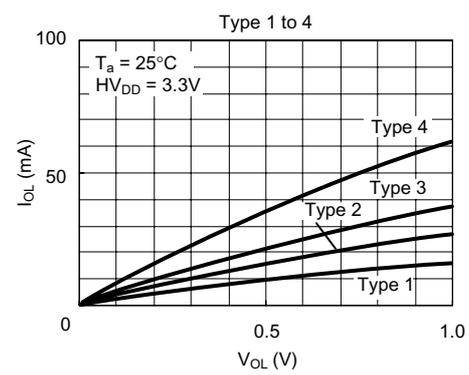


Figure 6-33

● 2.5 V ± 0.2 V

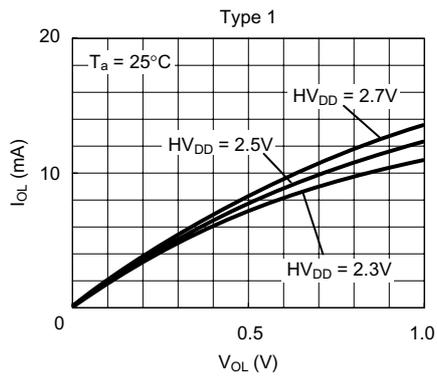


Figure 6-34

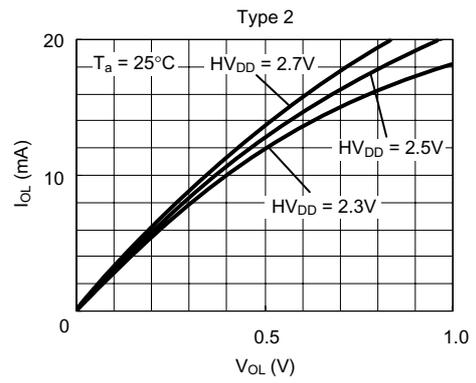


Figure 6-35

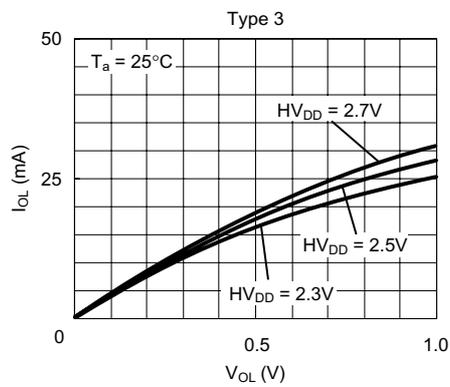


Figure 6-36

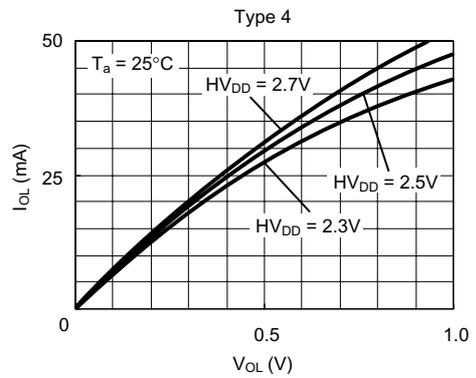


Figure 6-37

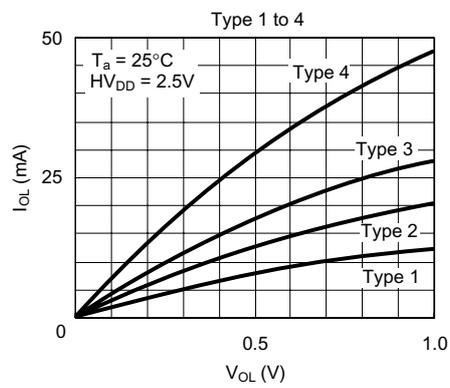


Figure 6-38

● 1.8 V ± 0.15 V

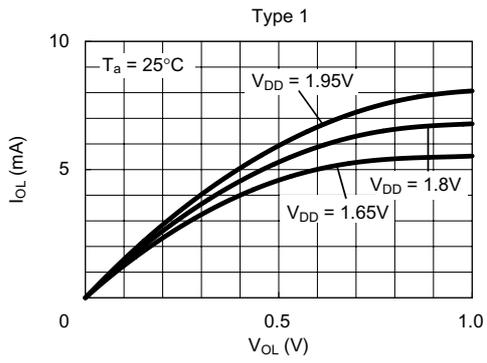


Figure 6-39

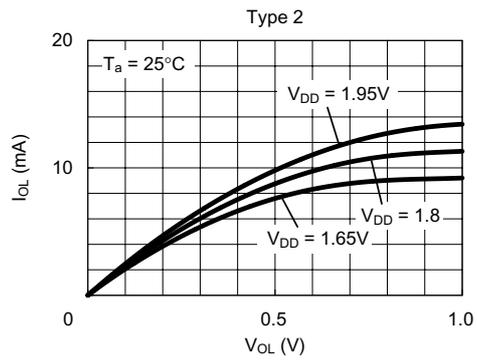


Figure 6-40

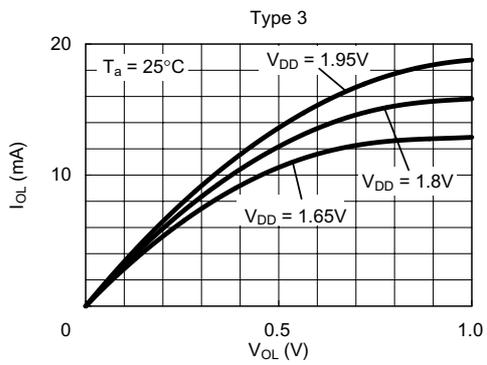


Figure 6-41

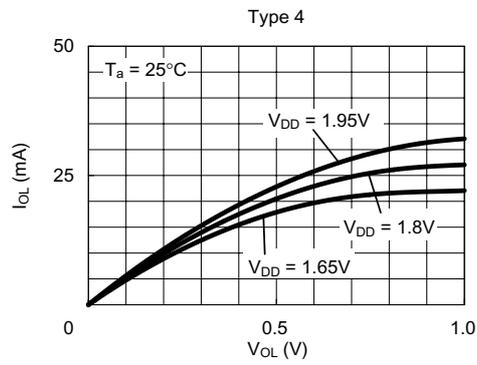


Figure 6-42

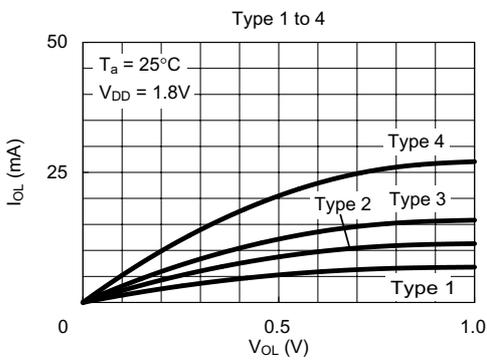


Figure 6-43

● 1.5 V ± 0.1 V

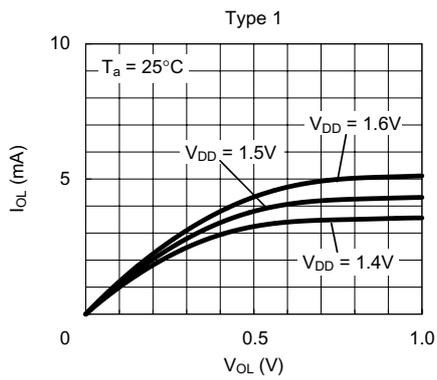


Figure 6-44

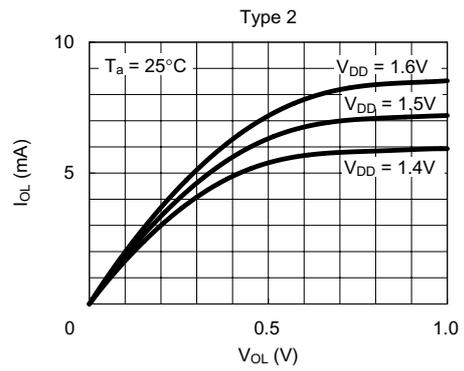


Figure 6-45

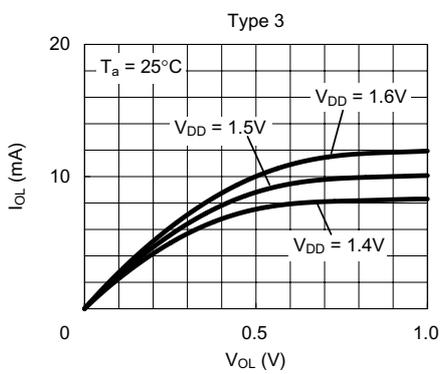


Figure 6-46

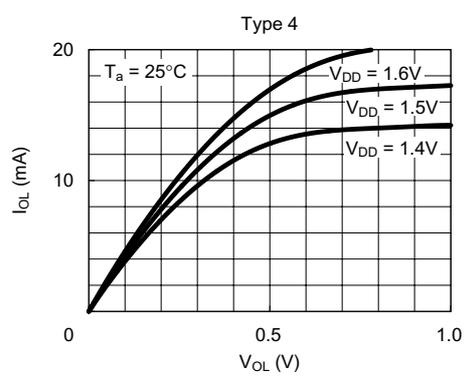


Figure 6-47

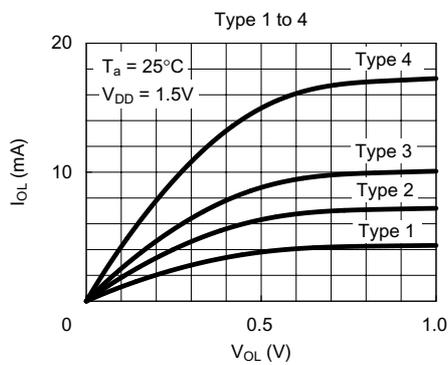


Figure 6-48

$I_{OH}-V_{OH}$

● $3.3\text{ V} \pm 0.3\text{ V}$

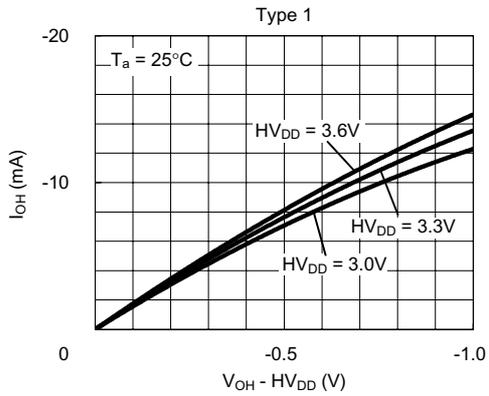


Figure 6-49

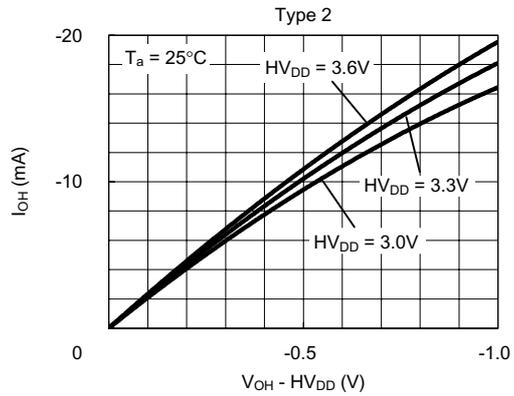


Figure 6-50

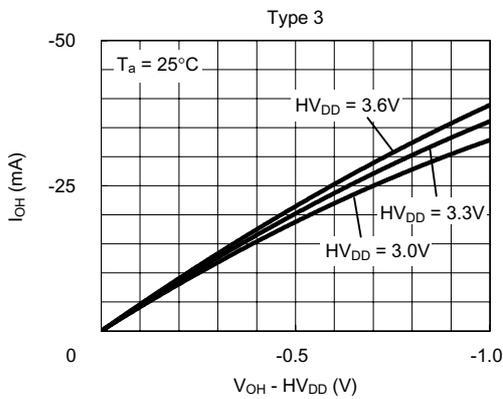


Figure 6-51

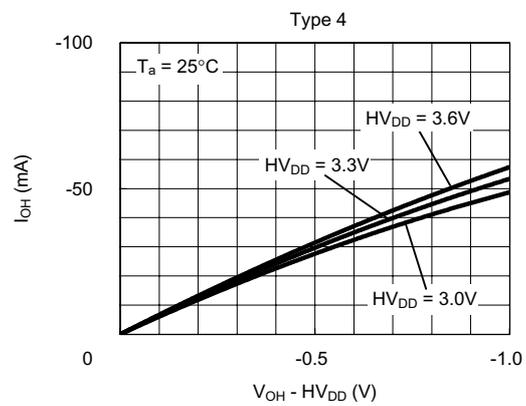


Figure 6-52

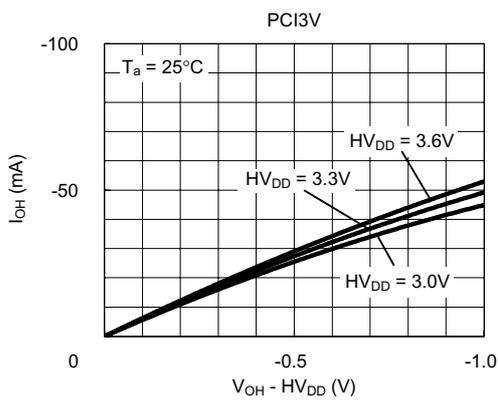


Figure 6-53

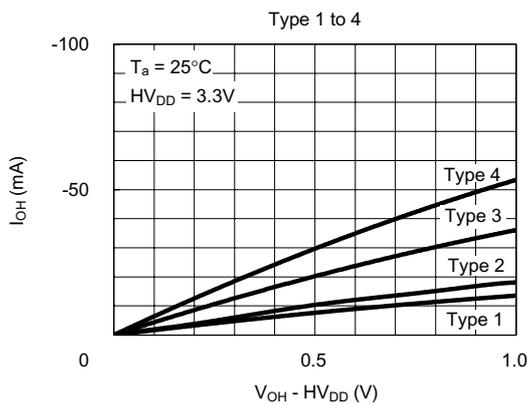


Figure 6-54

● 2.5 V ± 0.2 V

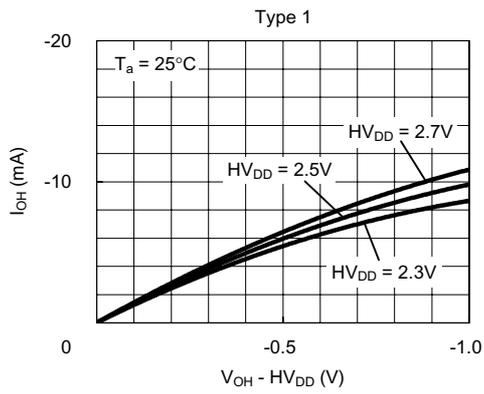


Figure 6-55

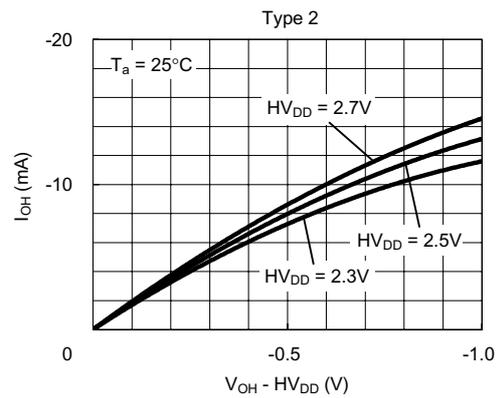


Figure 6-56

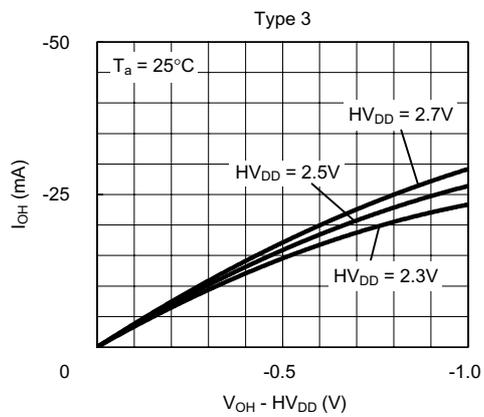


Figure 6-57

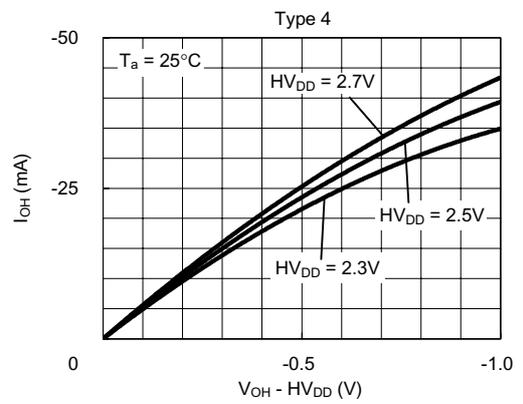


Figure 6-58

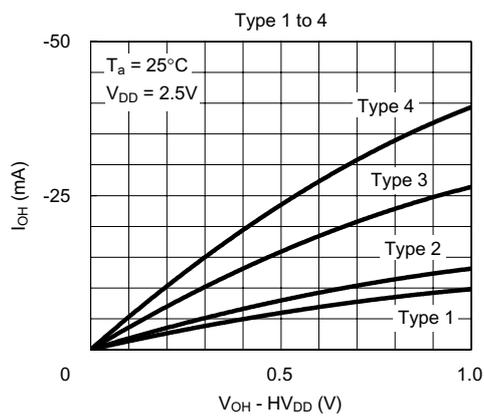


Figure 6-59

● 1.8 V ± 0.15 V

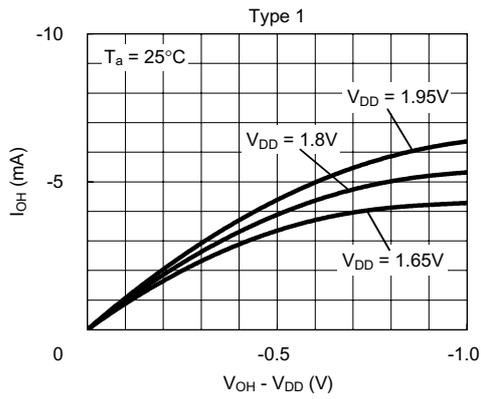


Figure 6-60

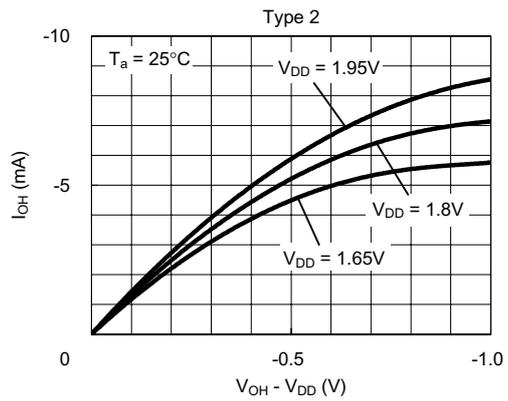


Figure 6-61

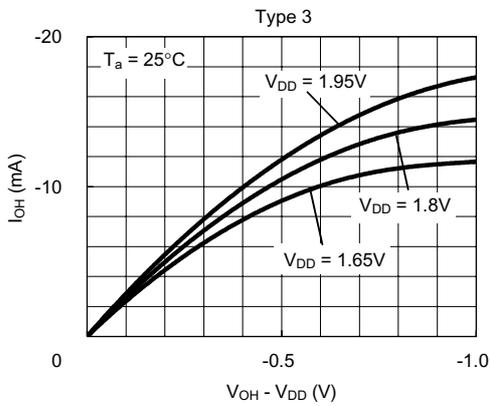


Figure 6-62

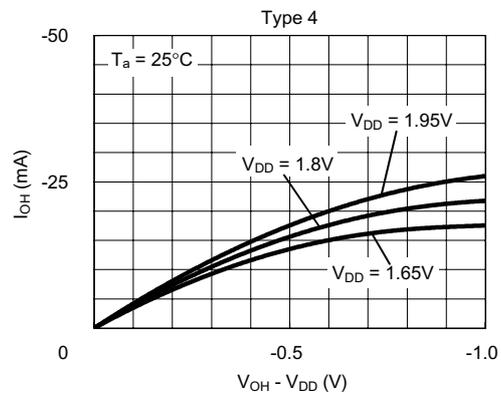


Figure 6-63

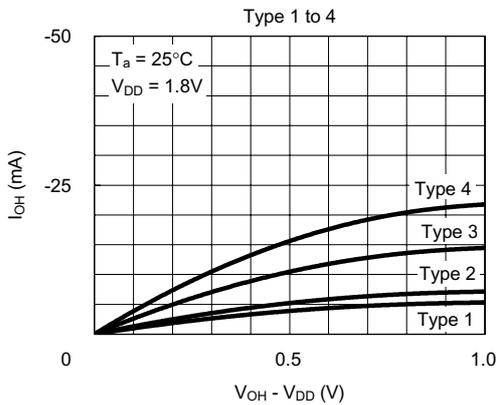


Figure 6-64

● 1.5 V ± 0.1 V

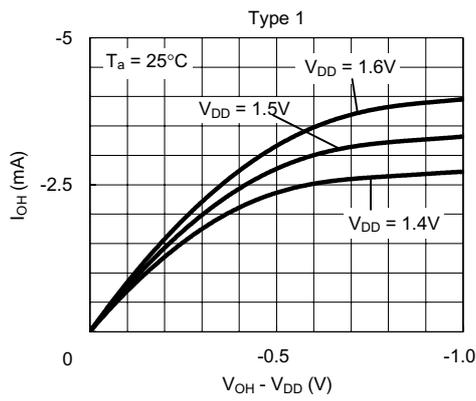


Figure 6-65

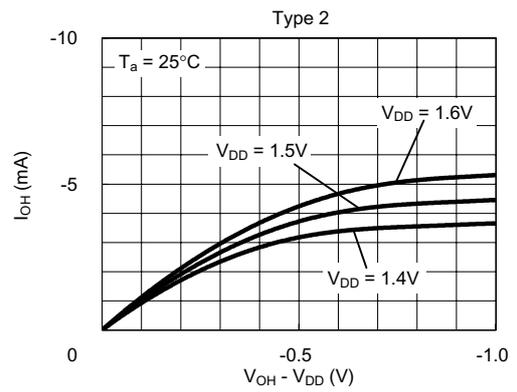


Figure 6-66

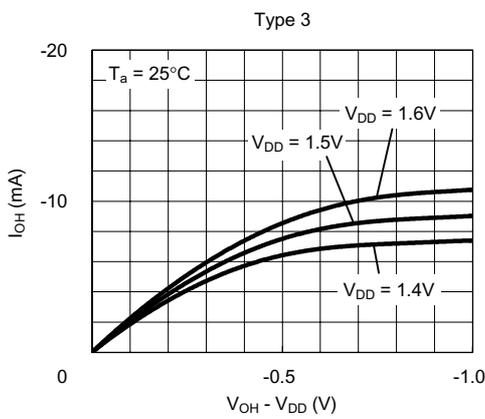


Figure 6-67

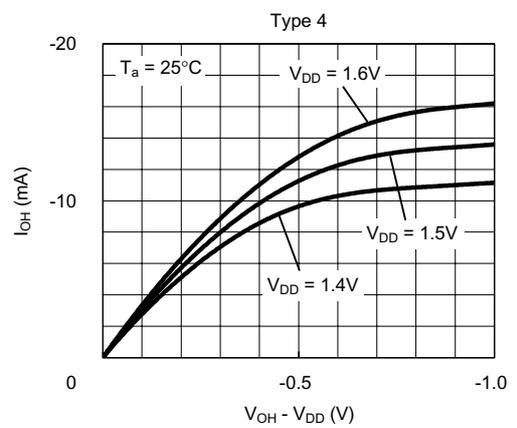


Figure 6-68

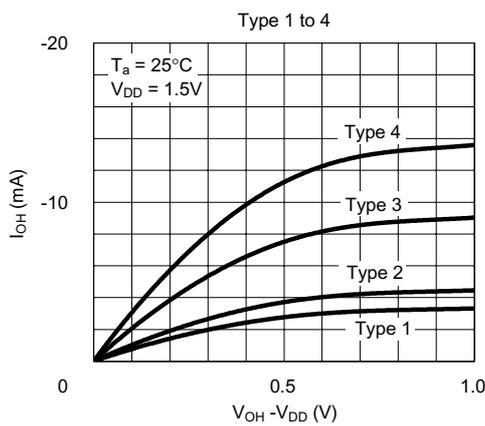


Figure 6-69

(3) I_{OH} and I_{OL} temperature characteristics

● 3.3 V ± 0.3 V

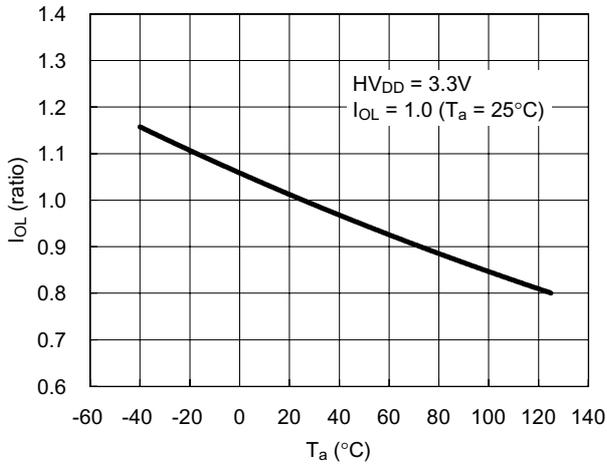


Figure 6-70 Ambient temperature (T_a) vs. Output current (I_{OL})

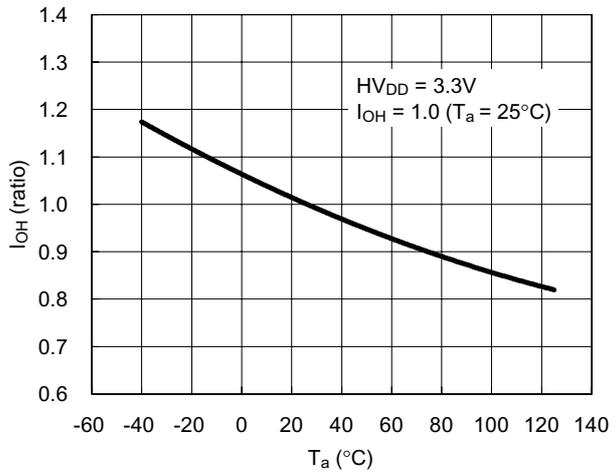


Figure 6-71 Ambient temperature (T_a) vs. Output current (I_{OH})

● 2.5 V ± 0.2 V

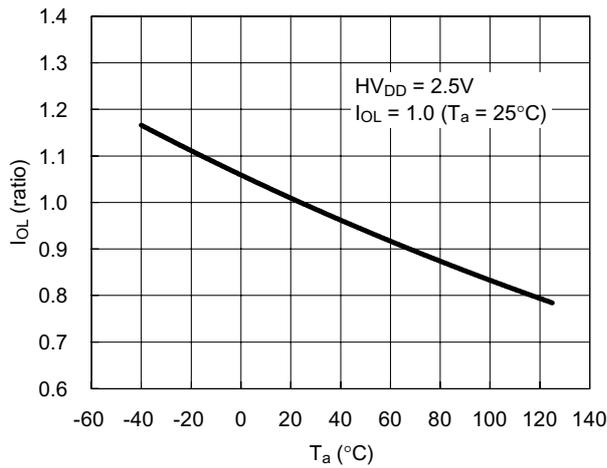


Figure 6-72 Ambient temperature (T_a) vs. Output current (I_{OL})

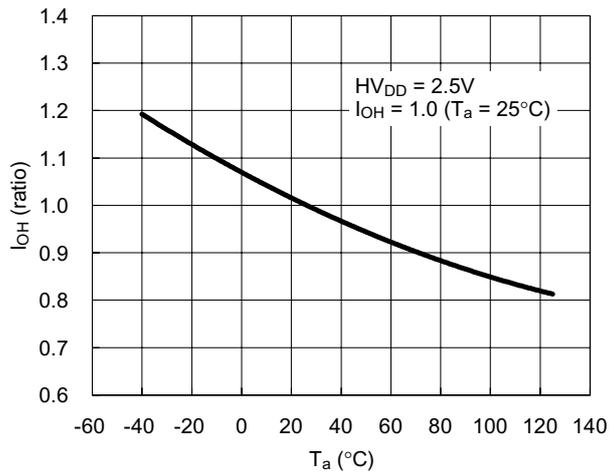


Figure 6-73 Ambient temperature (T_a) vs. Output current (I_{OH})

● 1.8 V ± 0.15 V

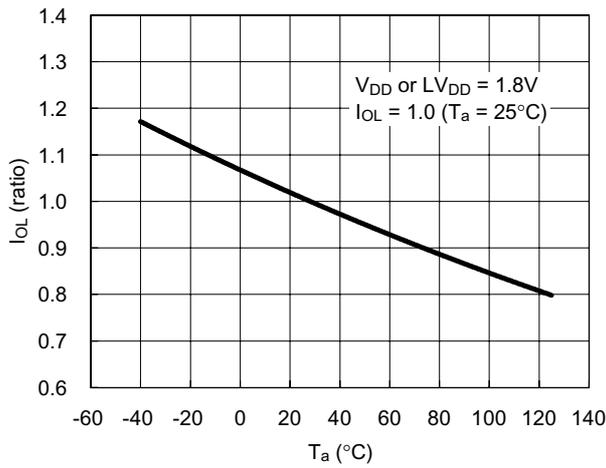


Figure 6-74 Ambient temperature (T_a) vs. Output current (I_{OL})

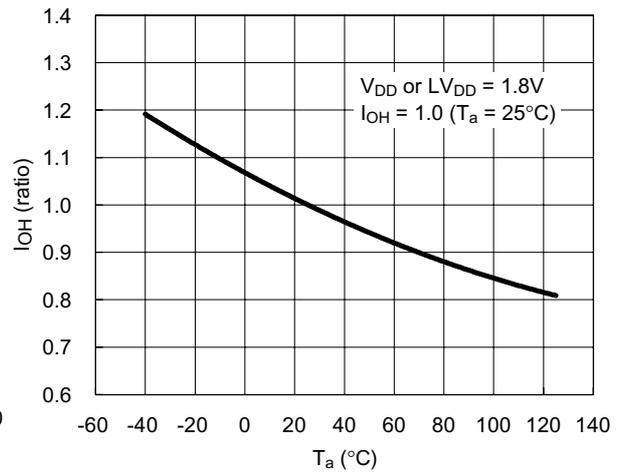


Figure 6-75 Ambient temperature (T_a) vs. Output current (I_{OH})

● 1.5 V ± 0.1 V

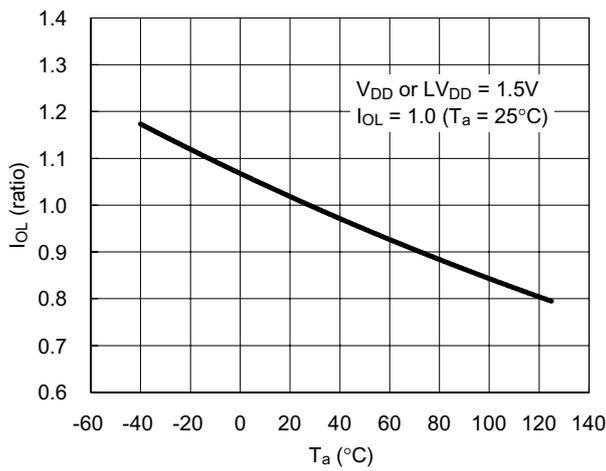


Figure 6-76 Ambient temperature (T_a) vs. Output current (I_{OL})

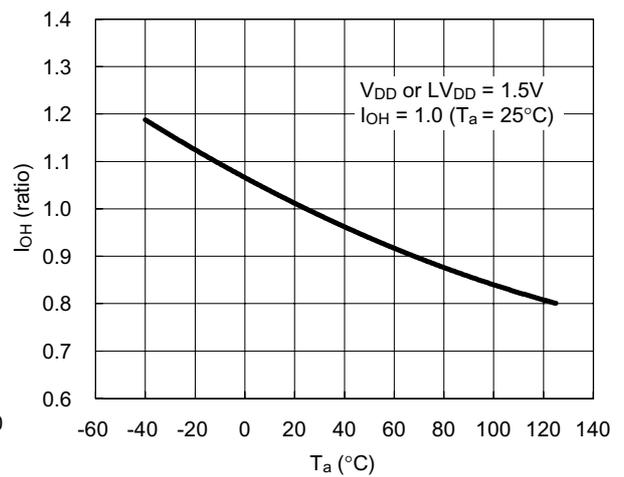


Figure 6-77 Ambient temperature (T_a) vs. Output current (I_{OH})

- (4) $t_{pHL}-C_L, t_{pLH}-C_L$
 ● 3.3 V ± 0.3 V

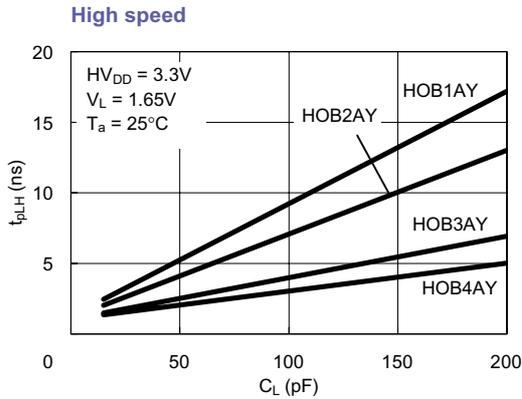


Figure 6-78 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

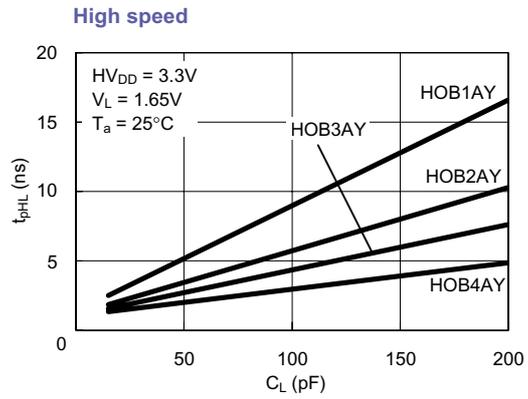


Figure 6-79 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

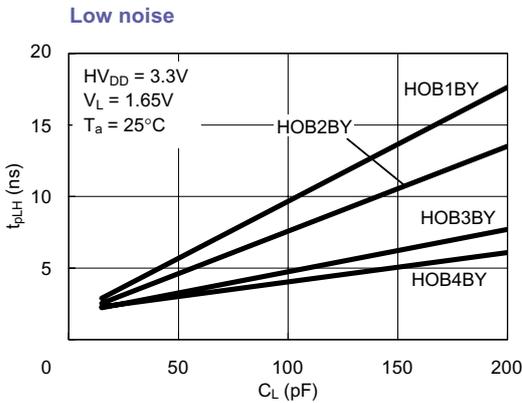


Figure 6-80 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

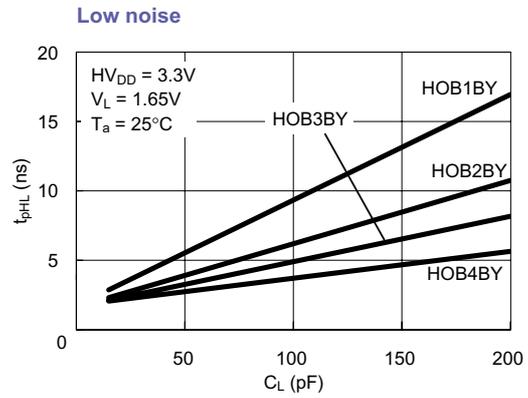


Figure 6-81 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

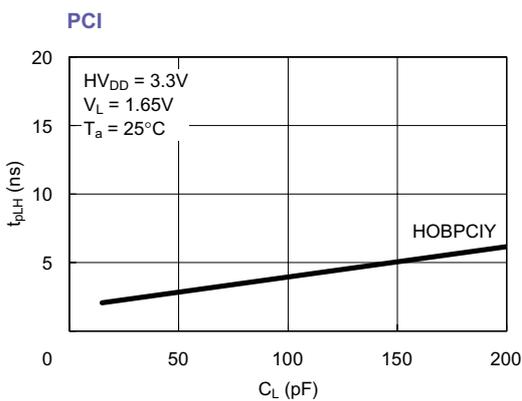


Figure 6-82 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

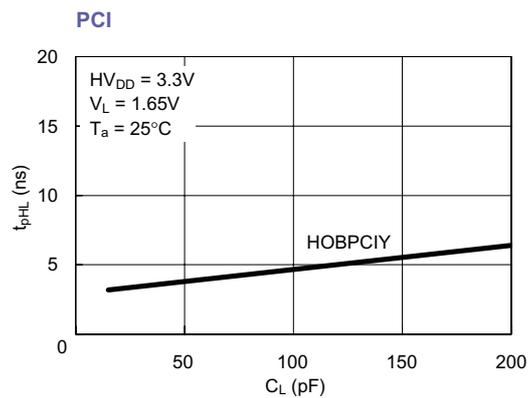


Figure 6-83 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

● 2.5 V ± 0.2 V

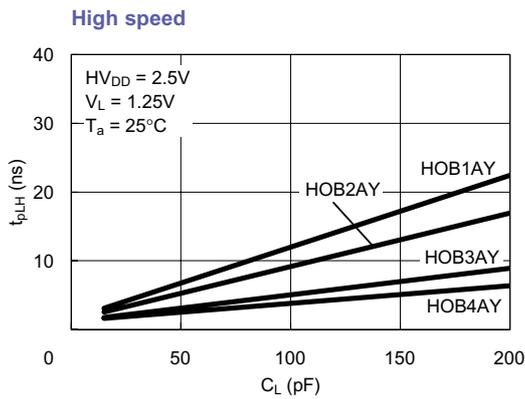


Figure 6-84 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

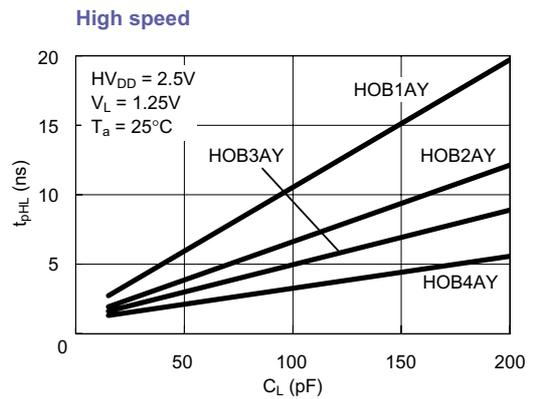


Figure 6-85 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

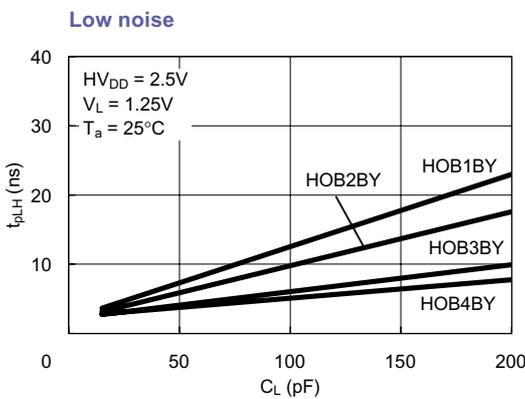


Figure 6-86 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

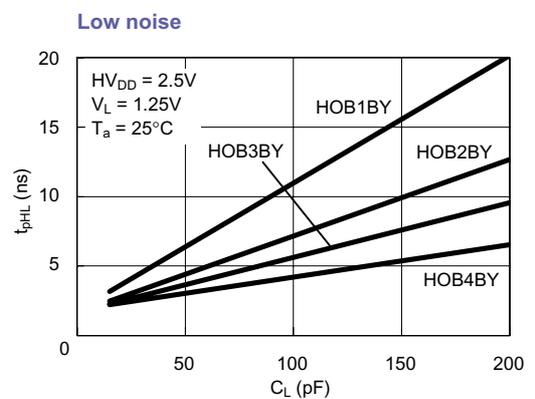


Figure 6-87 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

● 1.8 V ± 0.15 V

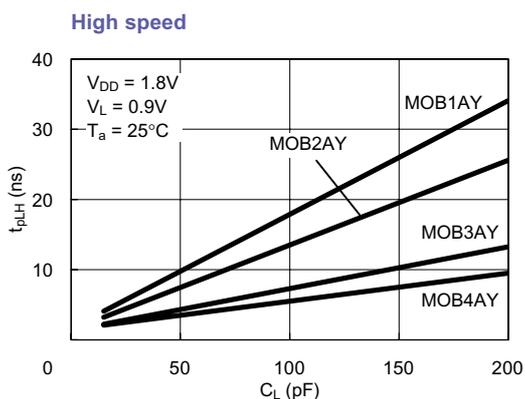


Figure 6-88 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

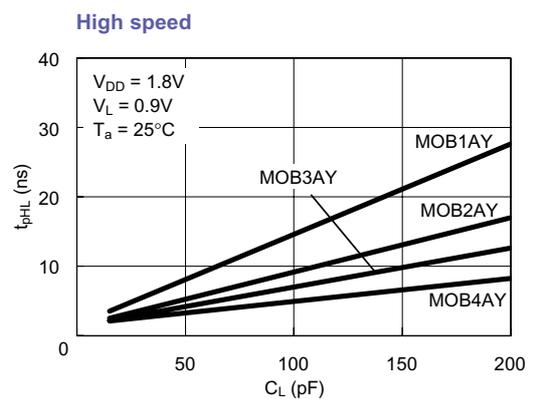


Figure 6-89 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

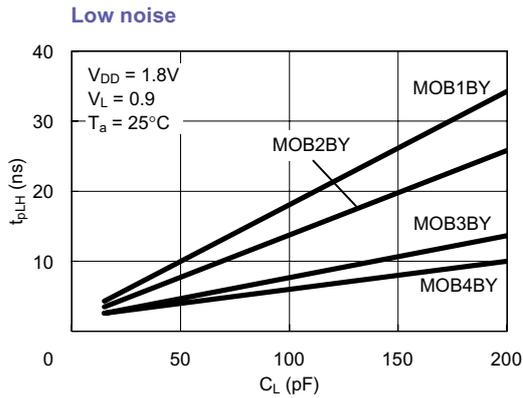


Figure 6-90 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

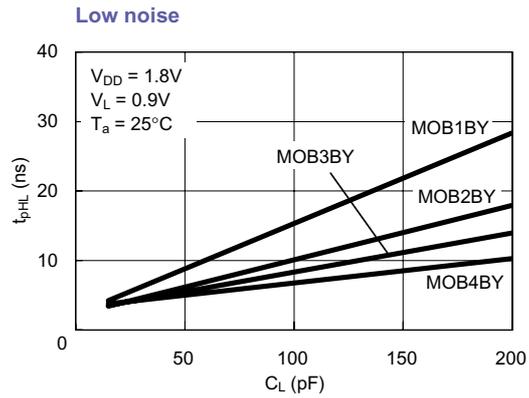


Figure 6-91 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

● $1.5V \pm 0.1V$

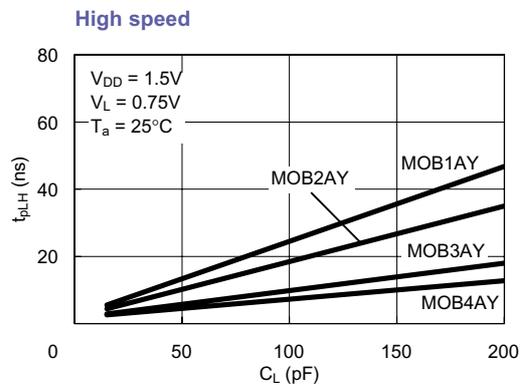


Figure 6-92 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

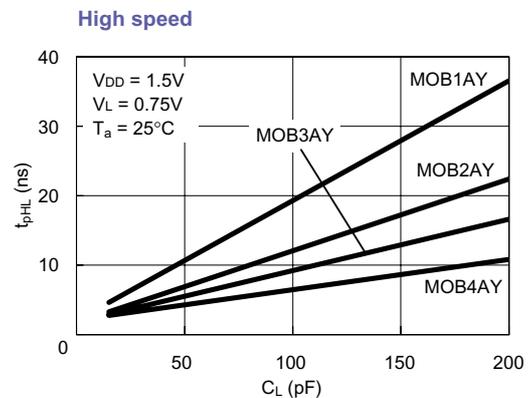


Figure 6-93 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

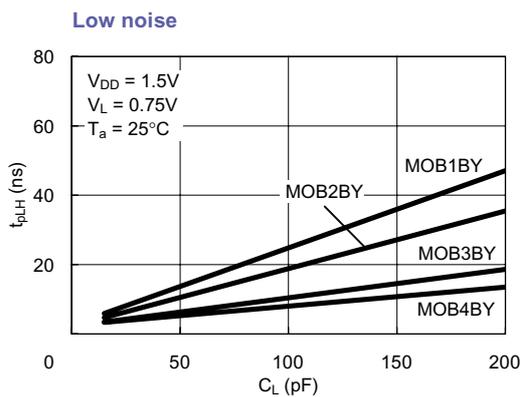


Figure 6-94 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

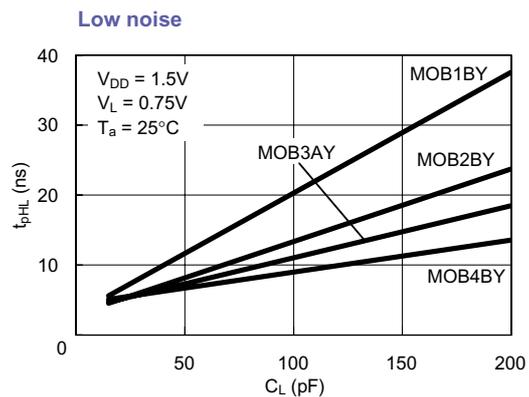


Figure 6-95 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

(5) t_r (10%-90%) - C_L , t_f (10%-90%) - C_L

● 3.3 V ± 0.3 V

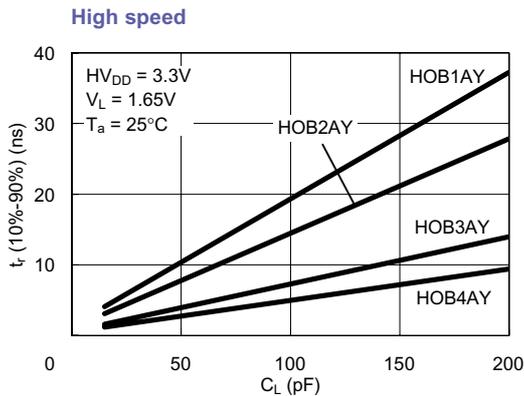


Figure 6-96 Rising Time (t_r) vs. Output load Capacitance (C_L)

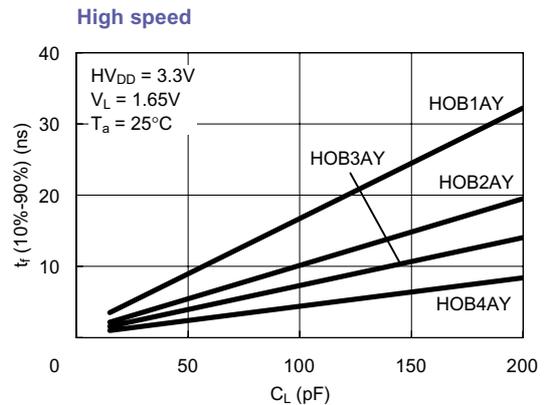


Figure 6-97 Falling Time (t_f) vs. Output load Capacitance (C_L)

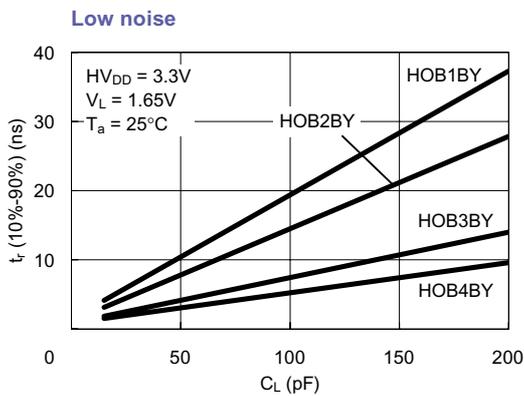


Figure 6-98 Rising Time (t_r) vs. Output load Capacitance (C_L)

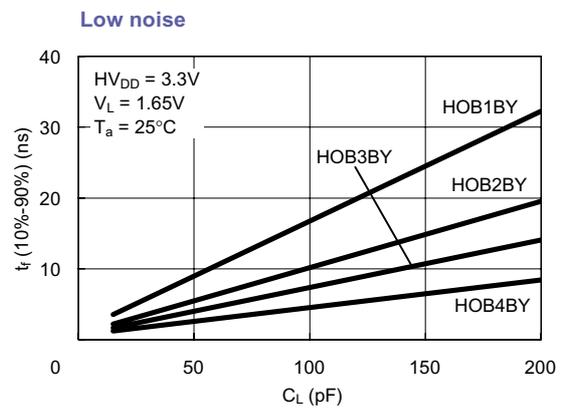


Figure 6-99 Falling Time (t_f) vs. Output load Capacitance (C_L)

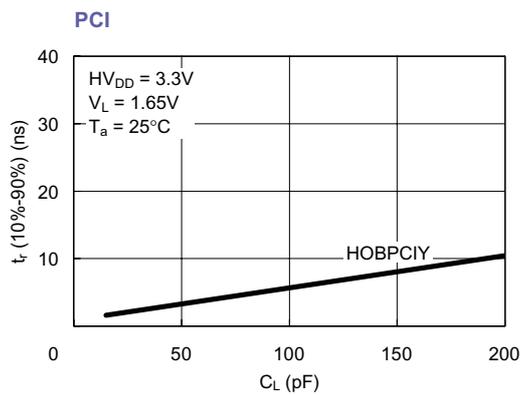


Figure 6-100 Rising Time (t_r) vs. Output load Capacitance (C_L)

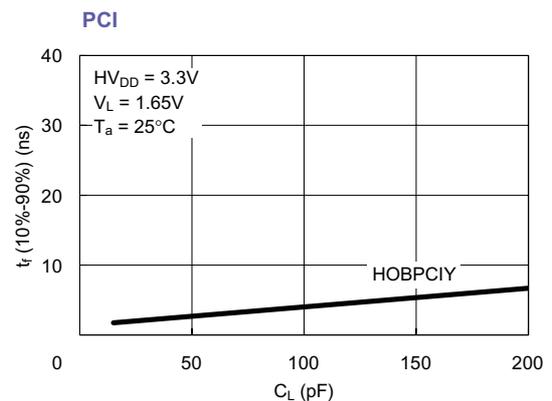


Figure 6-101 Falling Time (t_f) vs. Output load Capacitance (C_L)

● 2.5 V ± 0.2 V

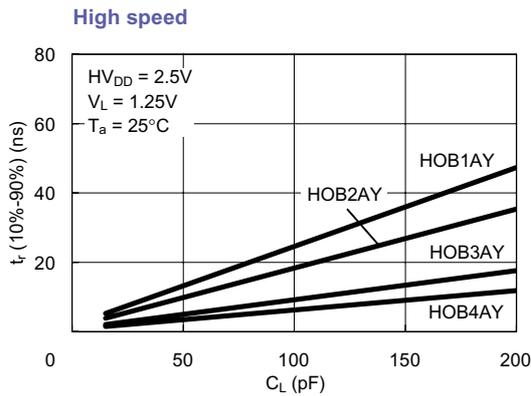


Figure 6-102 Rising Time (t_r) vs. Output load Capacitance (C_L)

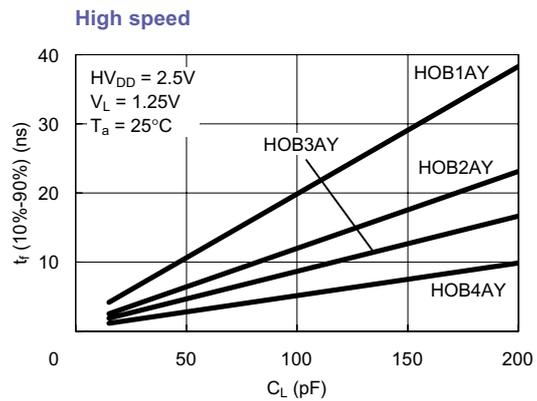


Figure 6-103 Falling Time (t_f) vs. Output load Capacitance (C_L)

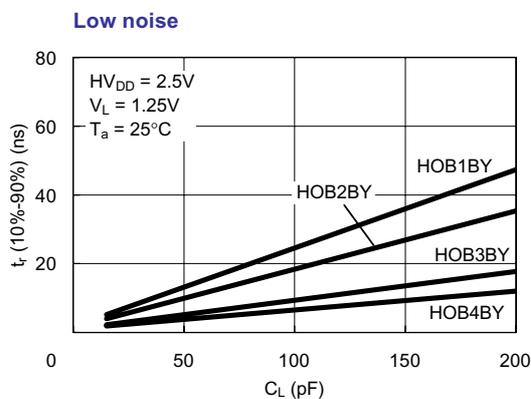


Figure 6-104 Rising Time (t_r) vs. Output load Capacitance (C_L)

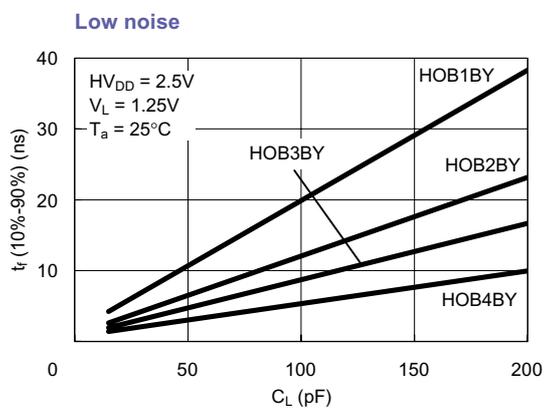


Figure 6-105 Falling Time (t_f) vs. Output load Capacitance (C_L)

● 1.8 V ± 0.15 V

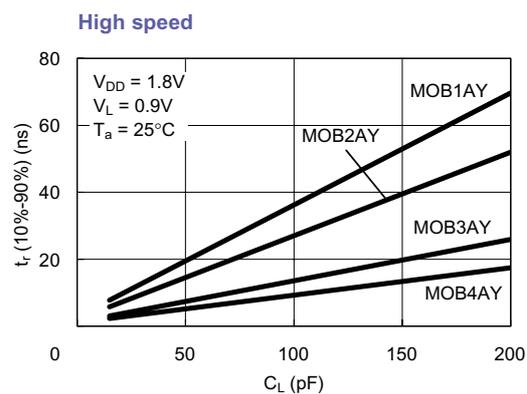


Figure 6-106 Rising Time (t_r) vs. Output load Capacitance (C_L)

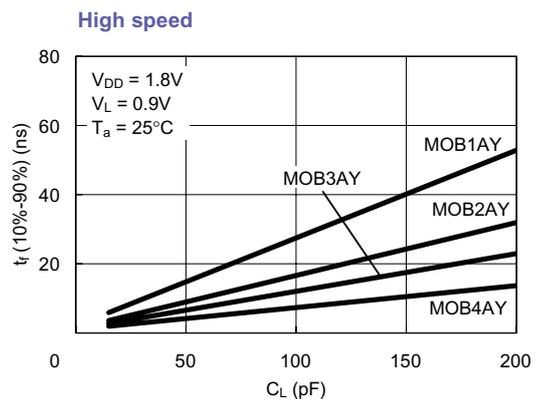


Figure 6-107 Falling Time (t_f) vs. Output load Capacitance (C_L)

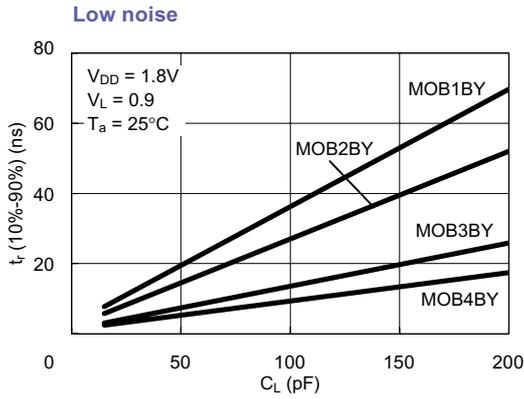


Figure 6-108 Rising Time (t_r) vs. Output load Capacitance (C_L)

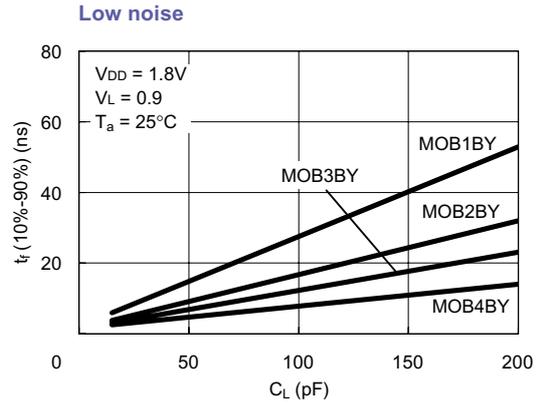


Figure 6-109 Falling Time (t_r) vs. Output load Capacitance (C_L)

● 1.5 V ± 0.1 V

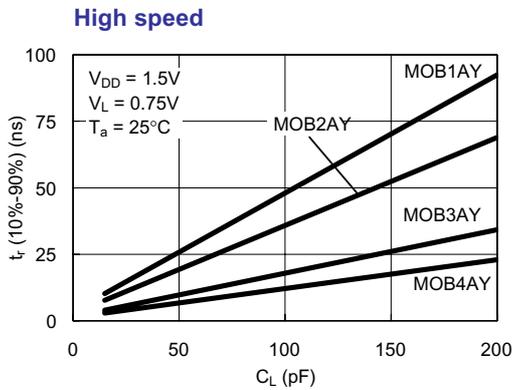


Figure 6-110 Rising Time (t_r) vs. Output load Capacitance (C_L)

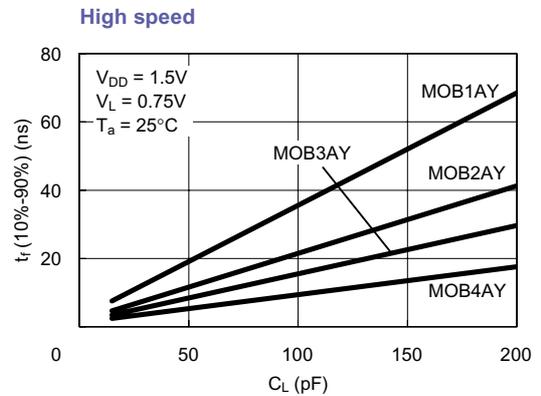


Figure 6-111 Falling Time (t_r) vs. Output load Capacitance (C_L)

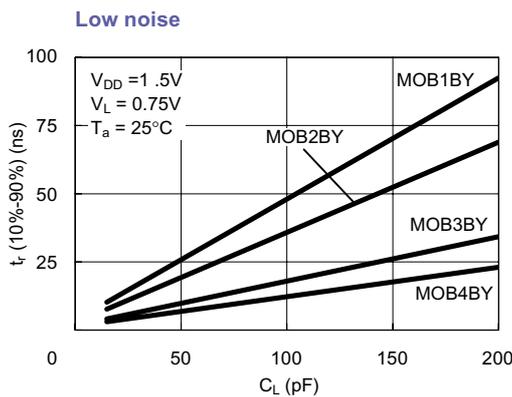


Figure 6-112 Rising Time (t_r) vs. Output load Capacitance (C_L)

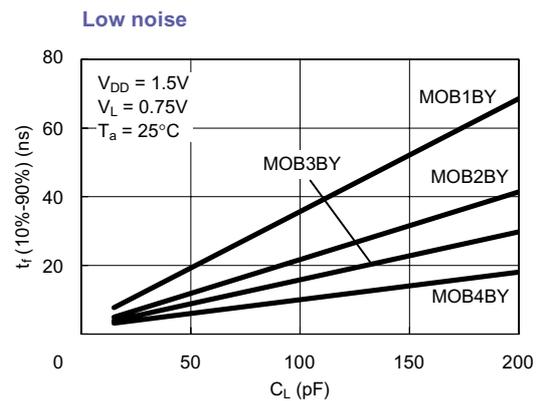


Figure 6-113 Falling Time (t_r) vs. Output load Capacitance (C_L)

(6) Recommended range of load capacitances for output buffers

Table 6-11 lists the recommended range of load capacitances for output buffers, classified by drive capability (consult Table 6-11 to select the most suitable output buffer for your design). Note that if output buffers are used with a load capacitance below the recommended range of load capacitances, the output signal may have larger overshoots or undershoots.

Table 6-11 Recommended Range of Output Buffer Load Capacitances

Type of Output Buffer	Example	Recommended Range of Load Capacitances (pF)
Type 1	MOB1ATY	0–40
Type 2	MOB2ATY	20–100
Type 3	MOB3ATY	50–150
Type 4	MOB4ATY	100–200

(7) $f_{max}-C_L$

● 3.3 V ± 0.3 V

HIGH SPEED

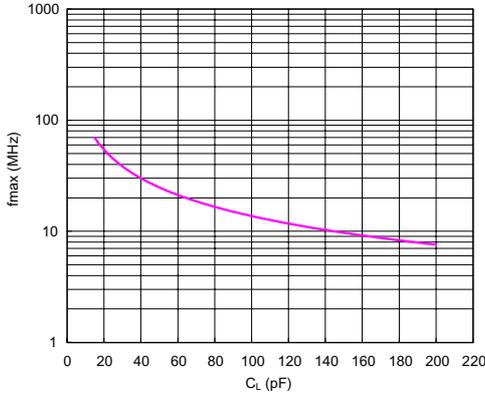


Figure 6-114 Output Operating Frequency “HOB1AY”

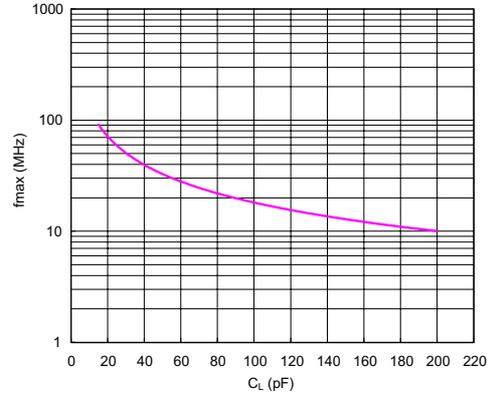


Figure 6-115 Output Operating Frequency “HOB2AY”

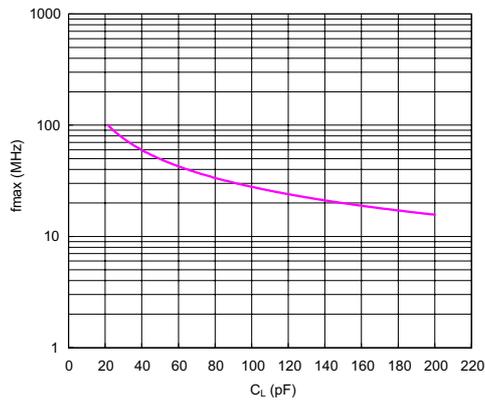


Figure 6-116 Output Operating Frequency “HOB3AY”

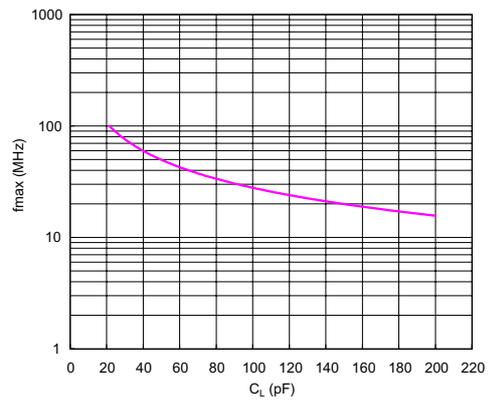


Figure 6-117 Output Operating Frequency “HOB4AY”

LOW NOISE

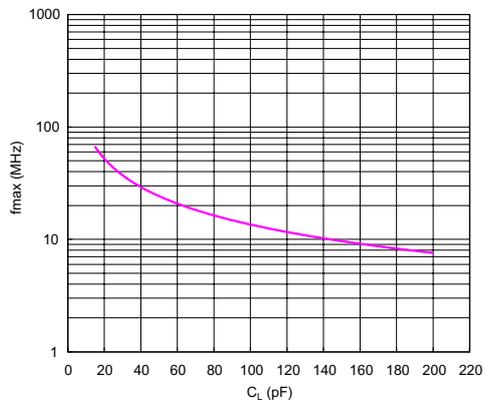


Figure 6-118 Output Operating Frequency “HOB1BY”

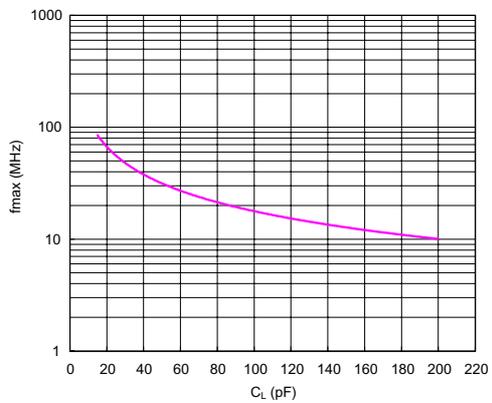


Figure 6-119 Output Operating Frequency “HOB2BY”

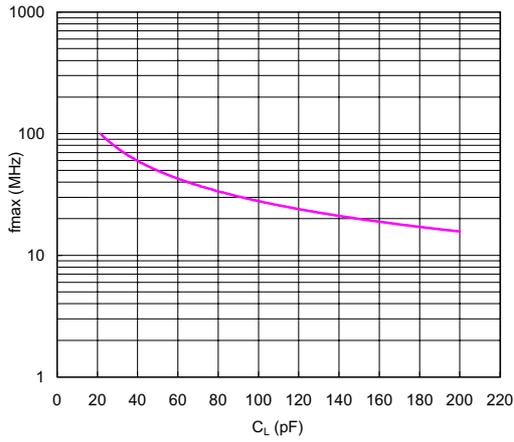


Figure 6-120 Output Operating Frequency
“HOB3BY”

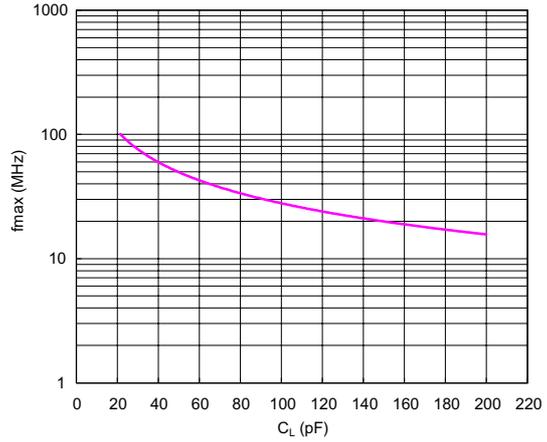


Figure 6-121 Output Operating Frequency
“HOB4BY”

● 2.5 V ± 0.2 V

HIGH SPEED

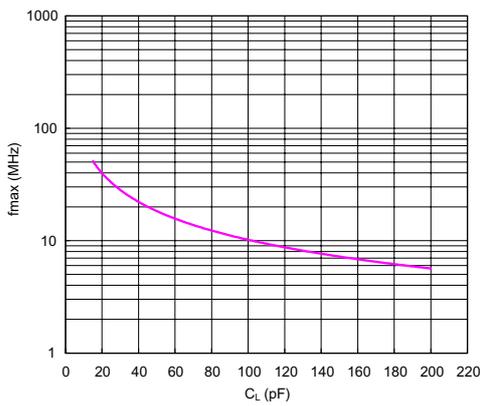


Figure 6-122 Output Operating Frequency
“HOB1AY”

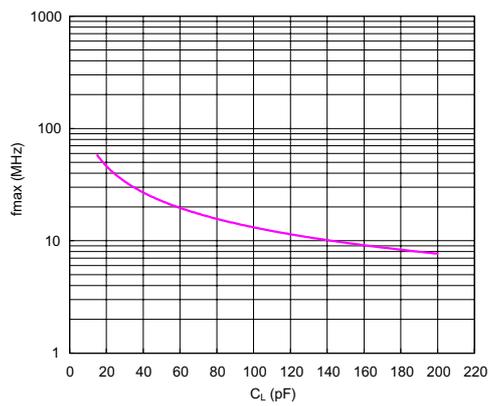


Figure 6-123 Output Operating Frequency
“HOB2AY”

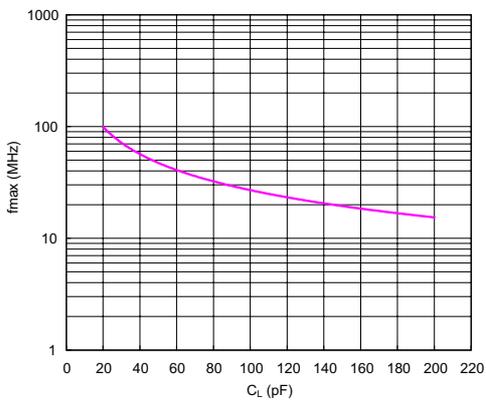


Figure 6-124 Output Operating Frequency
“HOB3AY”

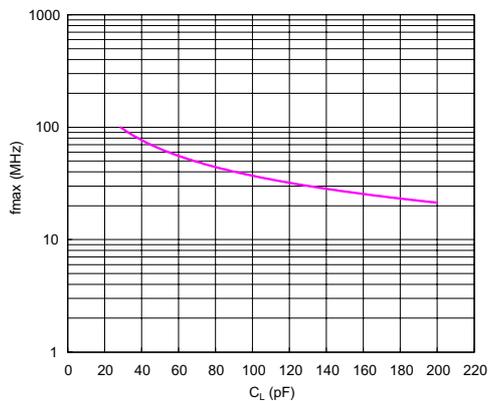


Figure 6-125 Output Operating Frequency
“HOB4AY”

LOW NOISE

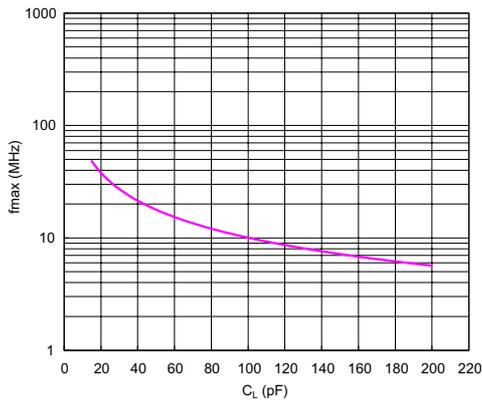


Figure 6-126 Output Operating Frequency “HOB1BY”

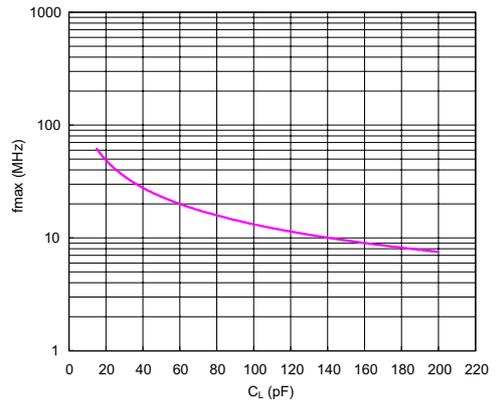


Figure 6-127 Output Operating Frequency “HOB2BY”

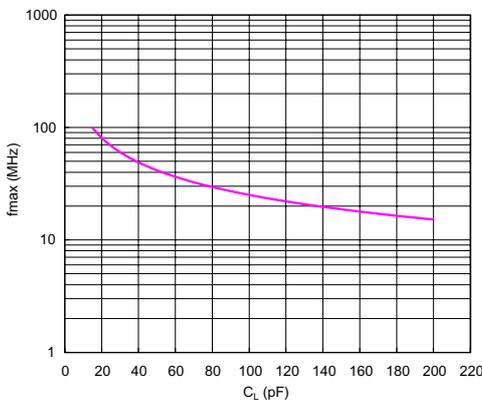


Figure 6-128 Output Operating Frequency “HOB3BY”

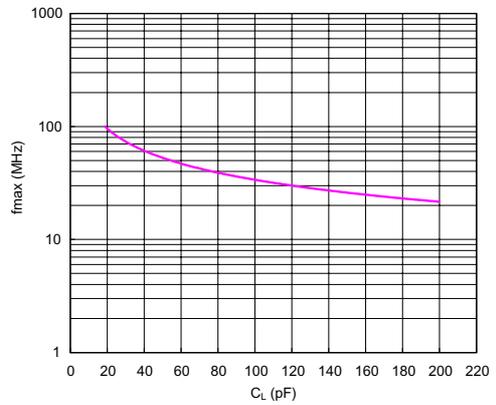


Figure 6-129 Output Operating Frequency “HOB4BY”

● 1.8 V ± 0.15 V

HIGH SPEED

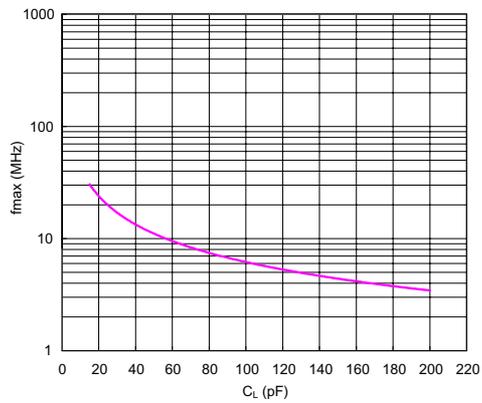


Figure 6-130 Output Operating Frequency “MOB1AY”

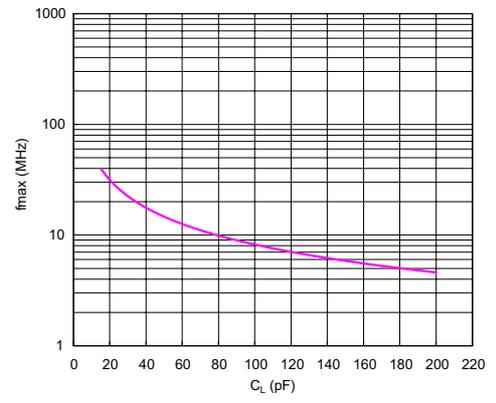


Figure 6-131 Output Operating Frequency “MOB2AY”

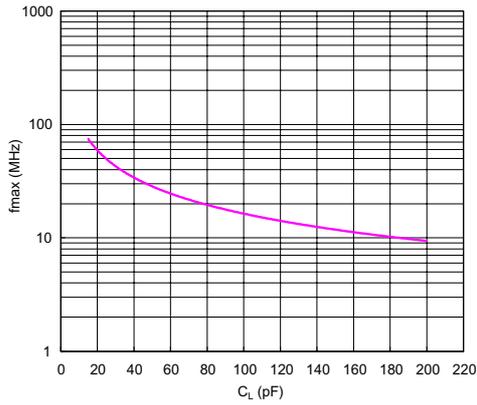


Figure 6-132 Output Operating Frequency “MOB3AY”

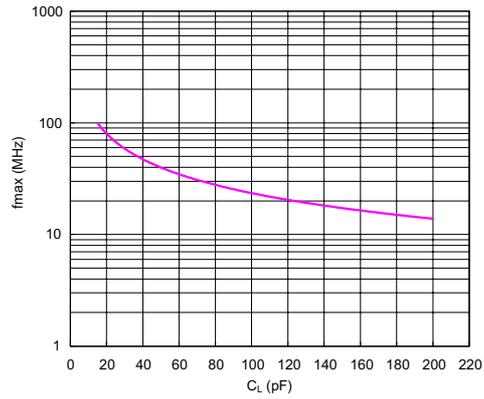


Figure 6-133 Output Operating Frequency “MOB4AY”

LOW NOISE

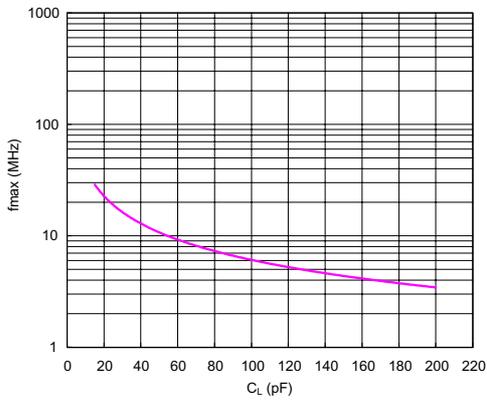


Figure 6-134 Output Operating Frequency “MOB1BY”

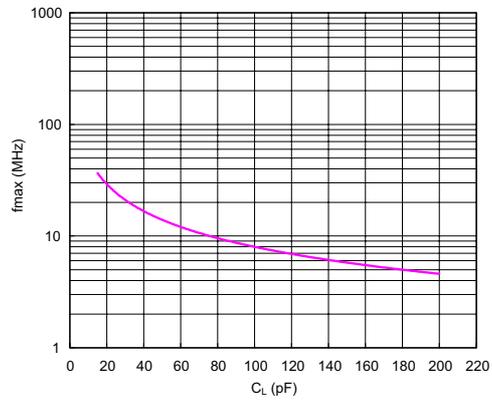


Figure 6-135 Output Operating Frequency “MOB2BY”

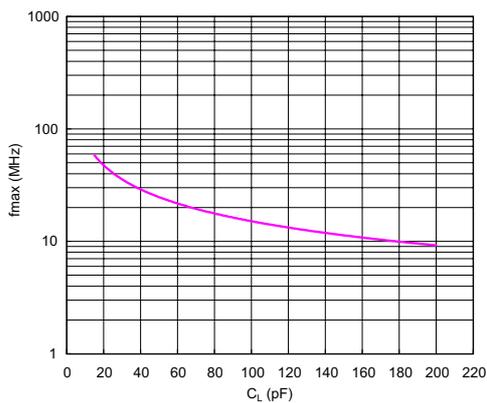


Figure 6-136 Output Operating Frequency “MOB3BY”

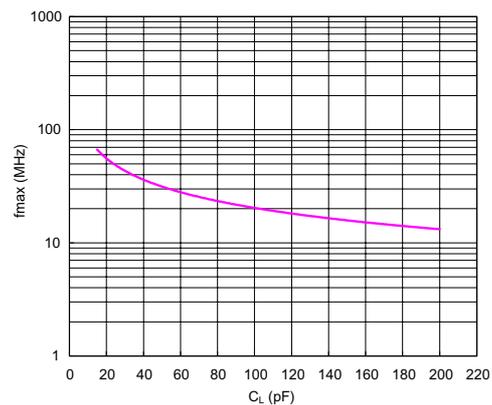


Figure 6-137 Output Operating Frequency “MOB4BY”

● 1.5 V ± 0.1 V

HIGH SPEED

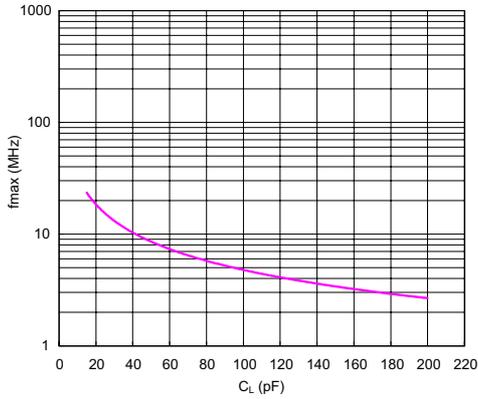


Figure 6-138 Output Operating Frequency “MOB1AY”

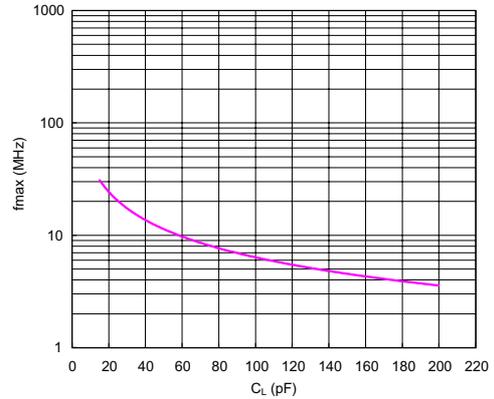


Figure 6-139 Output Operating Frequency “MOB2AY”

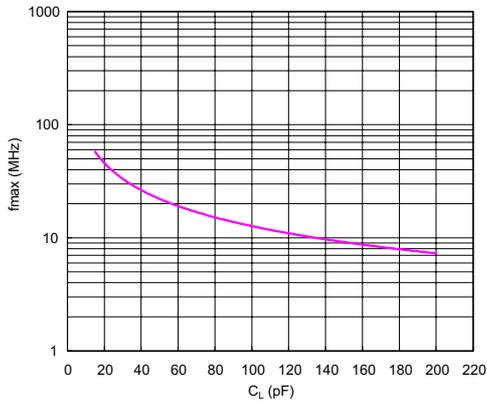


Figure 6-140 Output Operating Frequency “MOB3AY”

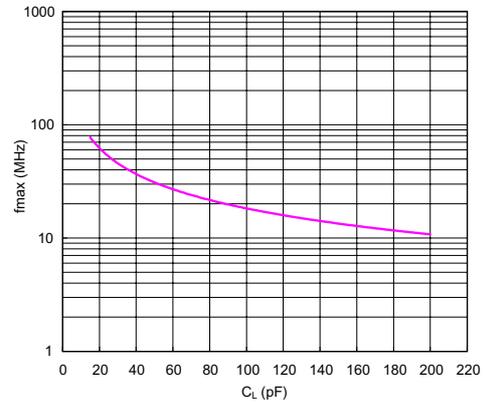


Figure 6-141 Output Operating Frequency “MOB4AY”

LOW NOISE

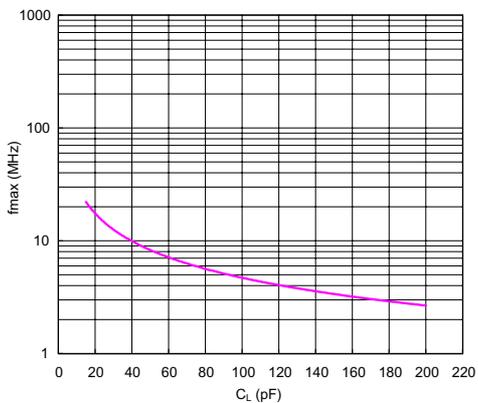


Figure 6-142 Output Operating Frequency “MOB1BY”

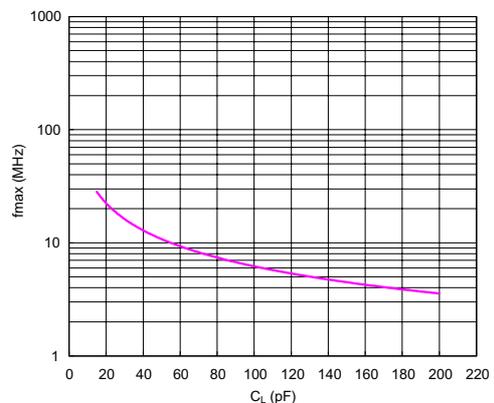


Figure 6-143 Output Operating Frequency “MOB2BY”

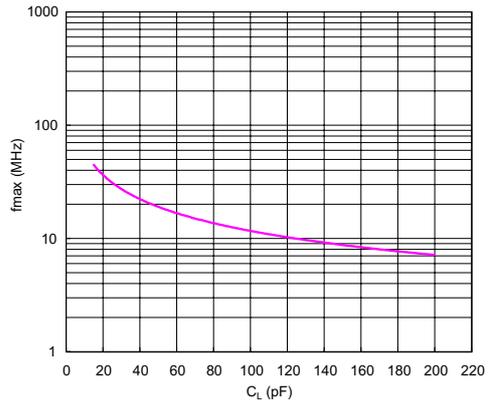


Figure 6-144 Output Operating Frequency
“MOB3BY”

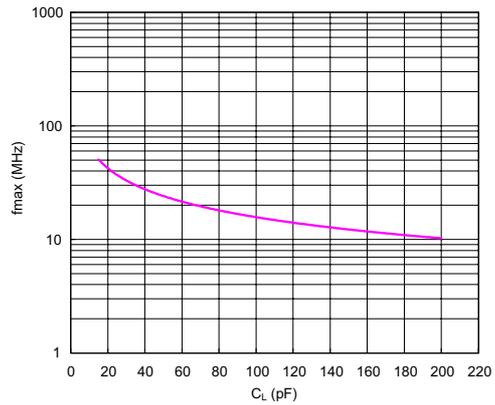


Figure 6-145 Output Operating Frequency
“MOB4BY”

(8) Pull-up/pull-down characteristics

- 3.3 V ± 0.3 V

Pull-up Characteristics

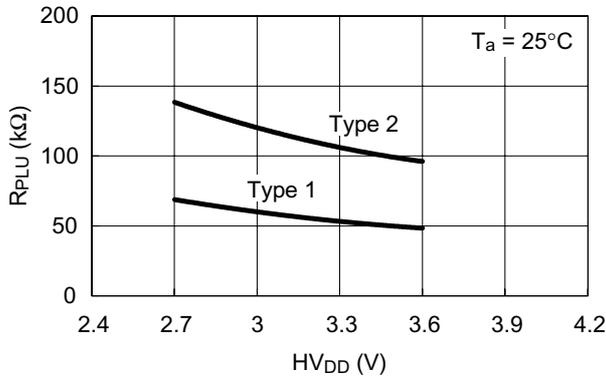


Figure 6-146 Pull-up Resistance (R_{PLU}) vs. HV_{DD}

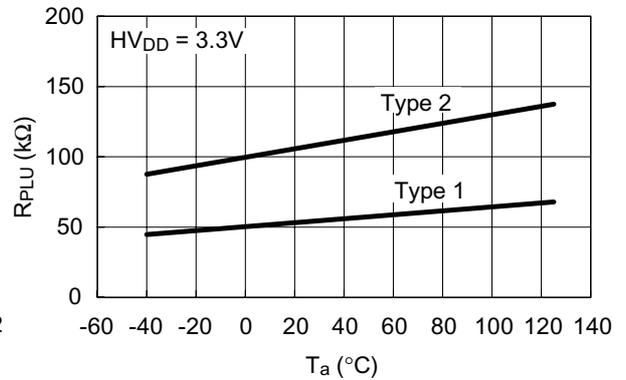


Figure 6-147 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

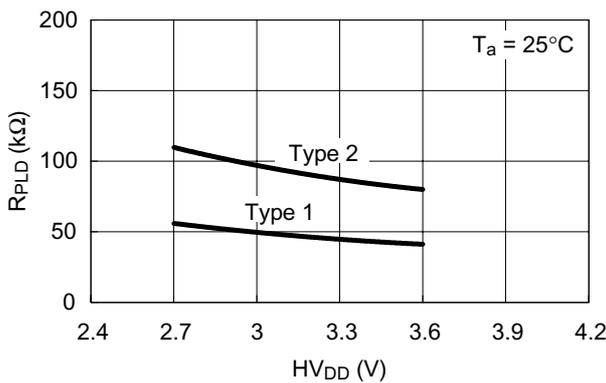


Figure 6-148 Pull-down Resistance (R_{PLD}) vs. HV_{DD}

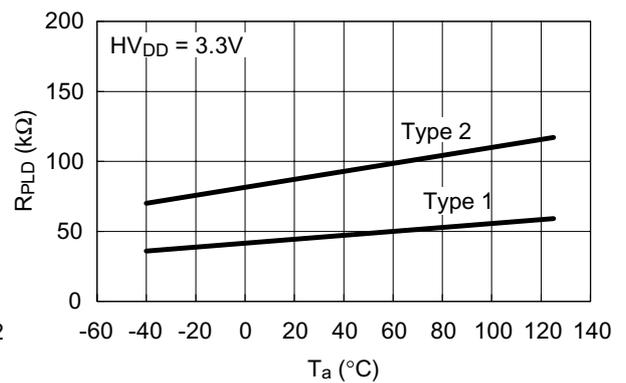


Figure 6-149 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

● 2.5 V ± 0.2 V

Pull-up Characteristics

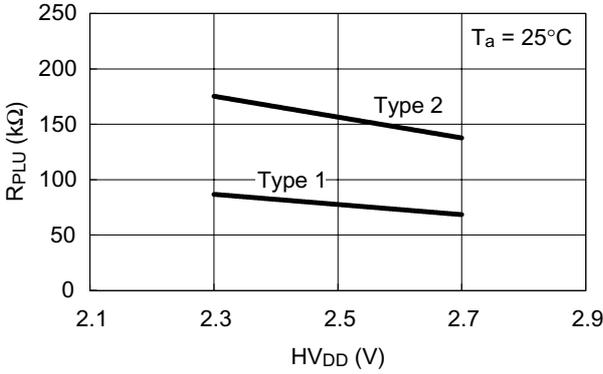


Figure 6-150 Pull-up Resistance (R_{PLU}) vs. HV_{DD}

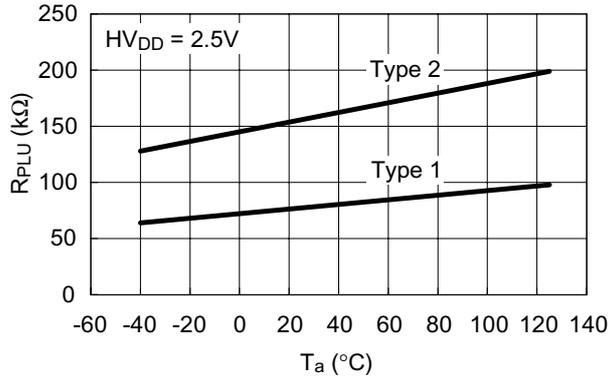


Figure 6-151 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

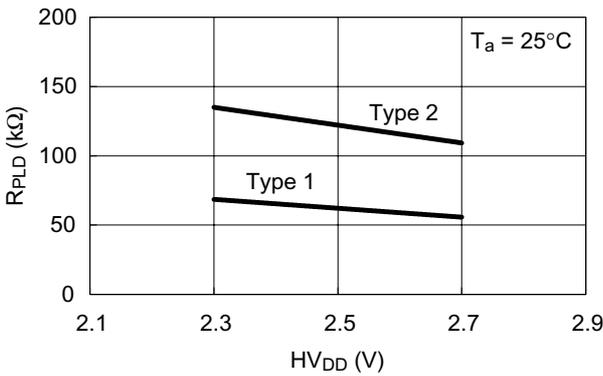


Figure 6-152 Pull-down Resistance (R_{PLD}) vs. HV_{DD}

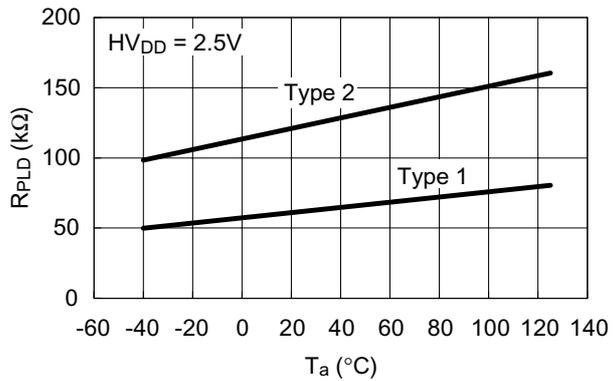


Figure 6-153 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

● 1.8 V ± 0.15 V

Pull-up Characteristics

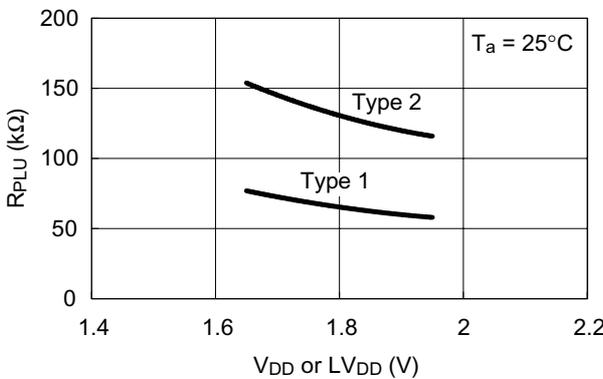


Figure 6-154 Pull-up Resistance (R_{PLU}) vs. V_{DD} (LV_{DD})

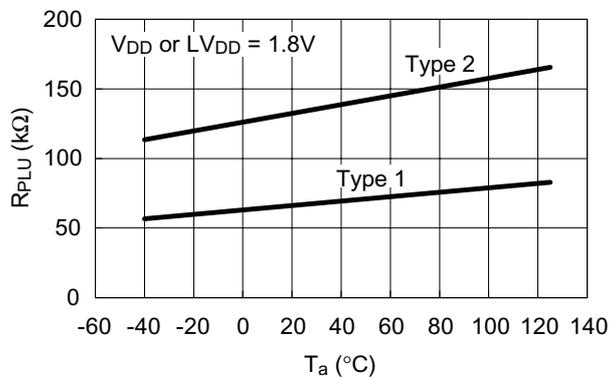


Figure 6-155 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

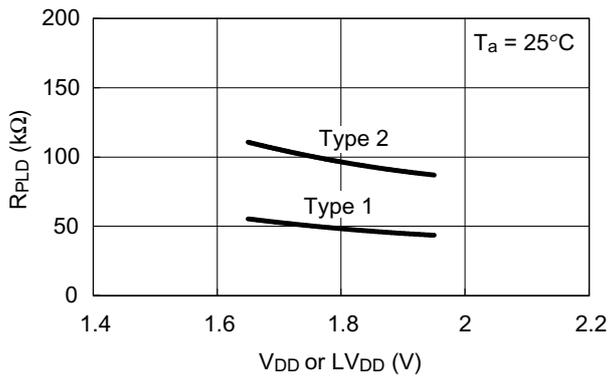


Figure 6-156 Pull-down Resistance (R_{PLD}) vs. V_{DD} (LV_{DD})

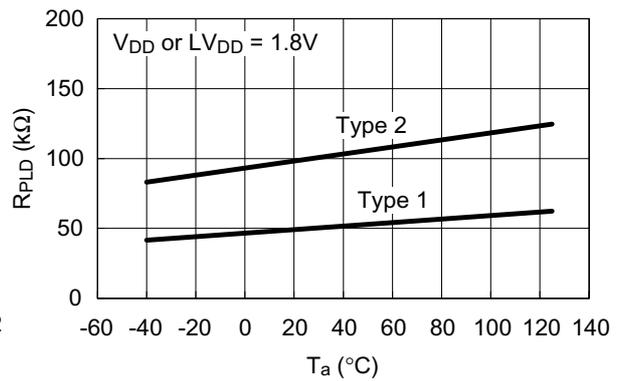


Figure 6-157 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

● 1.5 V ± 0.1 V

Pull-up Characteristics

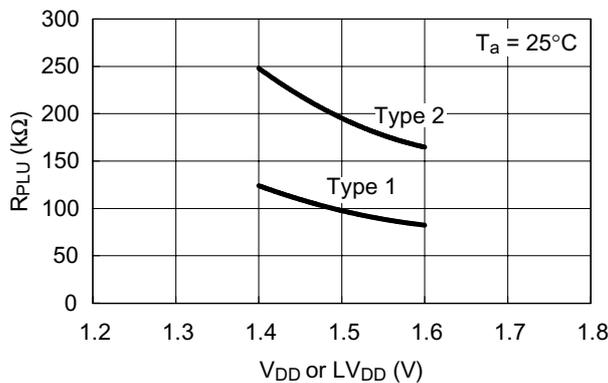


Figure 6-158 Pull-up Resistance (R_{PLU}) vs. V_{DD} (LV_{DD})

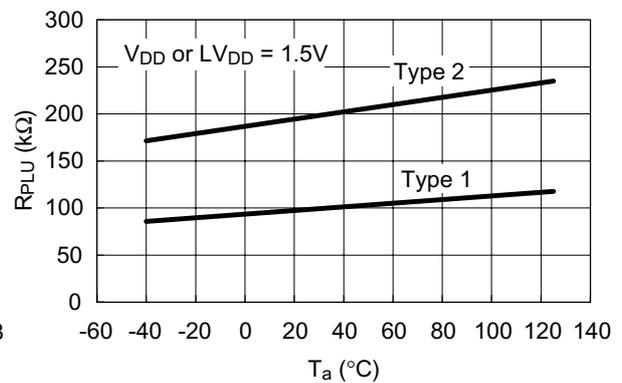


Figure 6-159 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

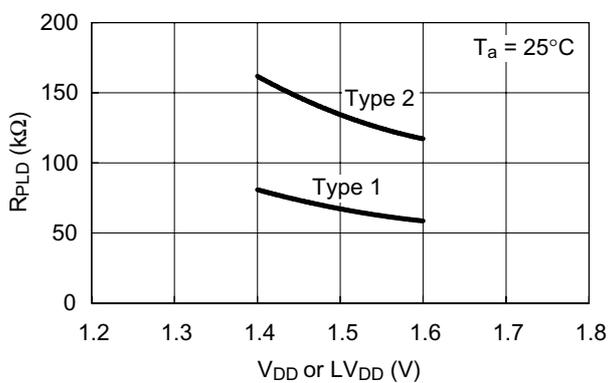


Figure 6-160 Pull-down Resistance (R_{PLD}) vs. V_{DD} (LV_{DD})

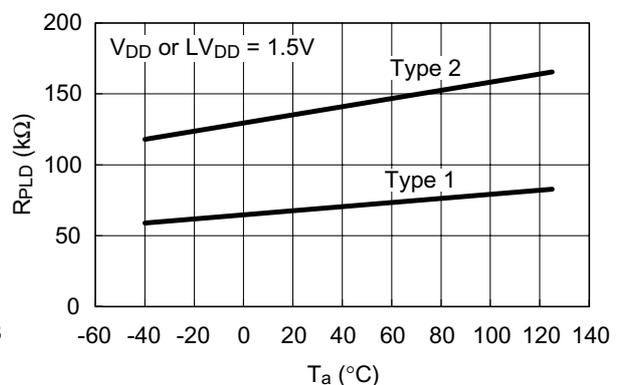


Figure 6-161 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(9) Output waveforms

- 3.3 V ± 0.3 V

Type 1

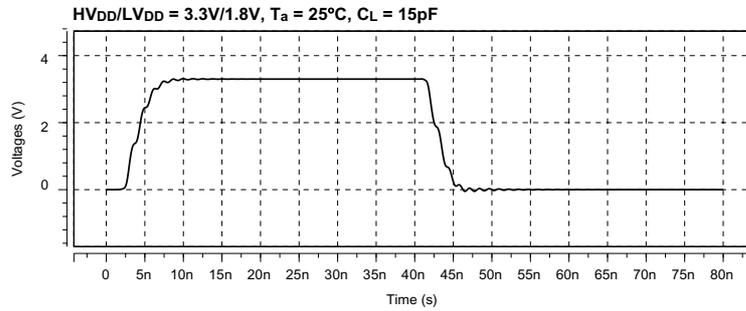


Figure 6-162 Output Waveform (HOB1AY)

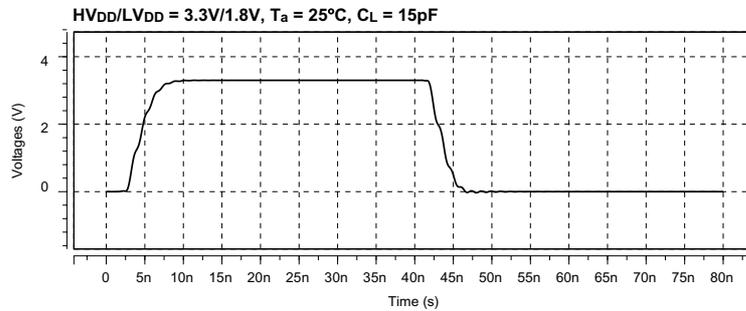


Figure 6-163 Output Waveform (HOB1BY)

Type 2

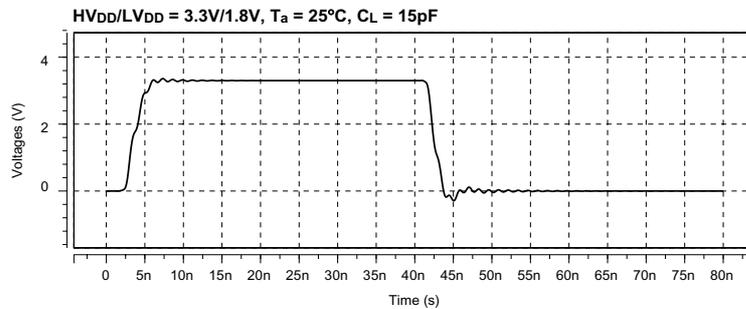


Figure 6-164 Output Waveform (HOB2AY)

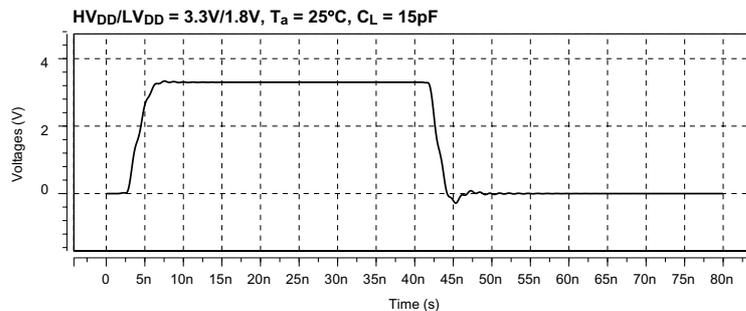


Figure 6-165 Output Waveform (HOB2BY)

Type 3

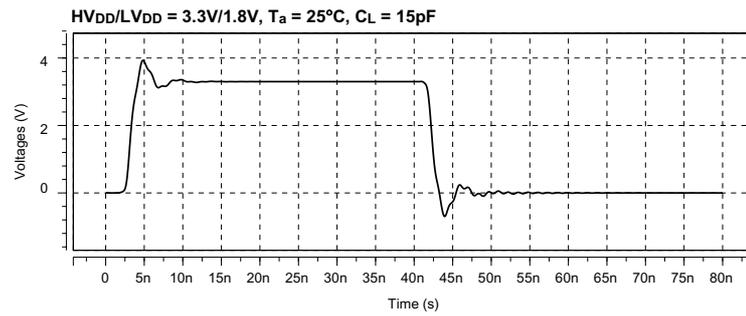


Figure 6-166 Output Waveform (HOB3AY)

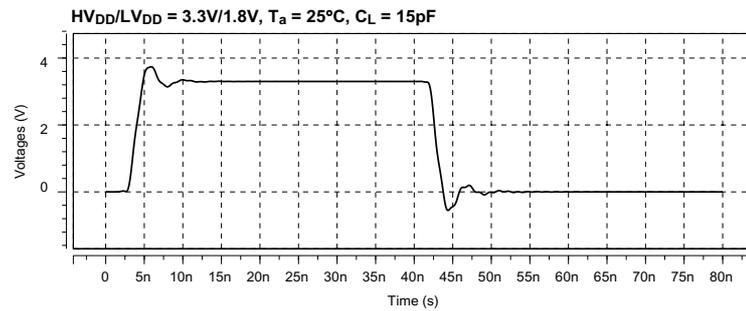


Figure 6-167 Output Waveform (HOB3BY)

Type 4

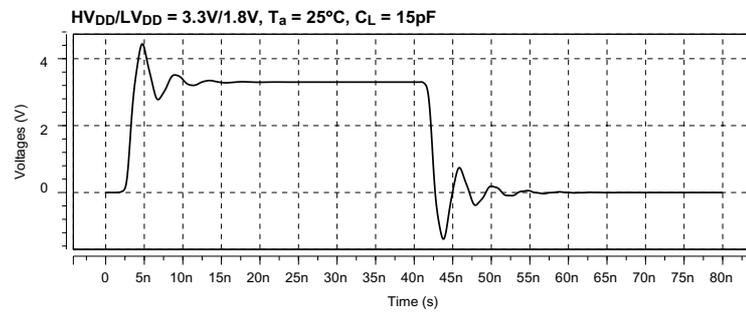


Figure 6-168 Output Waveform (HOB4AY)

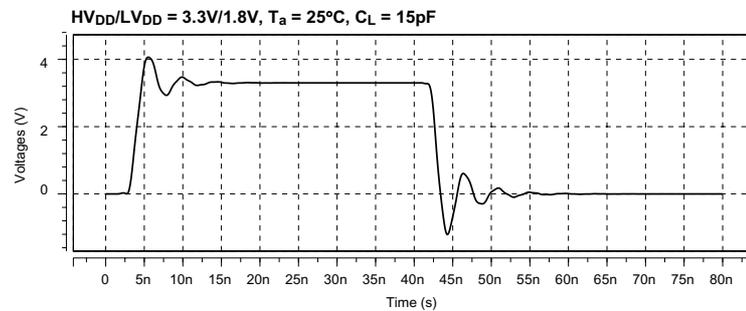


Figure 6-169 Output Waveform (HOB4BY)

- 2.5 V ± 0.2 V

Type 1

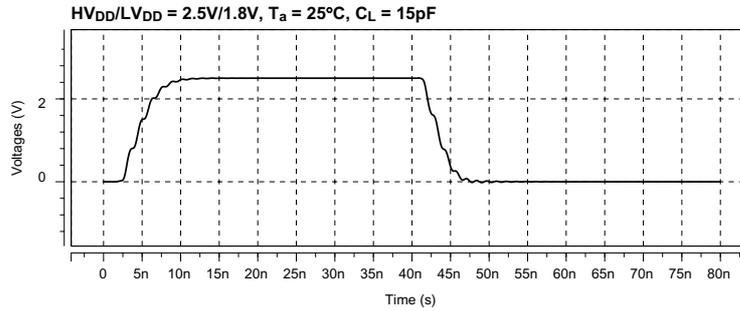


Figure 6-170 Output Waveform (HOB1AY)

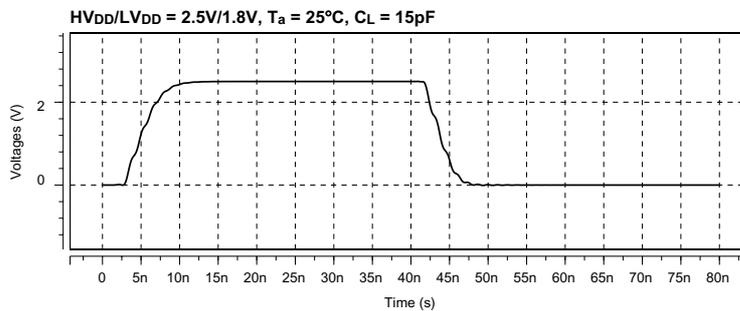


Figure 6-171 Output Waveform (HOB1BY)

Type 2

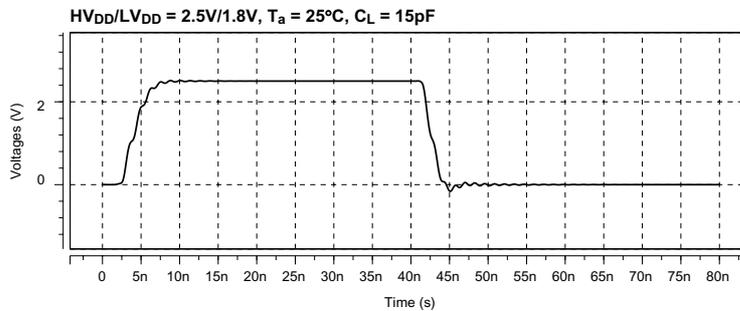


Figure 6-172 Output Waveform (HOB2AY)

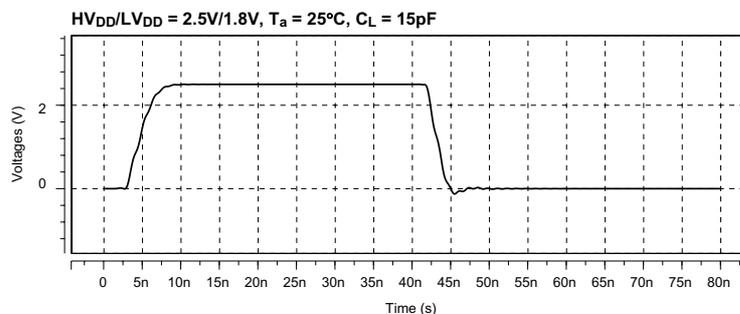


Figure 6-173 Output Waveform (HOB2BY)

Type 3

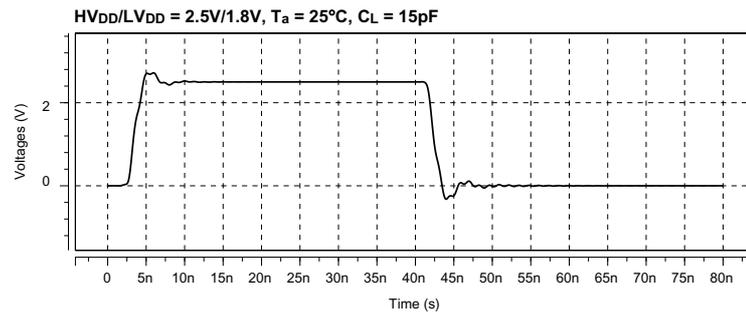


Figure 6-174 Output Waveform (HOB3AY)

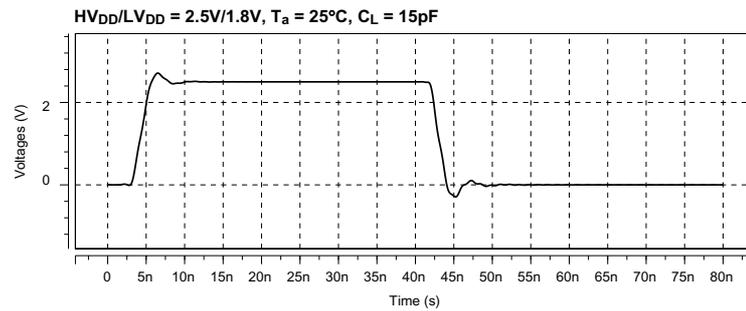


Figure 6-175 Output Waveform (HOB3BY)

Type 4

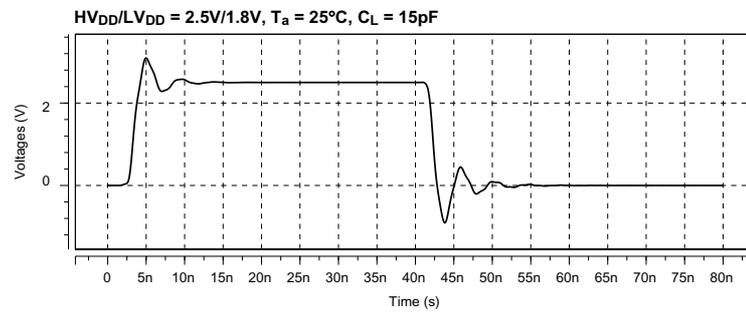


Figure 6-176 Output Waveform (HOB4AY)

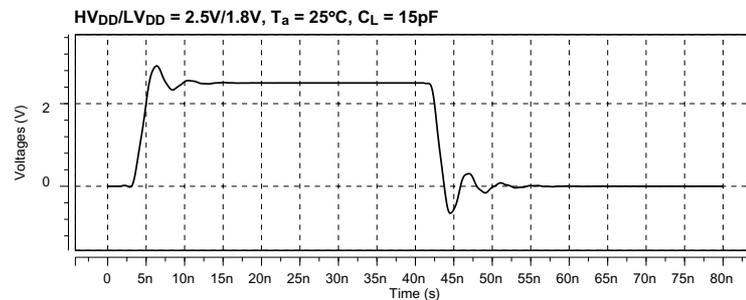


Figure 6-177 Output Waveform (HOB4BY)

- 1.8 V ± 0.15 V

Type 1

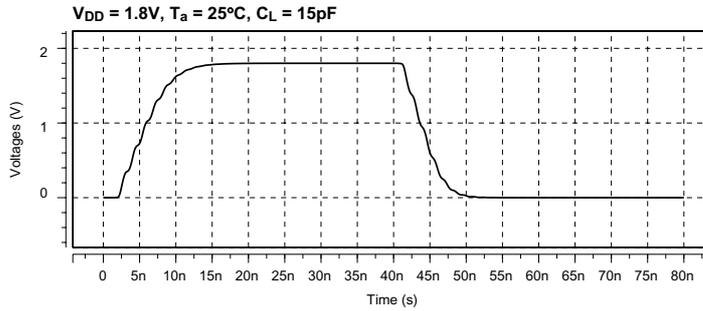


Figure 6-178 Output Waveform (MOB1AY)

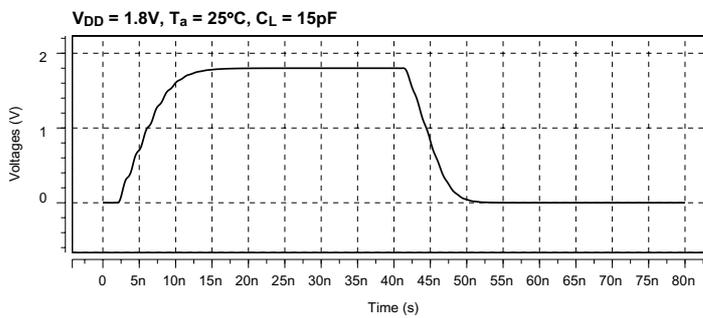


Figure 6-179 Output Waveform (MOB1BY)

Type 2

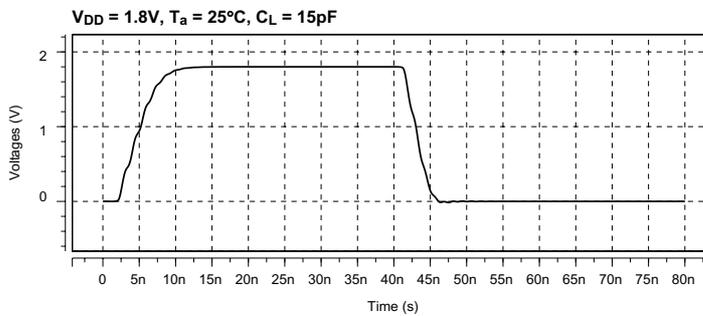


Figure 6-180 Output Waveform (MOB2AY)

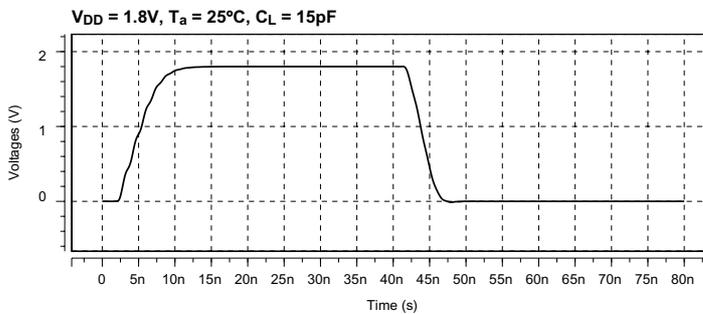


Figure 6-181 Output Waveform (MOB2BY)

Type 3

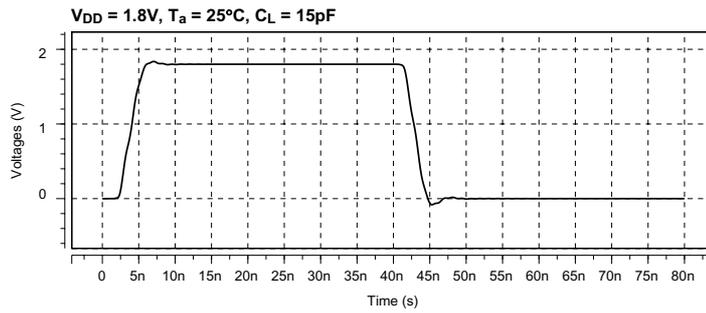


Figure 6-182 Output Waveform (MOB3AY)

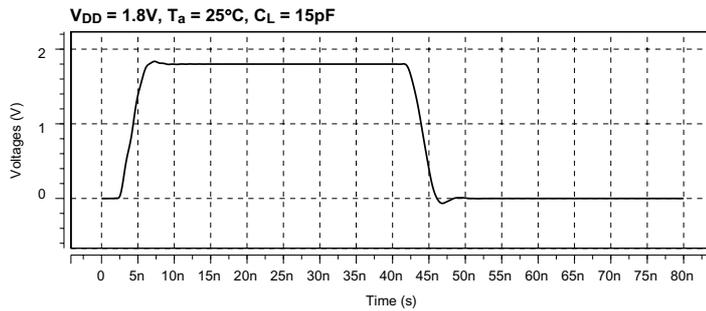


Figure 6-183 Output Waveform (MOB3BY)

Type 4

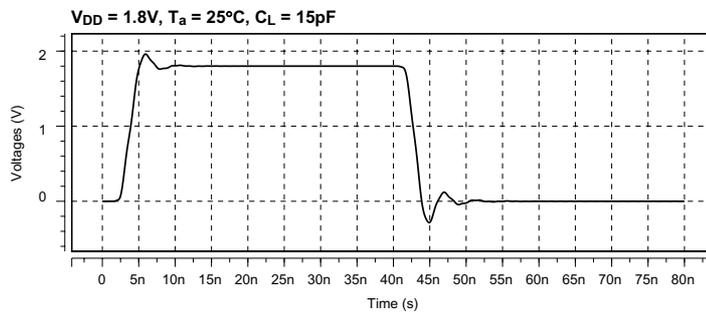


Figure 6-184 Output Waveform (MOB4AY)

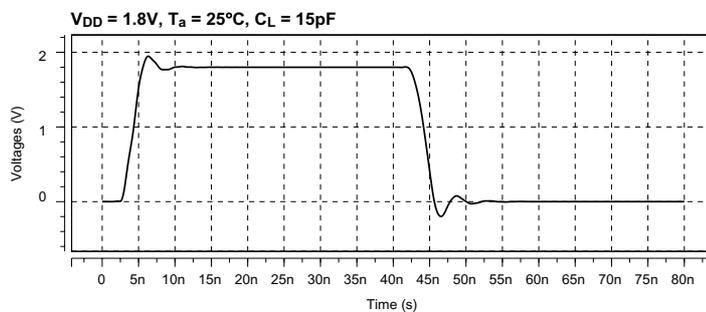


Figure 6-185 Output Waveform (MOB4BY)

- 1.5 V ± 0.1 V

Type 1

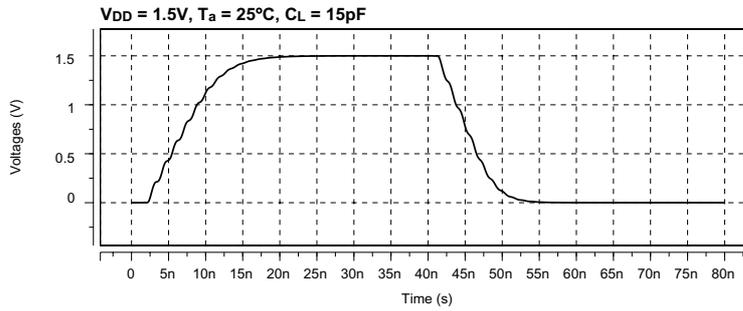


Figure 6-186 Output Waveform (MOB1AY)

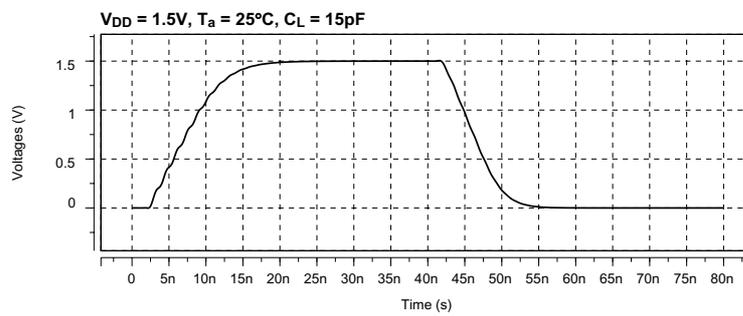


Figure 6-187 Output Waveform (MOB1BY)

Type 2

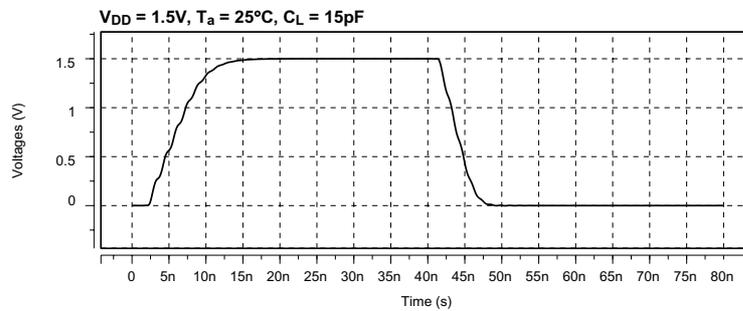


Figure 6-188 Output Waveform (MOB2AY)

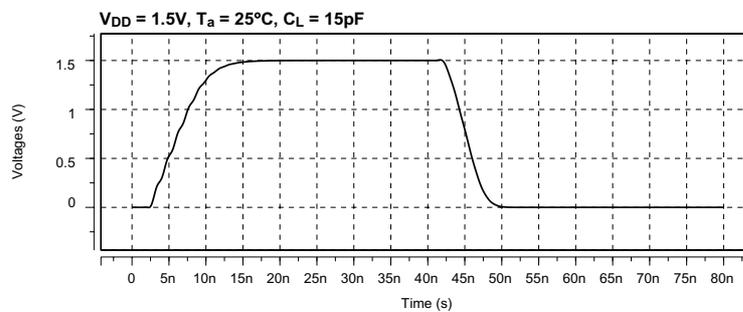


Figure 6-189 Output Waveform (MOB2BY)

Type 3

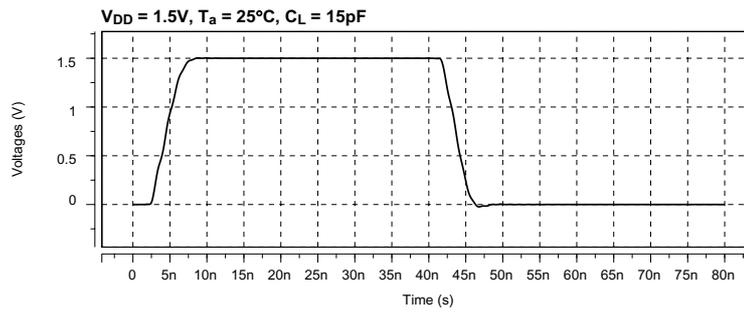


Figure 6-190 Output Waveform (MOB3AY)

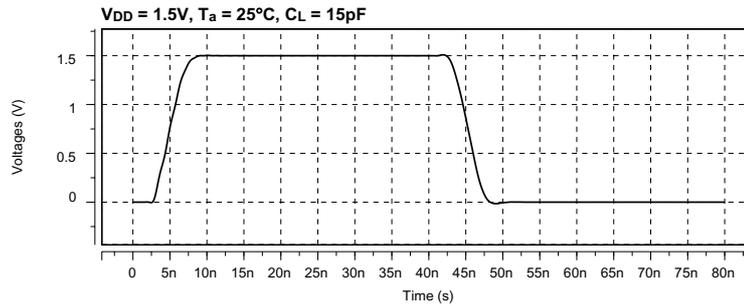


Figure 6-191 Output Waveform (MOB3BY)

Type 4

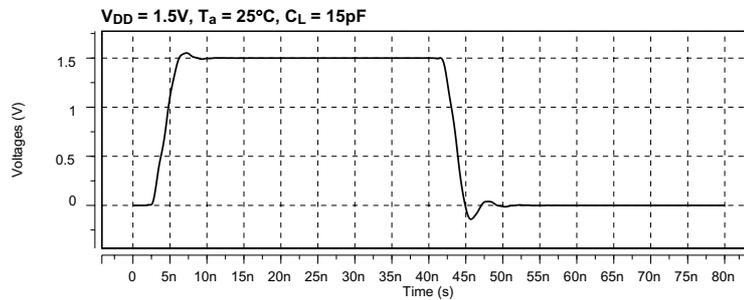


Figure 6-192 Output Waveform (MOB4AY)

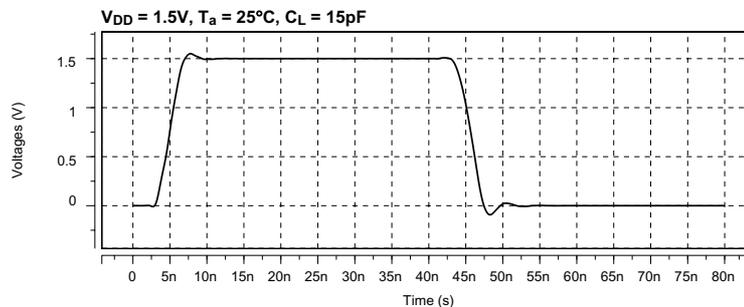


Figure 6-193 Output Waveform (MOB4BY)

6.4 Input/Output Buffer Characteristics (2.5-V Buffers: X Type)

6.4.1 Input Buffer Characteristics

Standard-cell input buffers

- 2.5 V ± 0.2 V

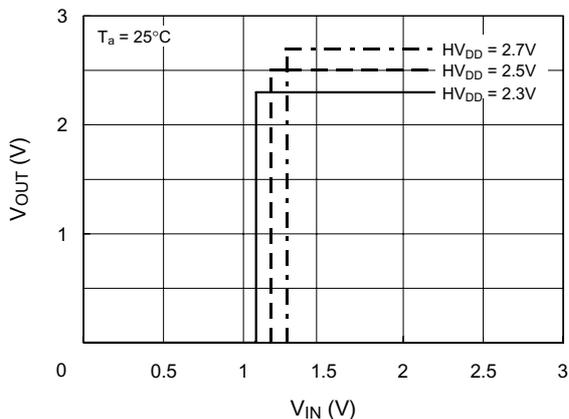


Figure 6-194 Input Characteristics (LVCMOS)

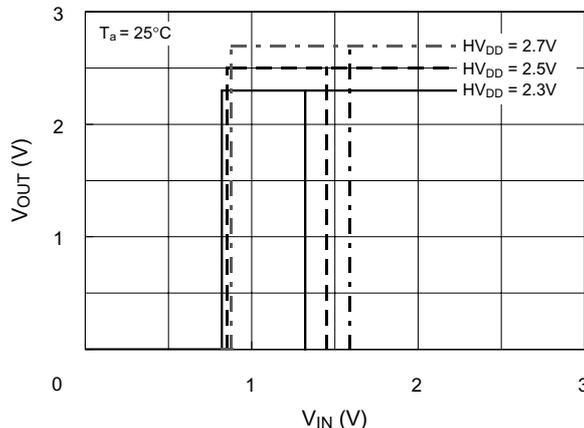


Figure 6-195 Input Characteristics (LVCMOS Schmitt)

- 1.8 V ± 0.15 V

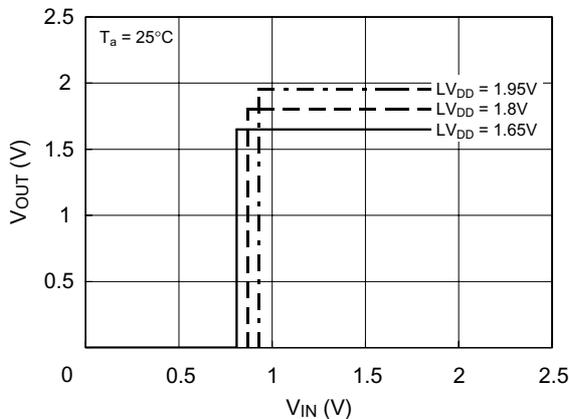


Figure 6-196 Input Characteristics (LVCMOS)

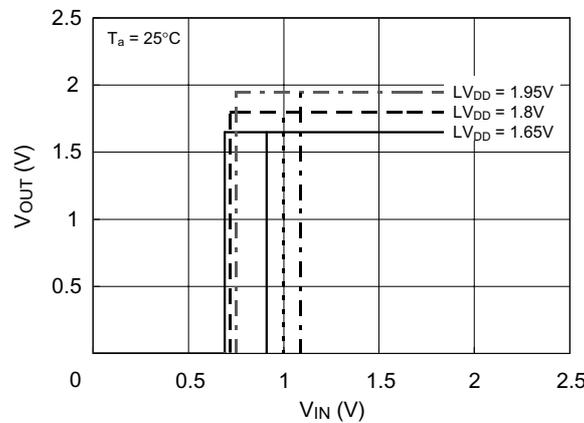


Figure 6-197 Input Characteristics (LVCMOS Schmitt)

● $1.5\text{ V} \pm 0.1\text{ V}$

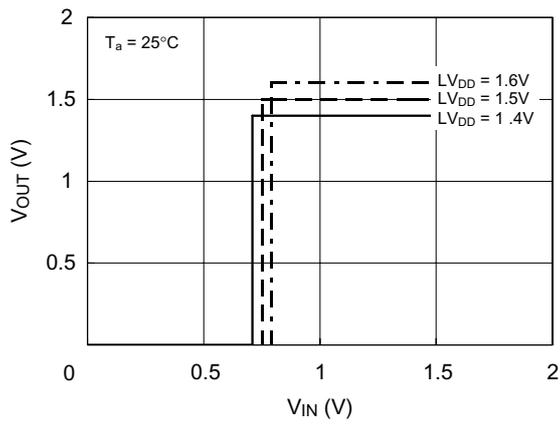


Figure 6-198 Input Characteristics (LVCMOS)

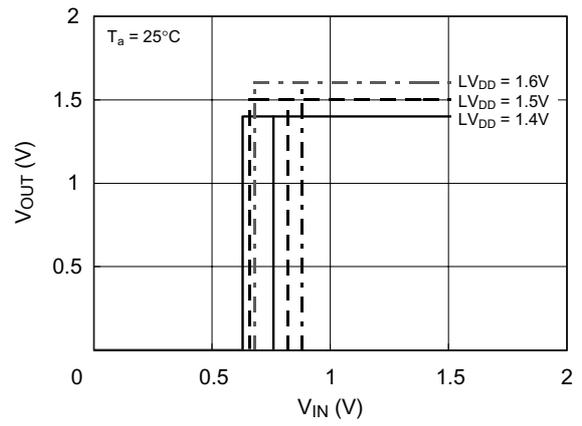


Figure 6-199 Input Characteristics (LVCMOS Schmitt)

6.4.1.1 Input Through Current

- 2.5 V ± 0.2 V

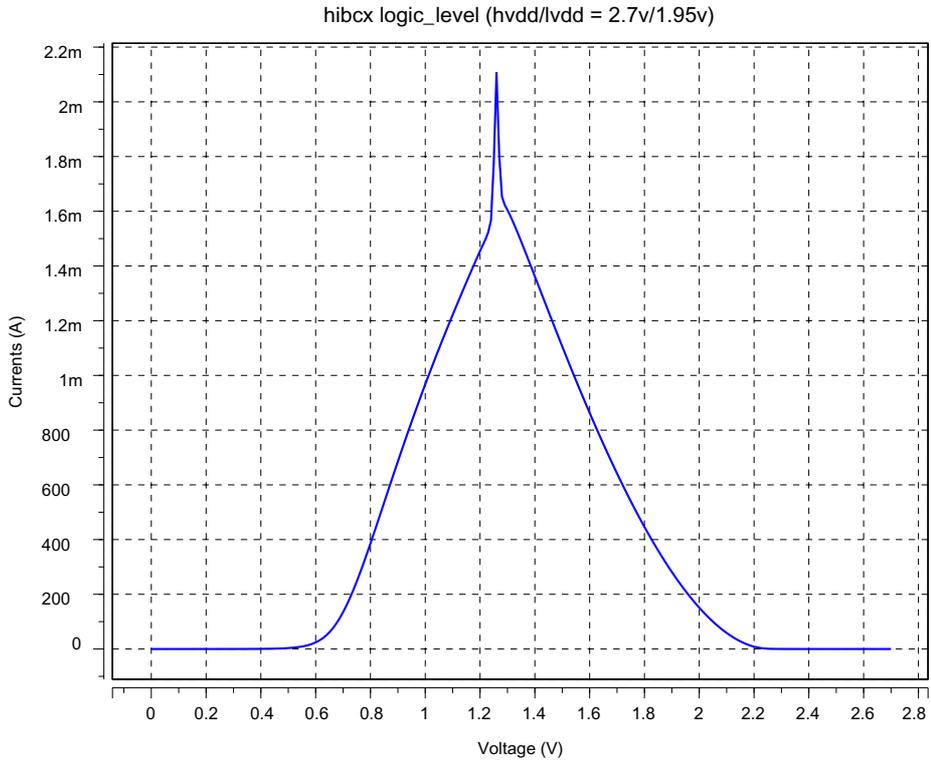


Figure 6-200 Input Through Current (LVC MOS)

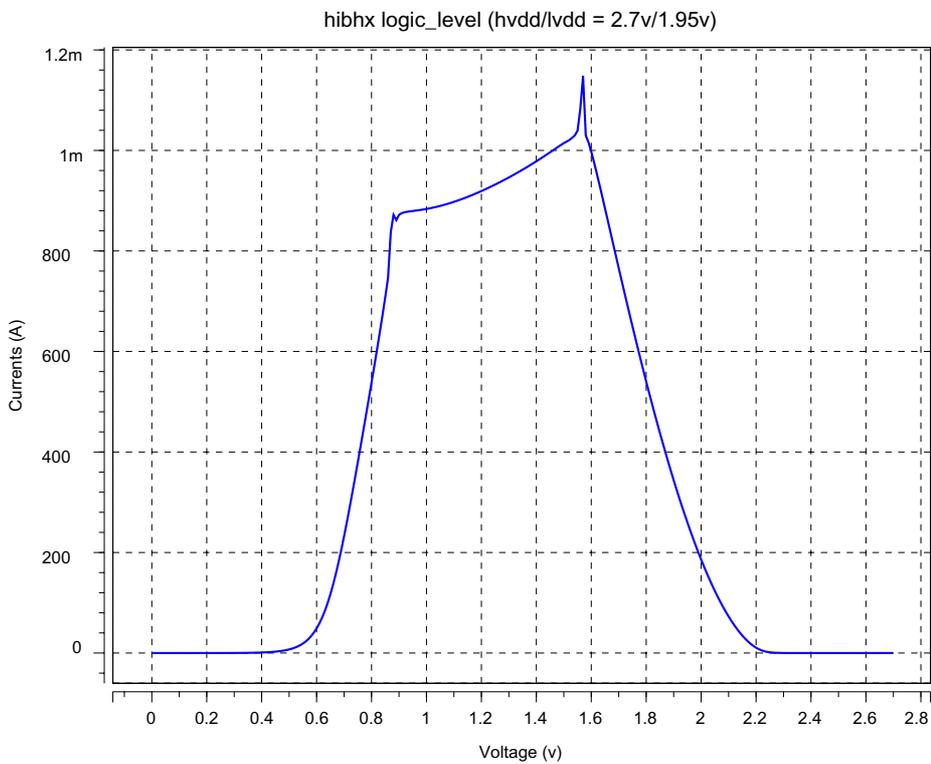


Figure 6-201 Input Through Current (LVC MOS Schmitt)

● 1.8 V ± 0.15 V

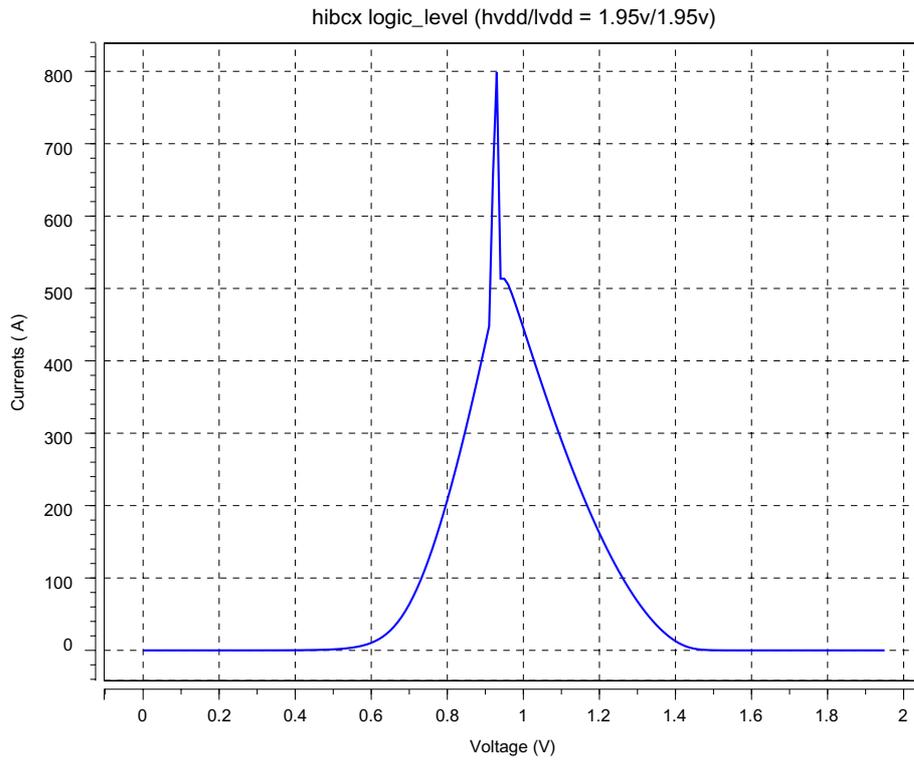


Figure 6-202 Input Through Current (LVCMOS)

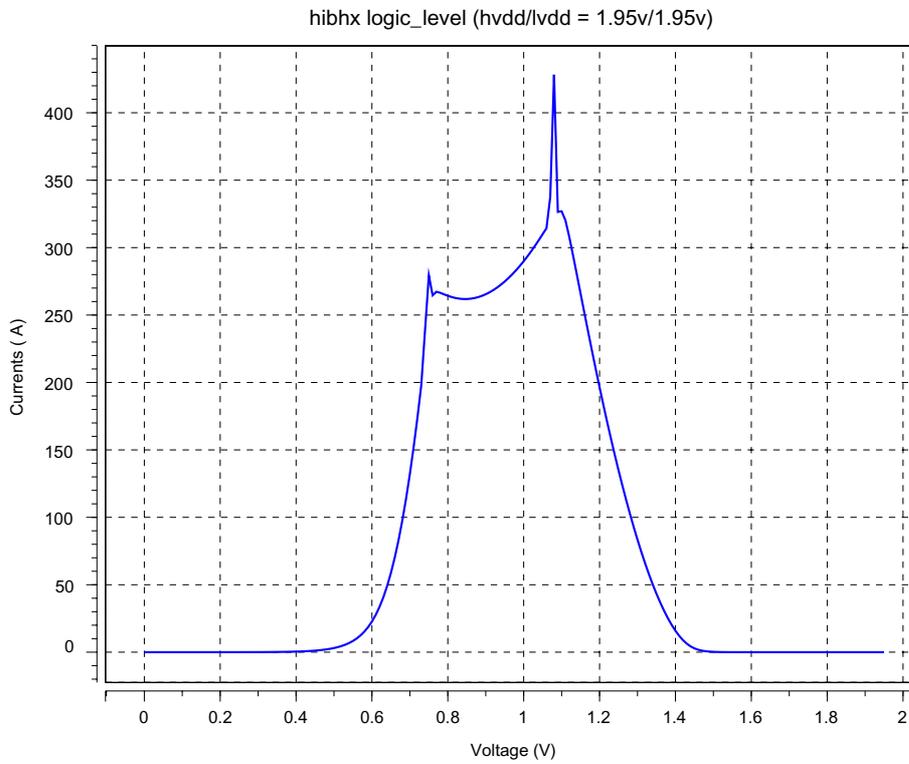


Figure 6-203 Input Through Current (LVCMOS Schmitt)

- 1.5 V \pm 0.1 V

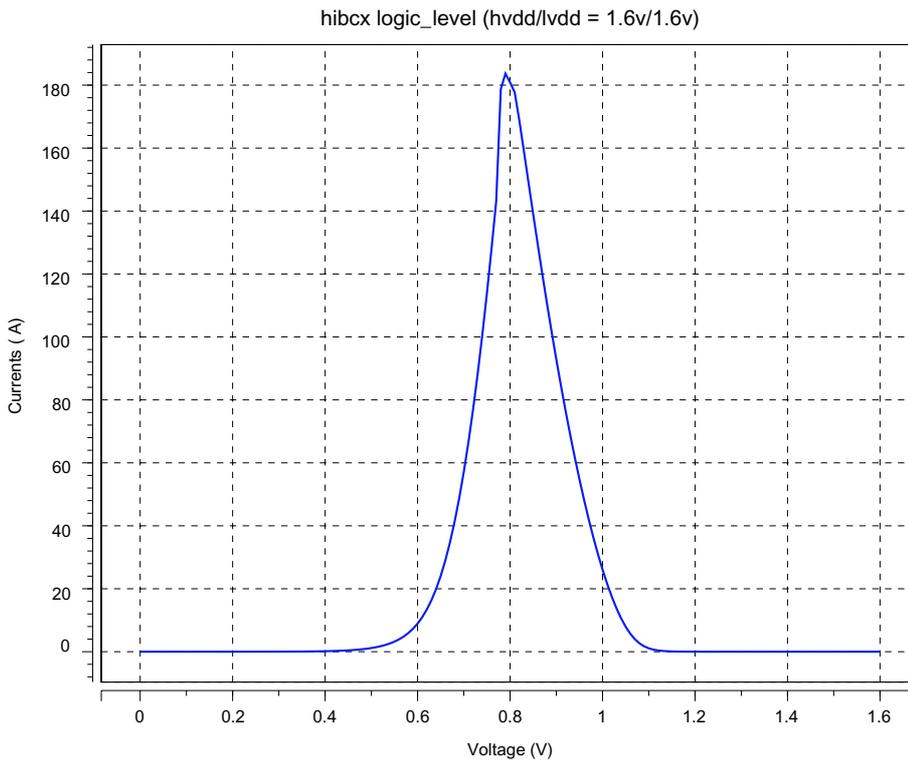


Figure 6-204 Input Through Current (LVCMOS)

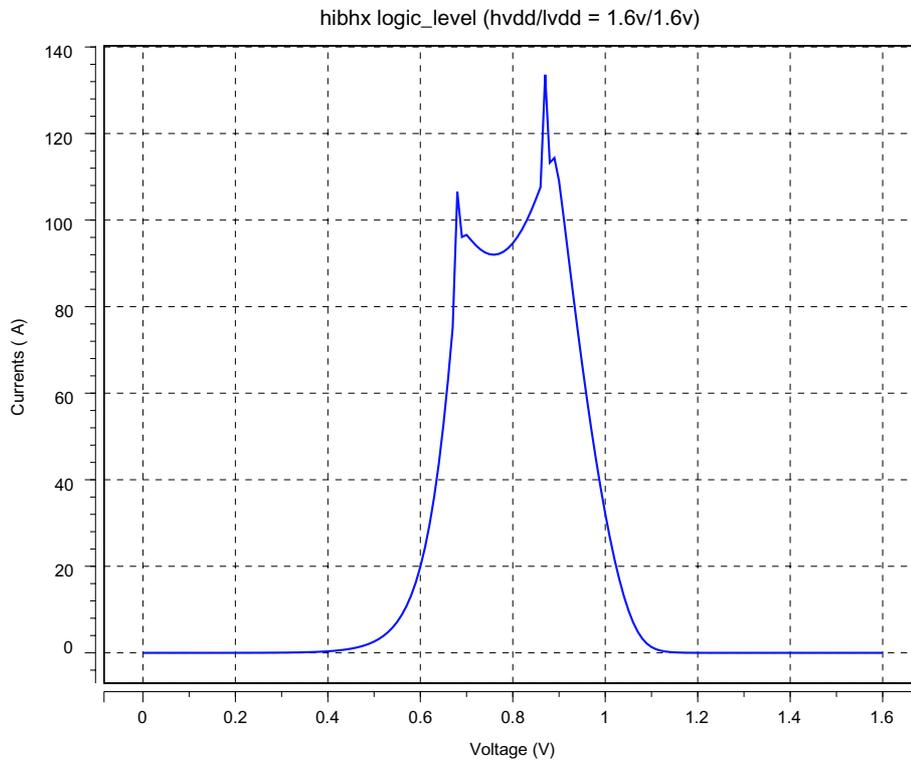


Figure 6-205 Input Through Current (LVCMOS Schmitt)

6.4.2 Output Buffer Characteristics

- (1) List of output buffer specifications

Table 6-12 Output Current Characteristics (X Type)

Type of Output Current	I_{OH}^{*1}/I_{OL}^{*2}			Unit
	HV _{DD} = 2.5 V	V _{DD} or LV _{DD} = 1.8 V	V _{DD} or LV _{DD} = 1.5 V	
Type 1	-2/2	-1.5/1.5	-1/1	mA
Type 2	-4/4	-3/3	-2/2	mA
Type 3	-8/8	-6/6	-4/4	mA
Type 4	-12/12	-9/9	-6/6	mA

Notes *1: V_{OH} = power-supply voltage -0.4 V (Power-supply voltage = 2.5 V, 1.8 V, or 1.5 V)

*2: V_{OL} = 0.4 V (Power-supply voltage = 2.5 V, 1.8 V, or 1.5 V)

(2) $I_{OL}-V_{OL}$, $I_{OH}-V_{OH}$

$I_{OL}-V_{OL}$

● $2.5\text{ V} \pm 0.2\text{ V}$

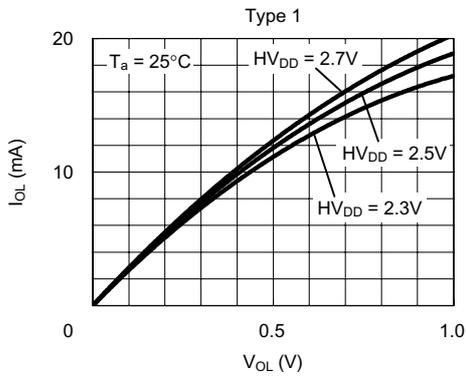


Figure 6-206

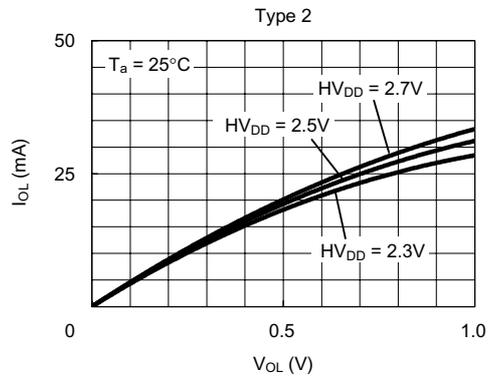


Figure 6-207

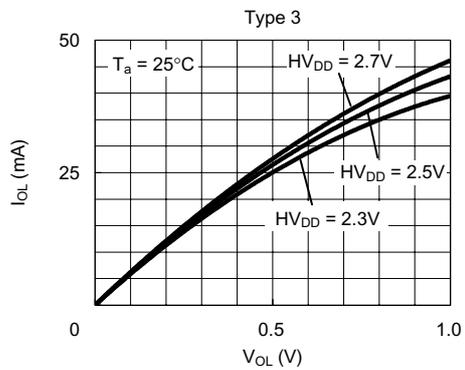


Figure 6-208

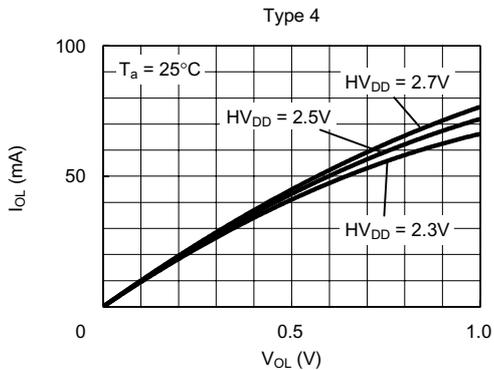


Figure 6-209

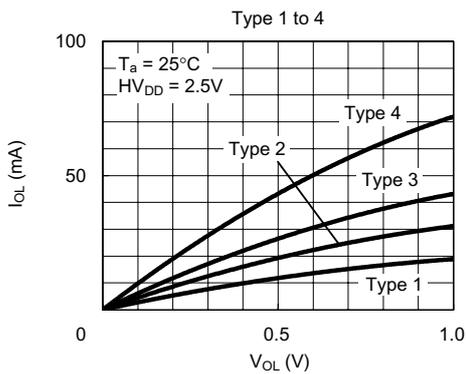


Figure 6-210

● 1.8 V ± 0.15 V

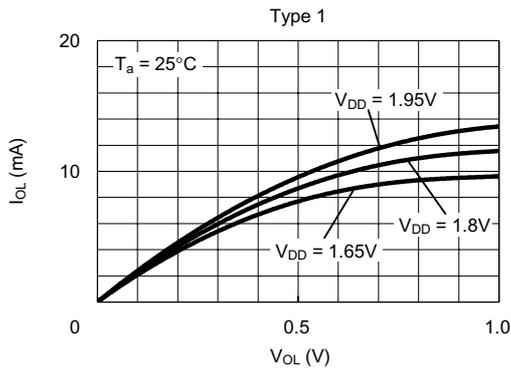


Figure 6-211

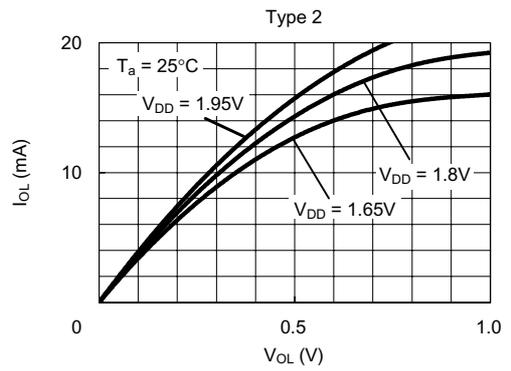


Figure 6-212

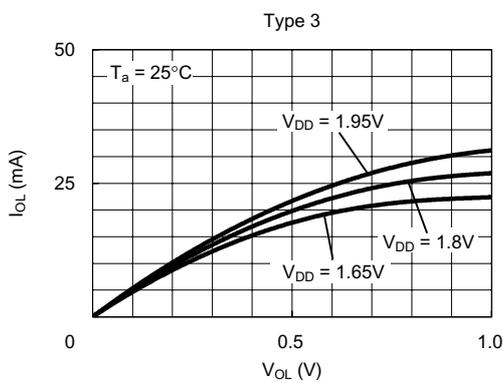


Figure 6-213

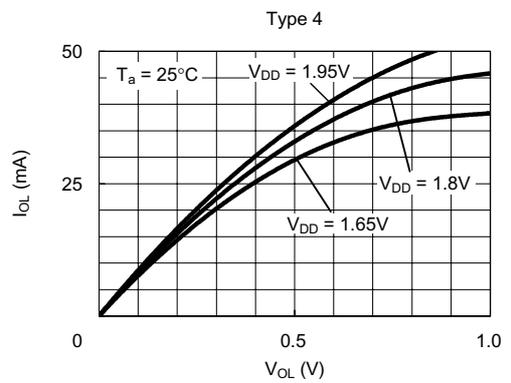


Figure 6-214

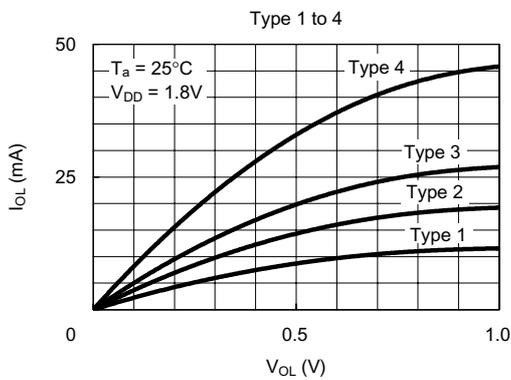


Figure 6-215

● 1.5 V ± 0.1 V

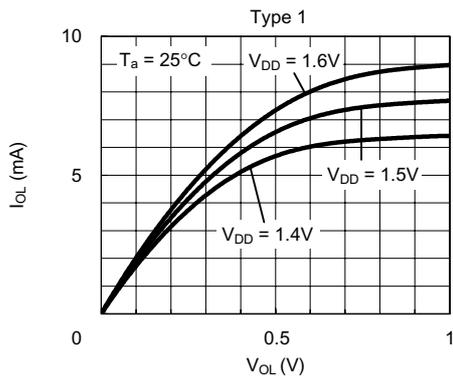


Figure 6-216

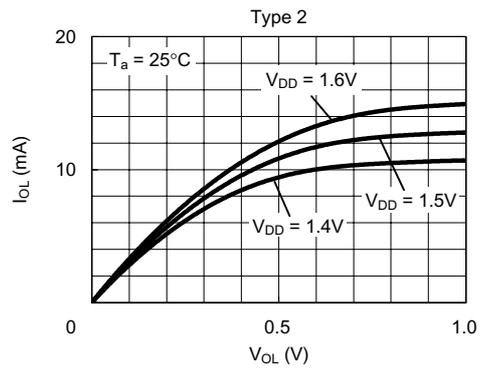


Figure 6-217

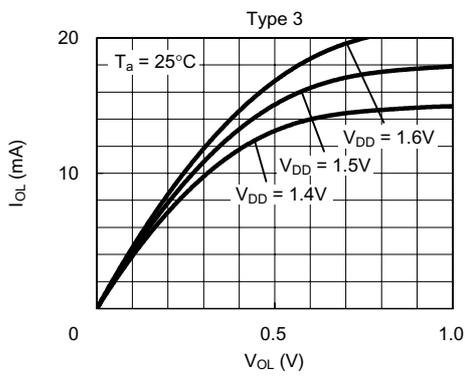


Figure 6-218

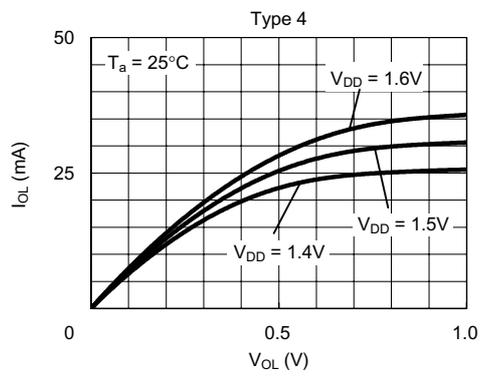


Figure 6-219

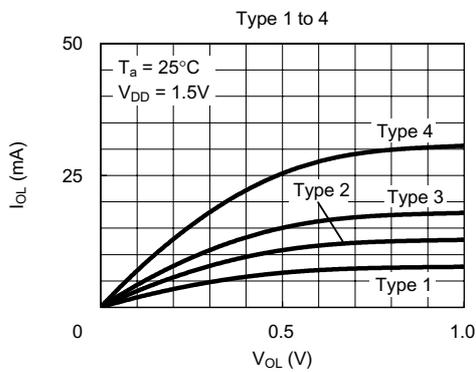


Figure 6-220

$I_{OH}-V_{OH}$

● $2.5\text{ V} \pm 0.2\text{ V}$

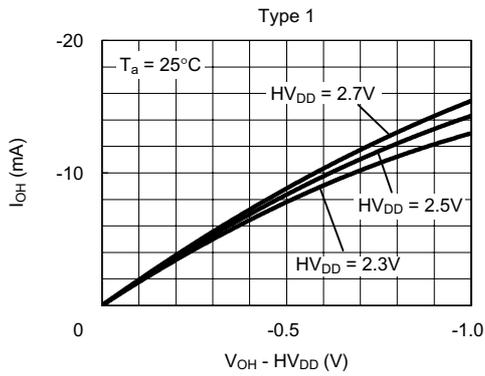


Figure 6-221

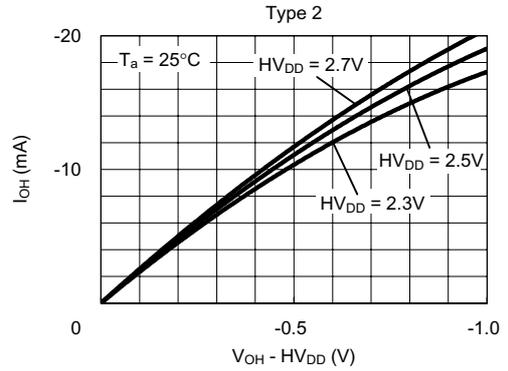


Figure 6-222

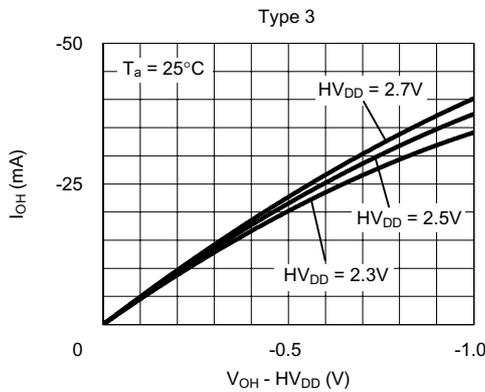


Figure 6-223

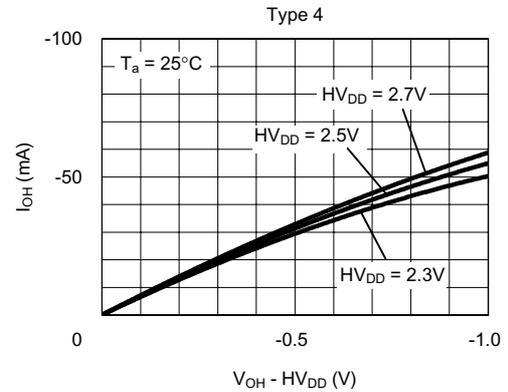


Figure 6-224

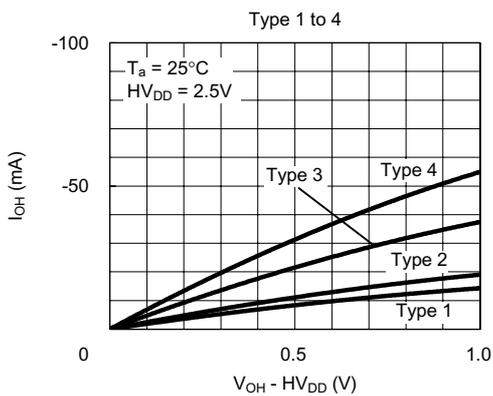


Figure 6-225

● 1.8 V ± 0.15 V

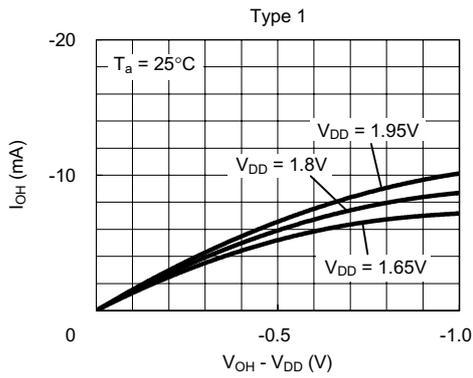


Figure 6-226

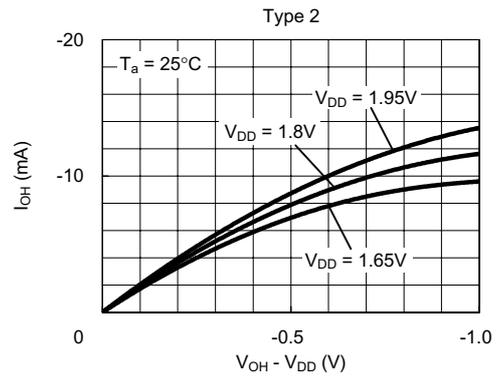


Figure 6-227

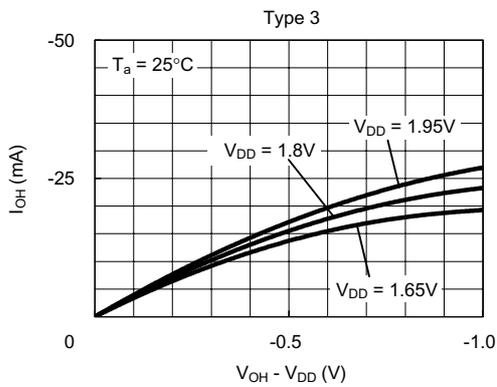


Figure 6-228

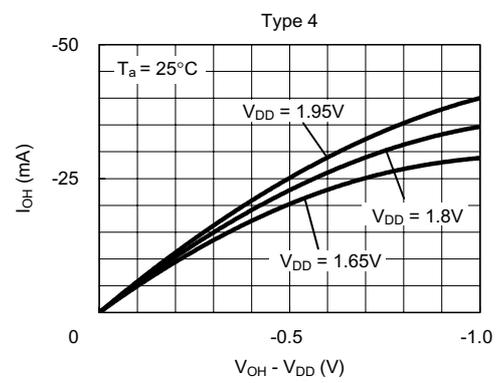


Figure 6-229

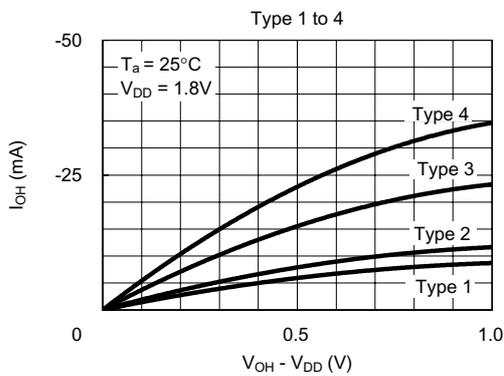


Figure 6-230

● 1.5 V ± 0.1 V

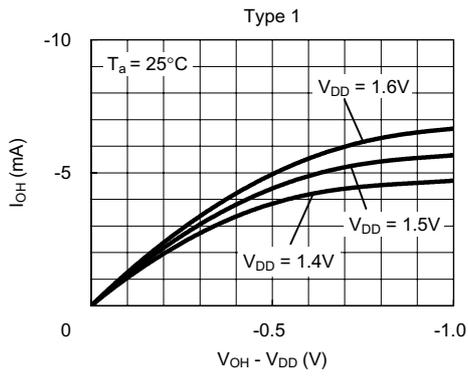


Figure 6-231

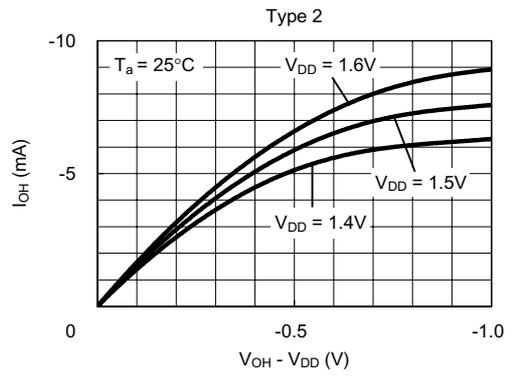


Figure 6-232

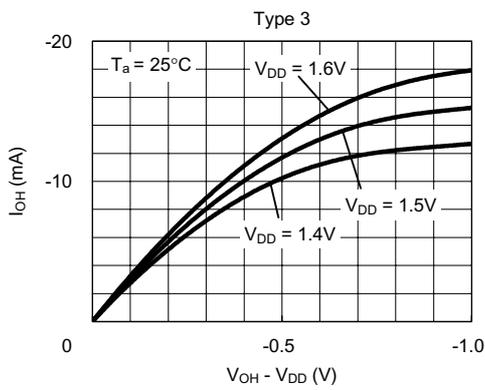


Figure 6-233

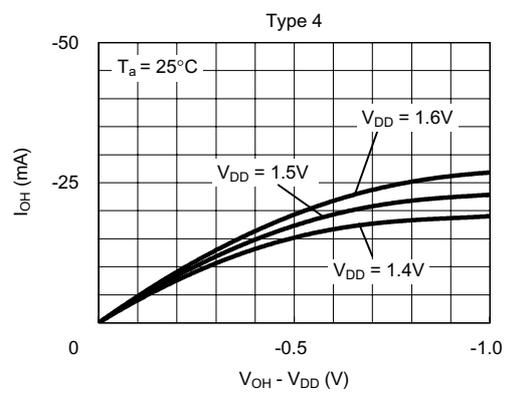


Figure 6-234

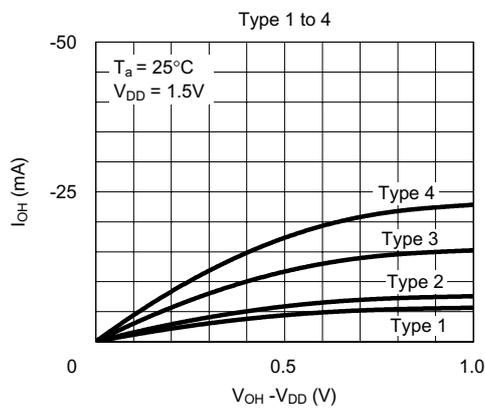


Figure 6-235

(3) I_{OH} and I_{OL} temperature characteristics

● 2.5 V ± 0.2 V

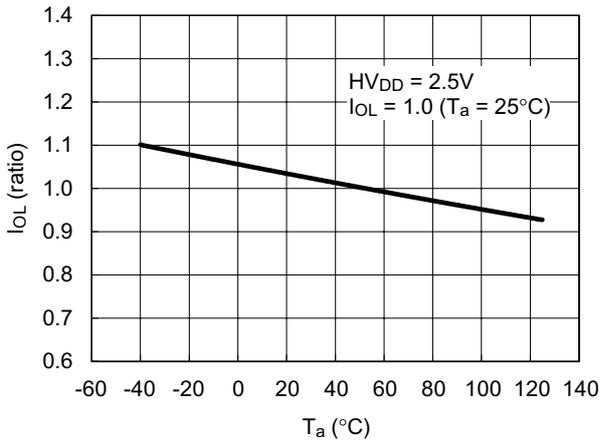


Figure 6-236 Ambient temperature (T_a) vs. Output current (I_{OL})

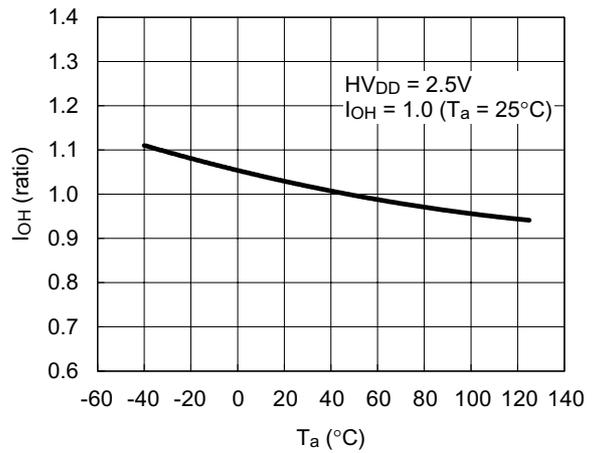


Figure 6-237 Ambient temperature (T_a) vs. Output current (I_{OH})

● 1.8 V ± 0.15 V

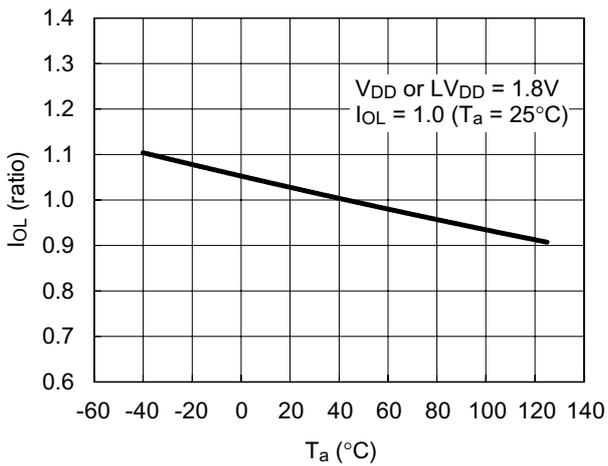


Figure 6-238 Ambient temperature (T_a) vs. Output current (I_{OL})

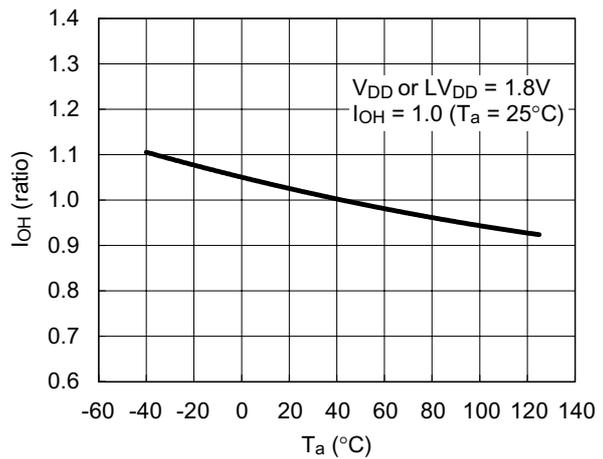


Figure 6-239 Ambient temperature (T_a) vs. Output current (I_{OH})

● 1.5 V ± 0.1 V

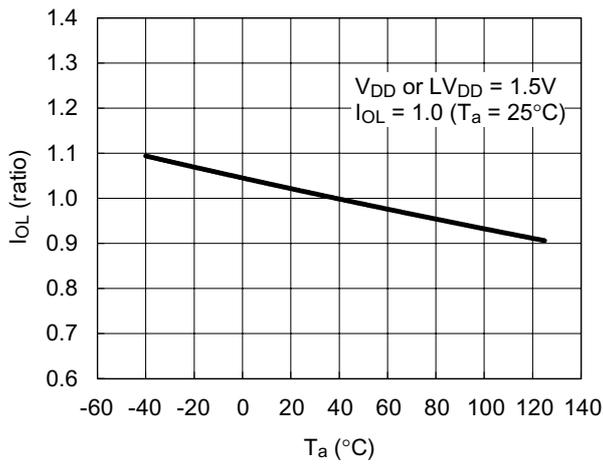


Figure 6-240 Ambient temperature (T_a) vs. Output current (I_{oL})

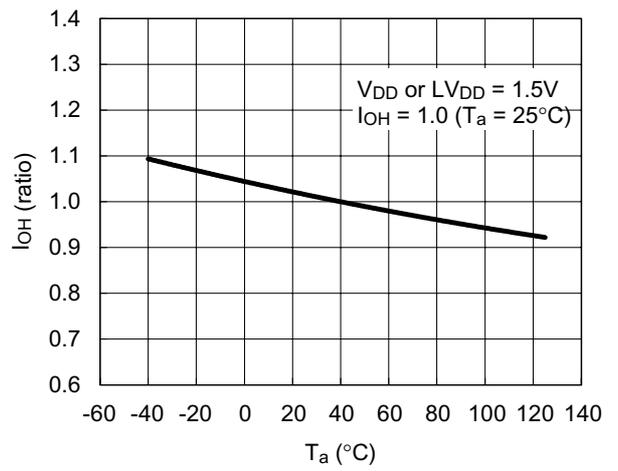


Figure 6-241 Ambient temperature (T_a) vs. Output current (I_{oH})

(4) $t_{pHL} - C_L, t_{pLH} - C_L$

● 2.5 V ± 0.2 V

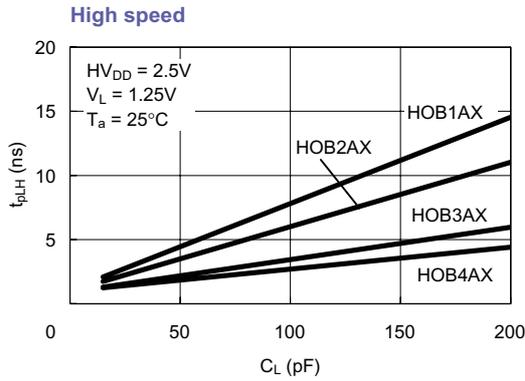


Figure 6-242 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

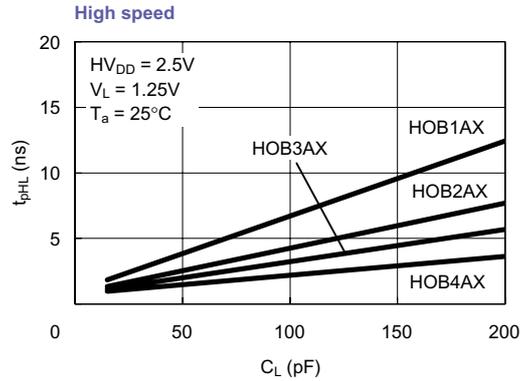


Figure 6-243 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

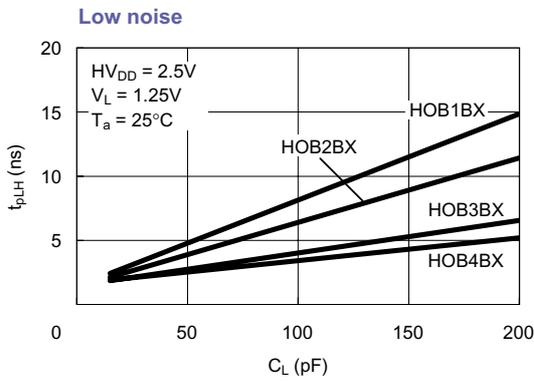


Figure 6-244 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

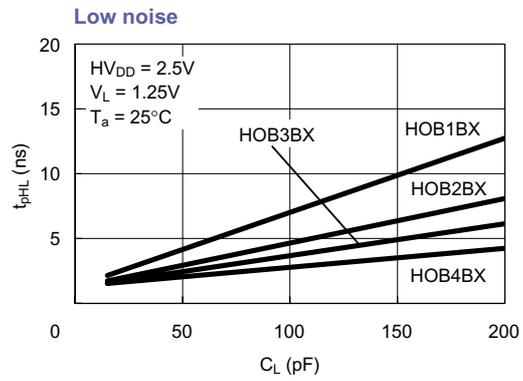


Figure 6-245 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

● 1.8 V ± 0.15 V

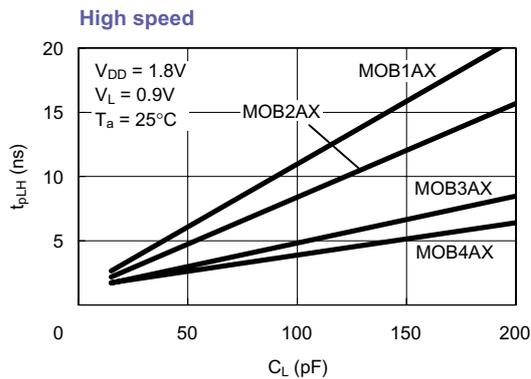


Figure 6-246 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

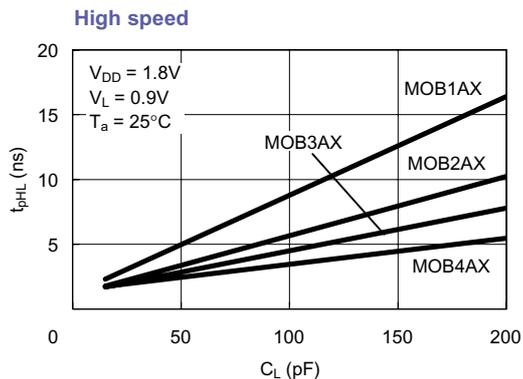


Figure 6-247 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

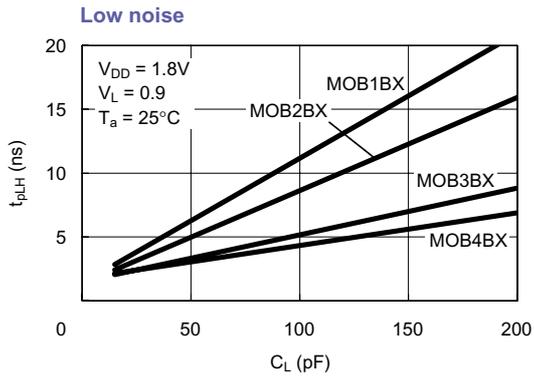


Figure 6-248 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

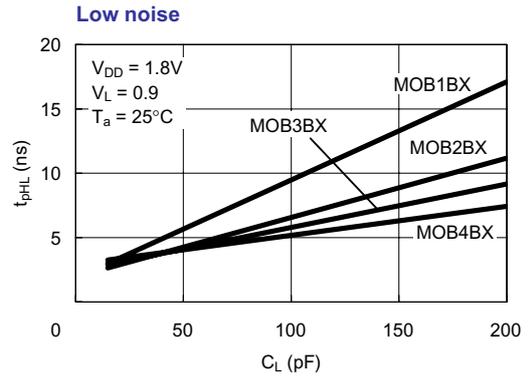


Figure 6-249 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

● $1.5 V \pm 0.1 V$

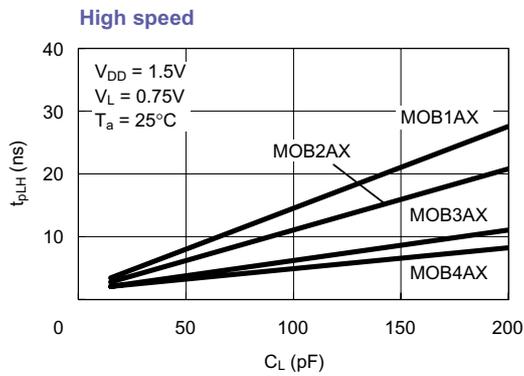


Figure 6-250 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

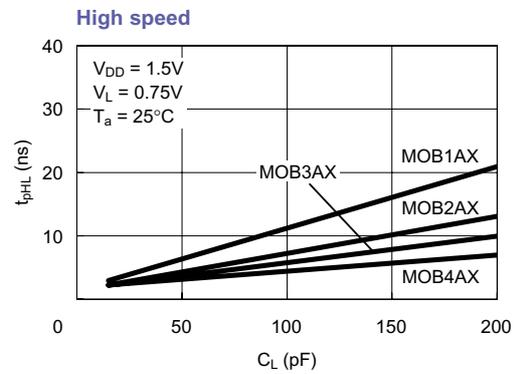


Figure 6-251 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

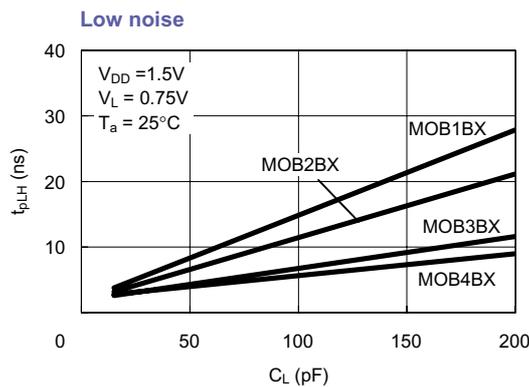


Figure 6-252 Output Delay Time (t_{pLH}) vs. Output load Capacitance (C_L)

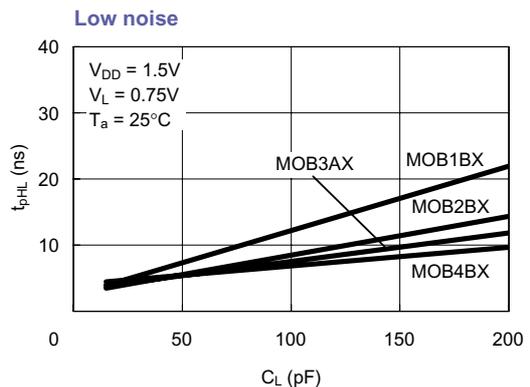


Figure-253 Output Delay Time (t_{pHL}) vs. Output load Capacitance (C_L)

(5) $t_r(10\%-90\%) - C_L$, $t_f(10\%-90\%) - C_L$

● $2.5\text{ V} \pm 0.2\text{ V}$

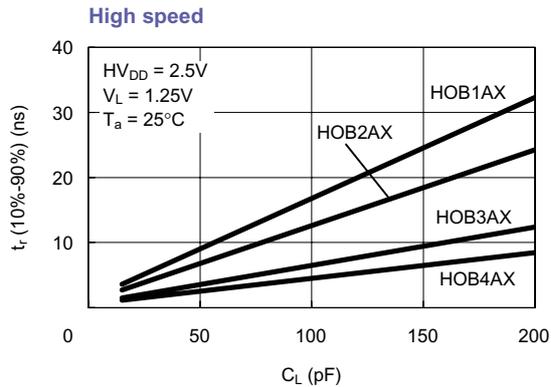


Figure 6-254 Rising Time (t_r) vs. Output load Capacitance (C_L)

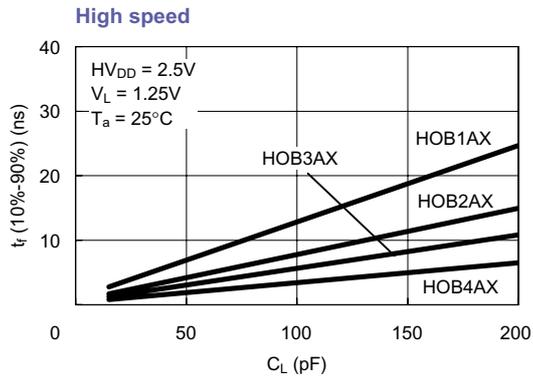


Figure 6-255 Falling Time (t_f) vs. Output load Capacitance (C_L)

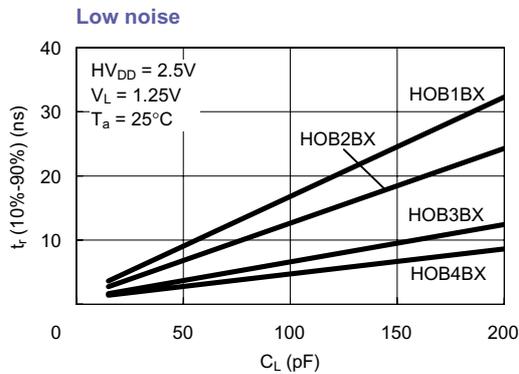


Figure 6-256 Rising Time (t_r) vs. Output load Capacitance (C_L)

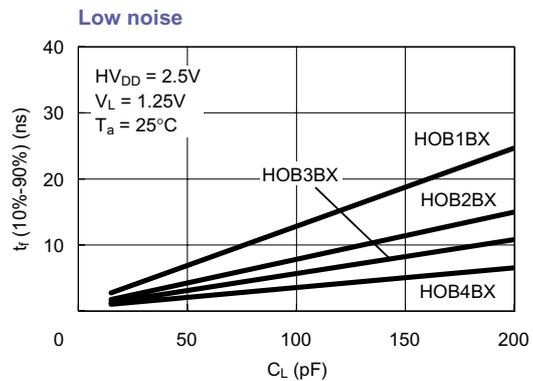


Figure 6-257 Falling Time (t_f) vs. Output load Capacitance (C_L)

● $1.8\text{ V} \pm 0.15\text{ V}$

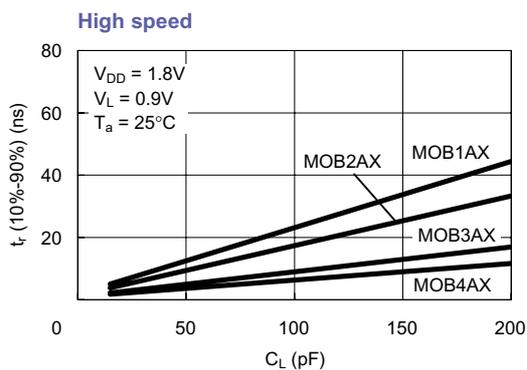


Figure 6-258 Rising Time (t_r) vs. Output load Capacitance (C_L)

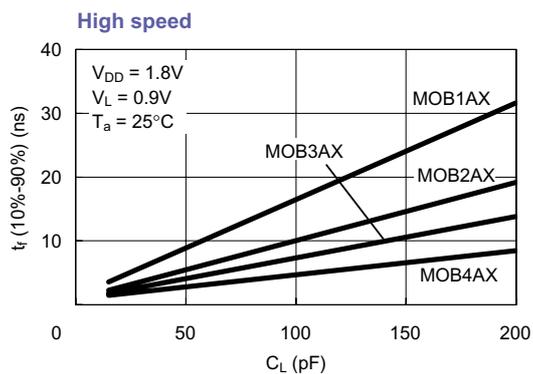


Figure 6-259 Falling Time (t_f) vs. Output load Capacitance (C_L)

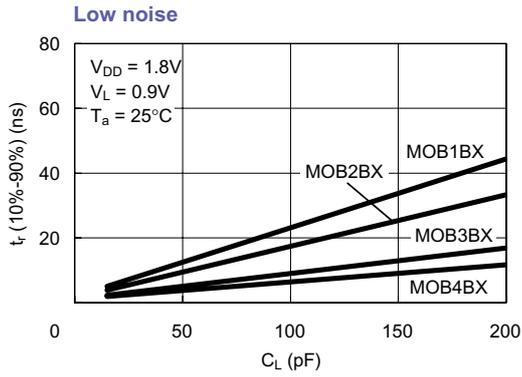


Figure 6-260 Rising Time (t_r) vs. Output load Capacitance (C_L)

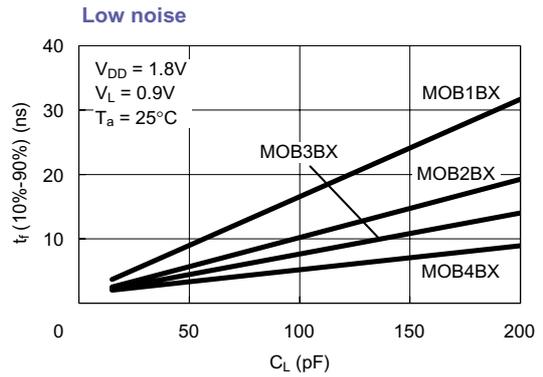


Figure 6-261 Falling Time (t_f) vs. Output load Capacitance (C_L)

● 1.5 V ± 0.1 V

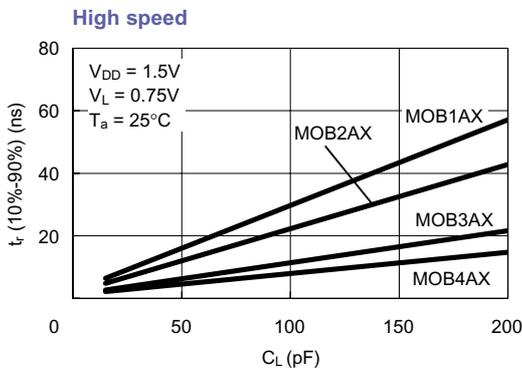


Figure 6-262 Rising Time (t_r) vs. Output load Capacitance (C_L)

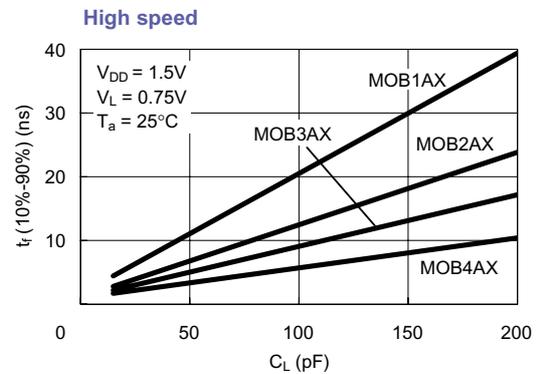


Figure 6-263 Falling Time (t_f) vs. Output load Capacitance (C_L)

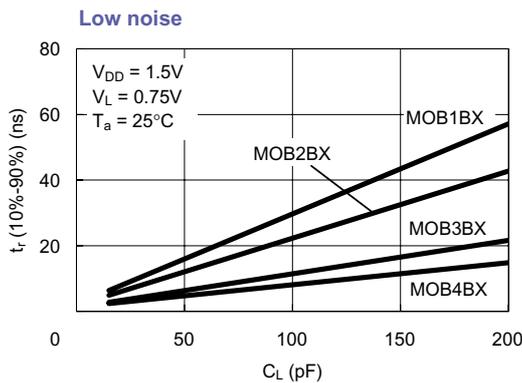


Figure 6-264 Rising Time (t_r) vs. Output load Capacitance (C_L)

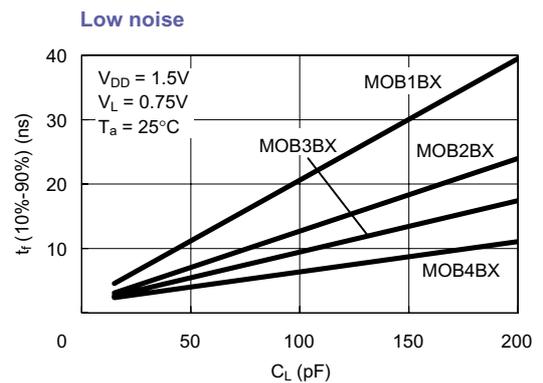


Figure 6-265 Falling Time (t_f) vs. Output load Capacitance (C_L)

(6) Recommended range of load capacitances for output buffers

Table 6-13 lists the recommended range of load capacitances for output buffers, classified by drive capability (consult Table 6-13 to select the most suitable output buffer for your design). Note that if output buffers are used with a smaller load capacitance beyond the recommended range of load capacitances, the output signal may have larger overshoots or undershoots.

Table 6-13 Recommended Range of Output Buffer Load Capacitances

Type of Output Buffer	Example	Recommended Range of Load Capacitances (pF)
Type 1	MOB1ATX	0–40
Type 2	MOB2ATX	20–100
Type 3	MOB3ATX	50–150
Type 4	MOB4ATX	100–200

(7) $f_{max}-C_L$

- 2.5 V ± 0.2 V

HIGH SPEED

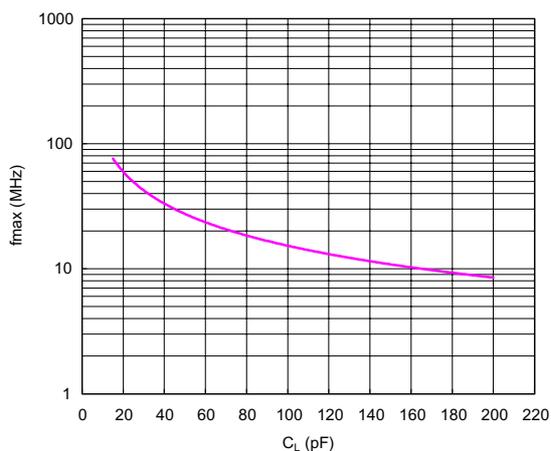


Figure 6-266 Output Operating Frequency “HOB1AX”

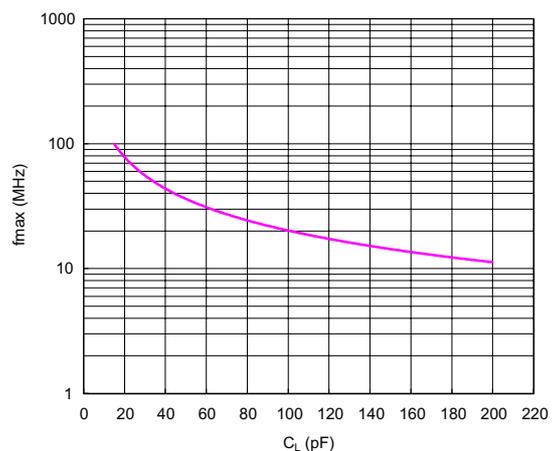


Figure 6-267 Output Operating Frequency “HOB2AX”

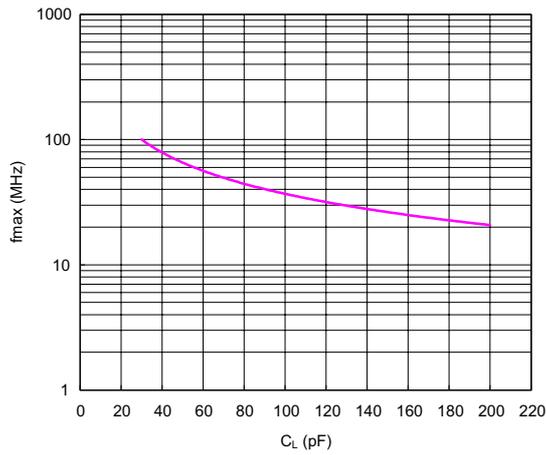


Figure 6-268 Output Operating Frequency “HOB3AX”

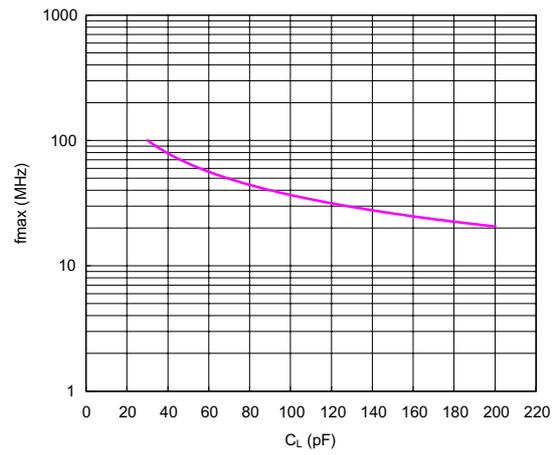


Figure 6-269 Output Operating Frequency “HOB4AX”

LOW NOISE

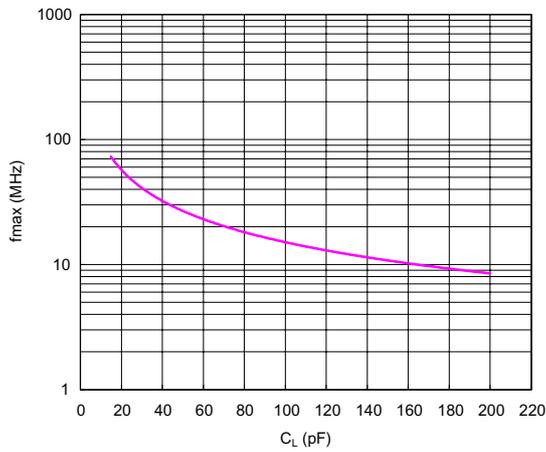


Figure 6-270 Output Operating Frequency “HOB1BX”

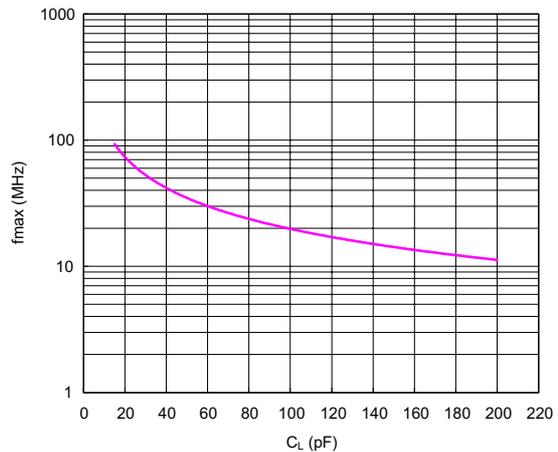


Figure 6-271 Output Operating Frequency “HOB2BX”

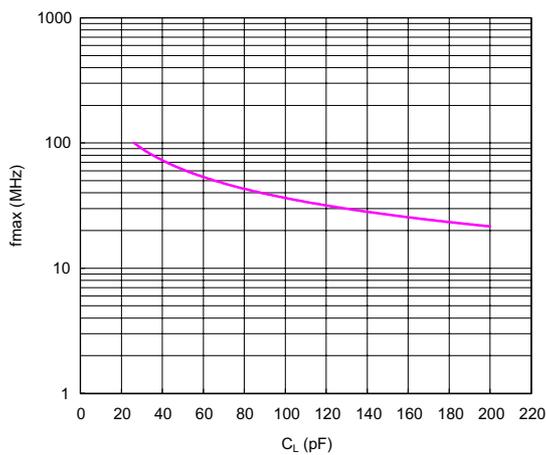


Figure 6-272 Output Operating Frequency “HOB3BX”

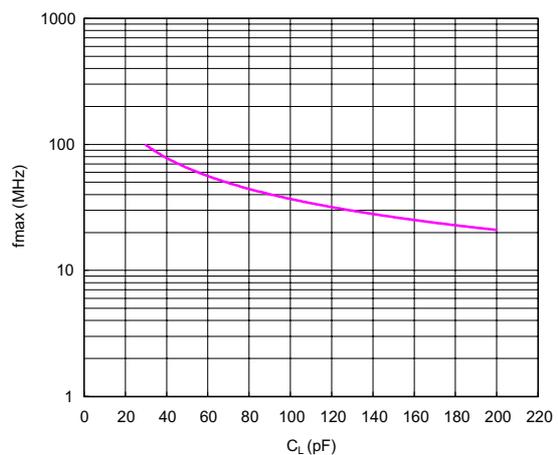


Figure 6-273 Output Operating Frequency “HOB4BX”

● 1.8 V ± 0.15 V

HIGH SPEED

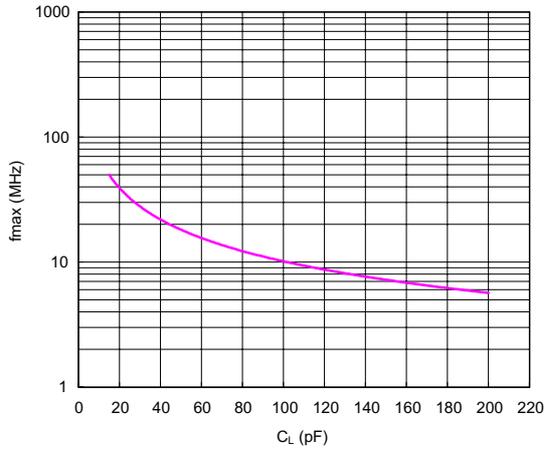


Figure 6-274 Output Operating Frequency “MOB1AX”

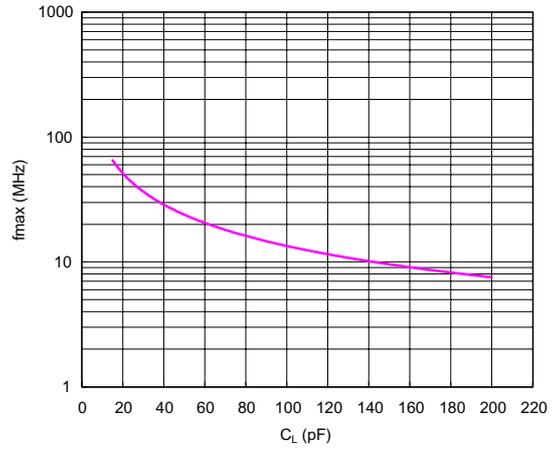


Figure 6-275 Output Operating Frequency “MOB2AX”

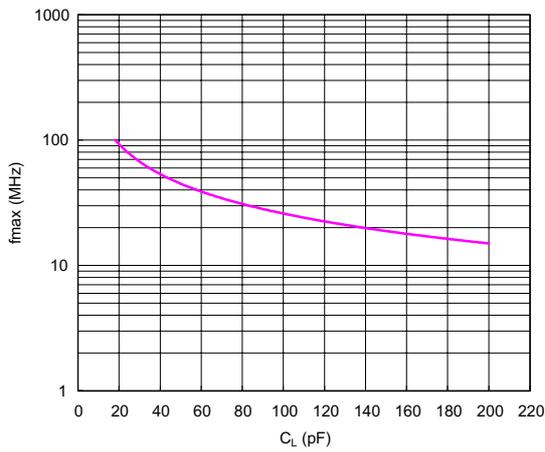


Figure 6-276 Output Operating Frequency “MOB3AX”

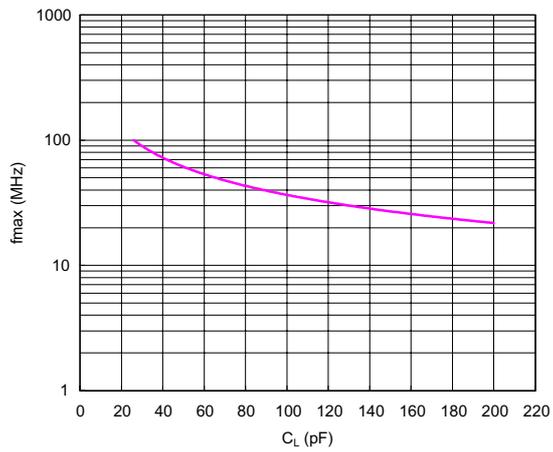


Figure 6-277 Output Operating Frequency “MOB4AX”

LOW NOISE

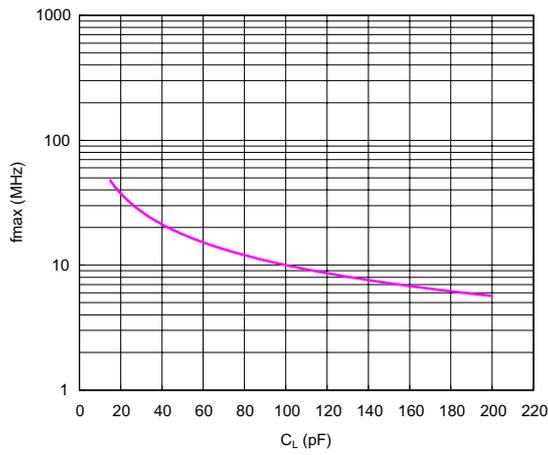


Figure 6-278 Output Operating Frequency “MOB1BX”

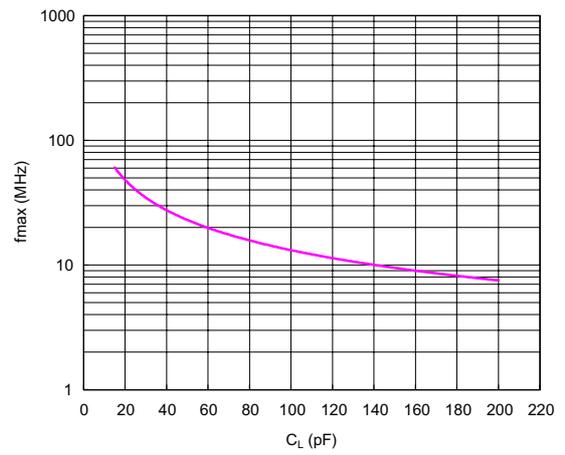


Figure 6-279 Output Operating Frequency “MOB2BX”

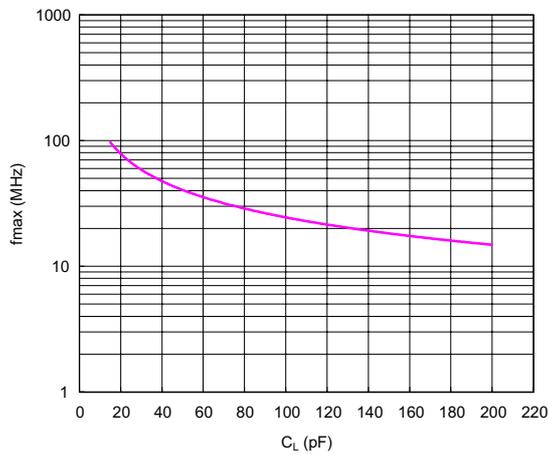


Figure 6-280 Output Operating Frequency “MOB3BX”

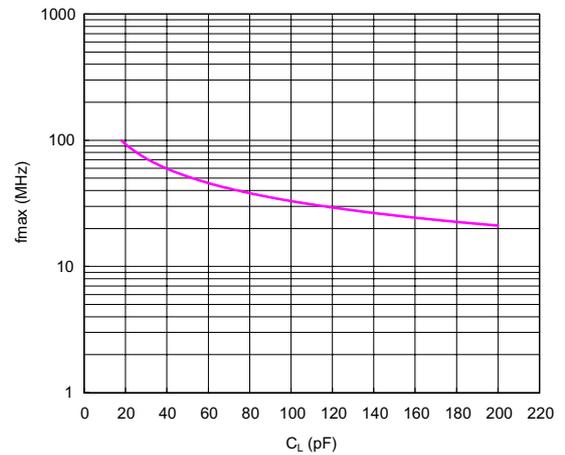


Figure 6-281 Output Operating Frequency “MOB4BX”

● 1.5 V ± 0.1 V

HIGH SPEED

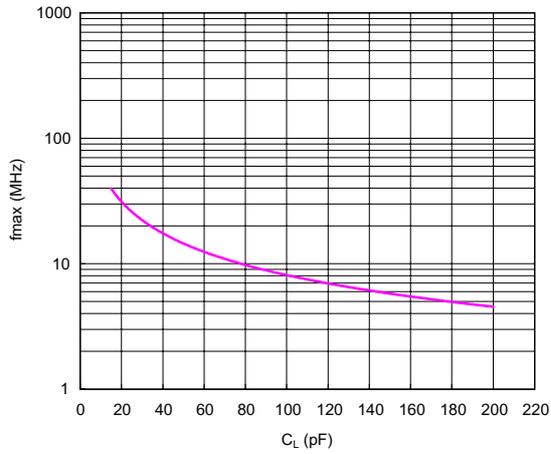


Figure 6-282 Output Operating Frequency “MOB1AX”

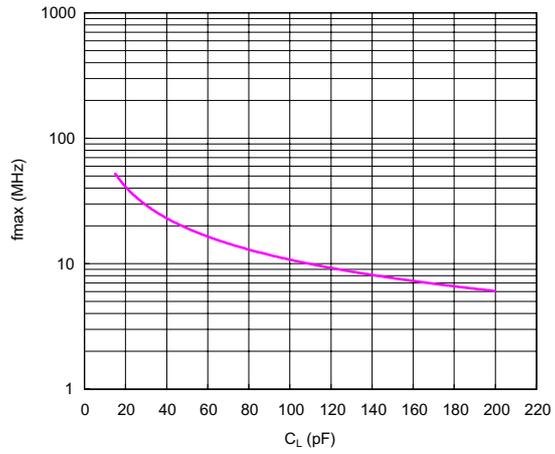


Figure 6-283 Output Operating Frequency “MOB2AX”

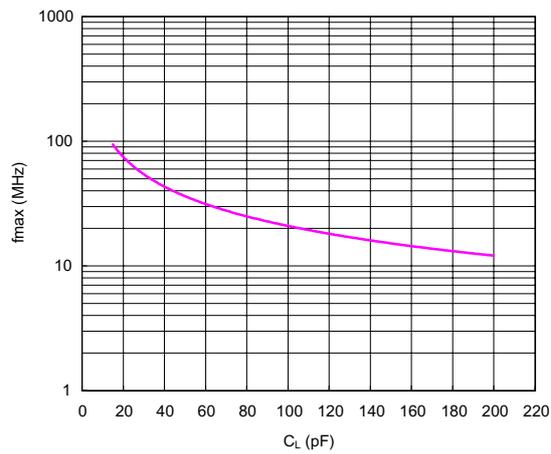


Figure 6-284 Output Operating Frequency “MOB3AX”

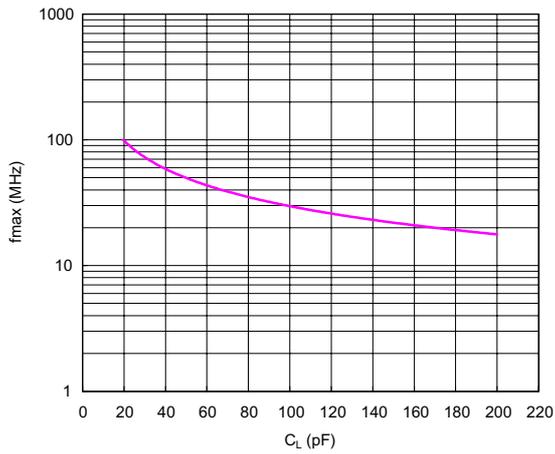


Figure 6-285 Output Operating Frequency “MOB4AX”

LOW NOISE

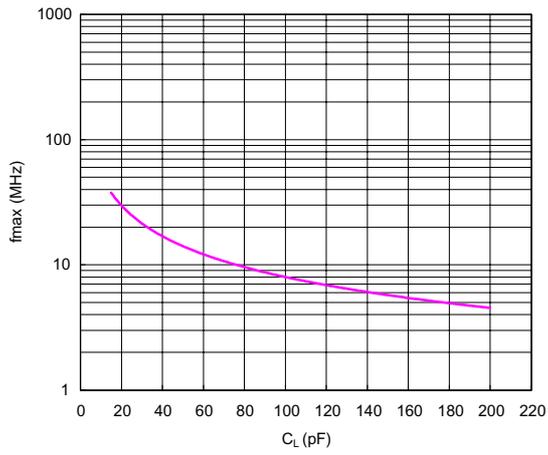


Figure 6-286 Output Operating Frequency “MOB1BX”

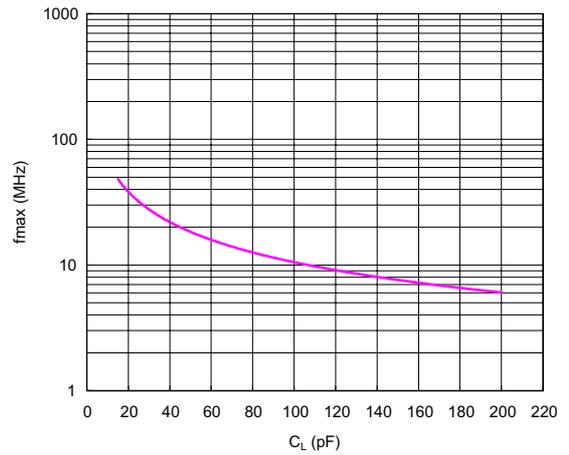


Figure 6-287 Output Operating Frequency “MOB2BX”

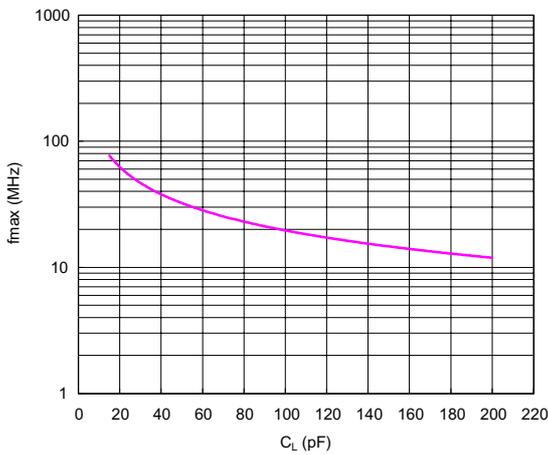


Figure 6-288 Output Operating Frequency “MOB3BX”

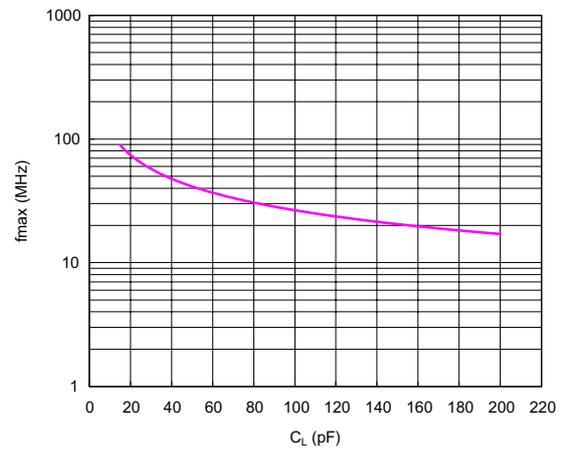


Figure 6-289 Output Operating Frequency “MOB4BX”

(8) Pull-up/pull-down characteristics

- 2.5 V ± 0.2 V

Pull-up Characteristics

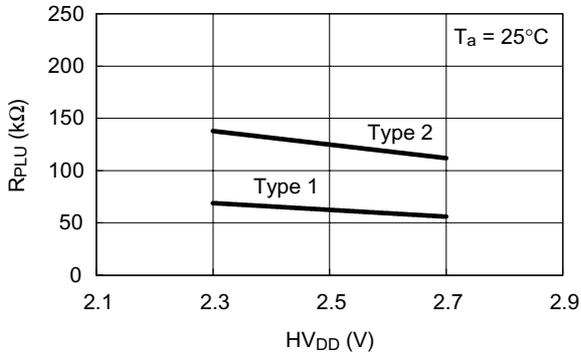


Figure 6-290 Pull-up Resistance (R_{PLU}) vs. HV_{DD}

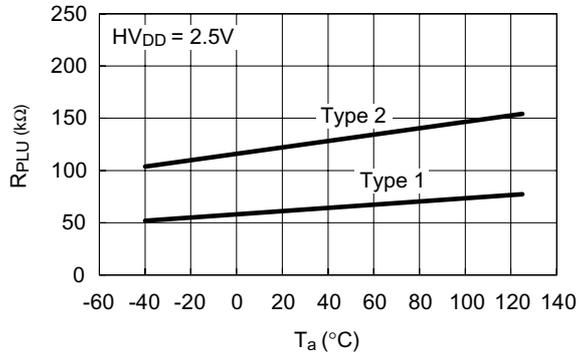


Figure 6-291 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

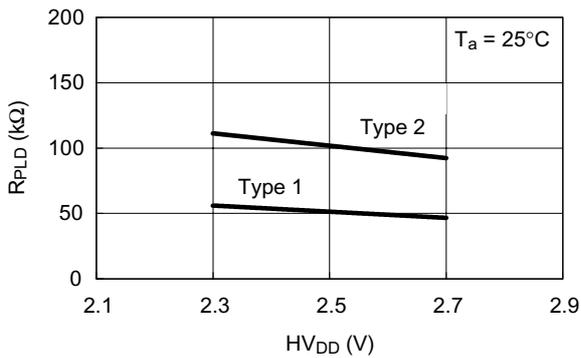


Figure 6-292 Pull-down Resistance (R_{PLD}) vs. HV_{DD}

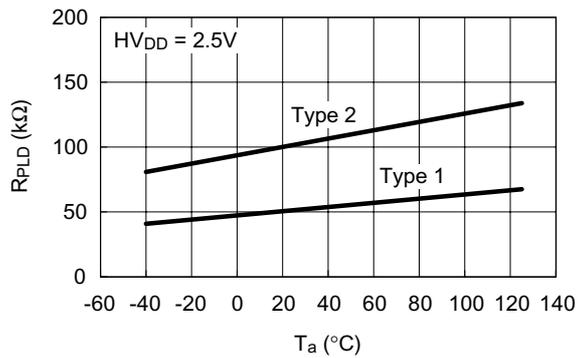


Figure 6-293 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

- 1.8 V ± 0.15 V

Pull-up Characteristics

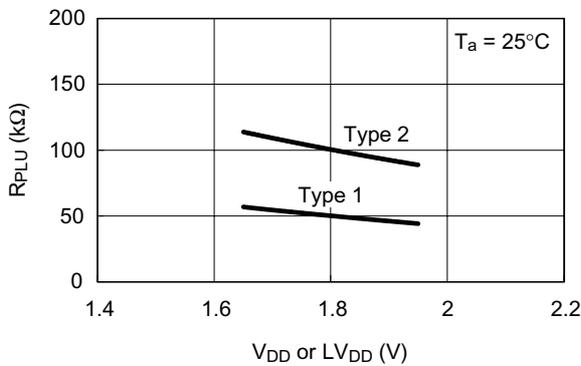


Figure 6-294 Pull-up Resistance (R_{PLU}) vs. V_{DD} (LV_{DD})

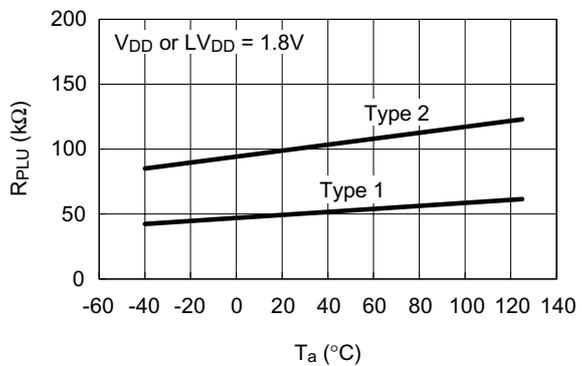


Figure 6-295 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

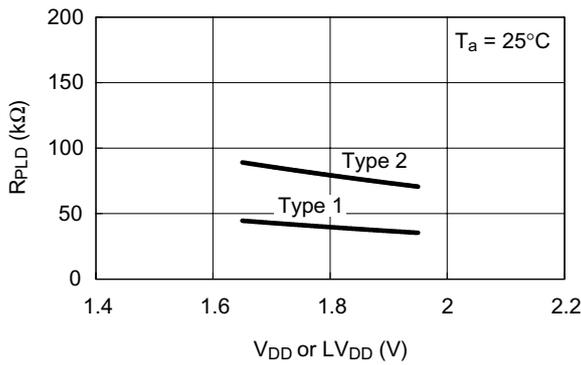


Figure 6-296 Pull-down Resistance (R_{PLD}) vs. V_{DD} (LV_{DD})

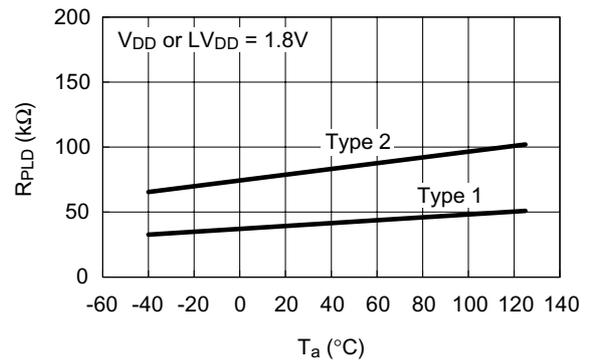


Figure 6-297 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

- 1.5 V ± 0.1 V

Pull-up Characteristics

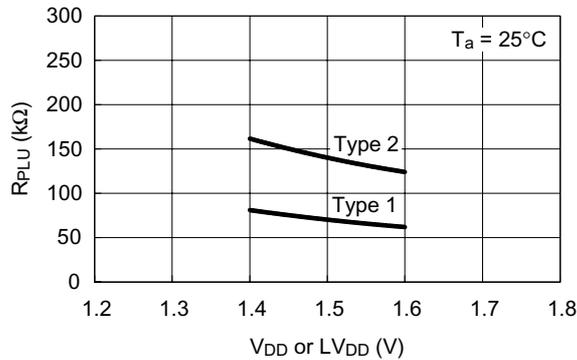


Figure 6-298 Pull-up Resistance (R_{PLU}) vs. V_{DD} (LV_{DD})

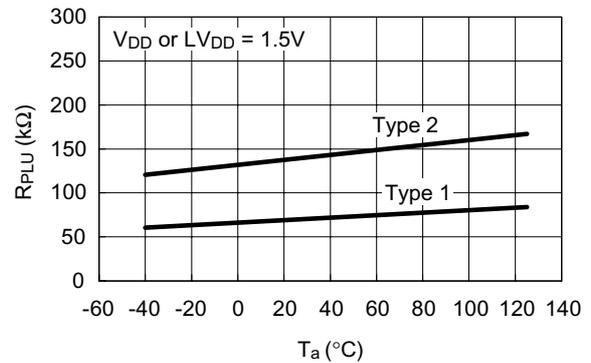


Figure 6-299 Pull-up Resistance (R_{PLU}) vs. Ambient Temperature (T_a)

Pull-down Characteristics

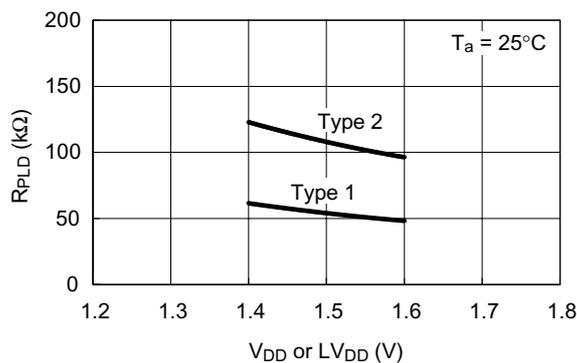


Figure 6-300 Pull-down Resistance (R_{PLD}) vs. V_{DD} (LV_{DD})

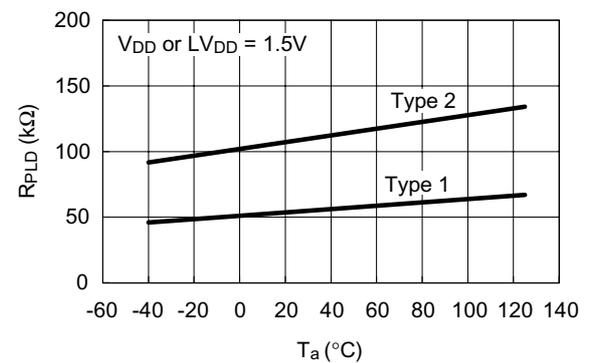


Figure 6-301 Pull-down Resistance (R_{PLD}) vs. Ambient Temperature (T_a)

(9) Output waveforms

- $2.5\text{ V} \pm 0.2\text{ V}$

Type 1

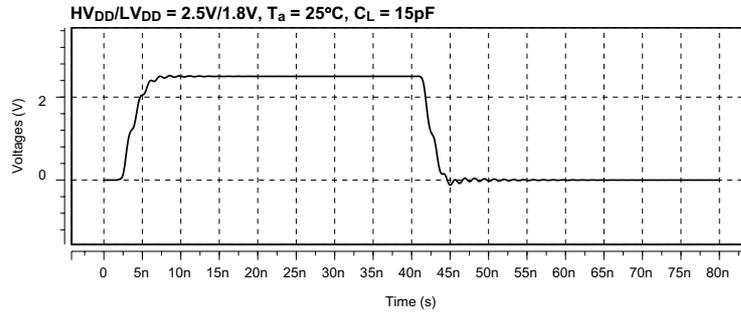


Figure 6-302 Output Waveform (HOB1AX)

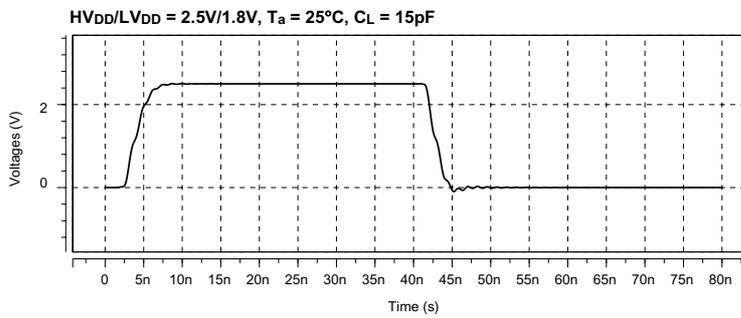


Figure 6-303 Output Waveform (HOB1BX)

Type 2

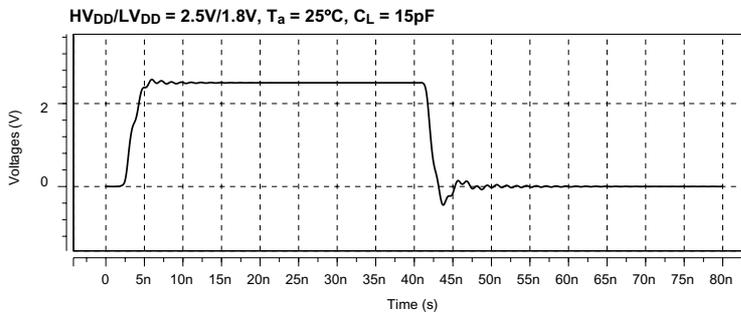


Figure 6-304 Output Waveform (HOB2AX)

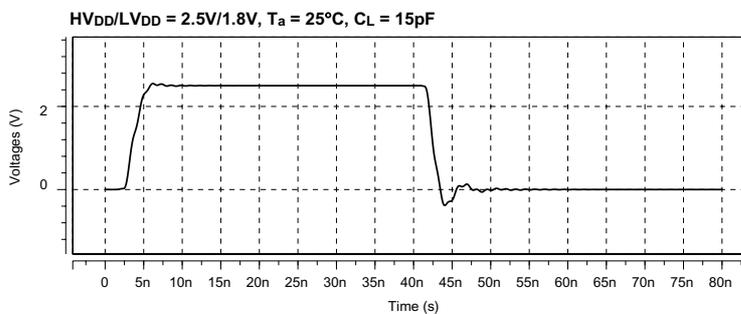


Figure 6-305 Output Waveform (HOB2BX)

Type 3

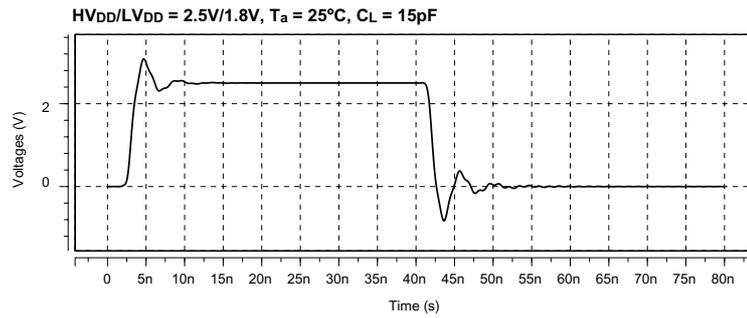


Figure 6-306 Output Waveform (HOB3AX)

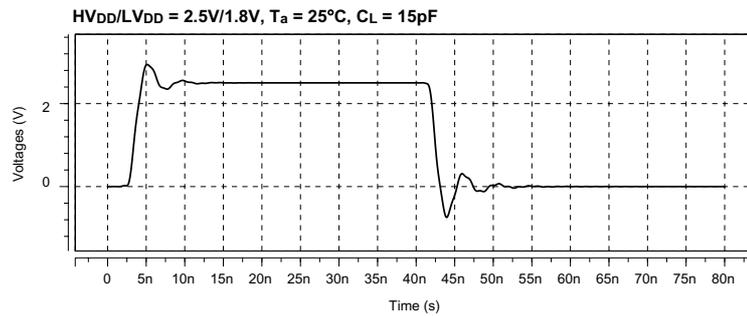


Figure 6-307 Output Waveform (HOB3BX)

Type 4

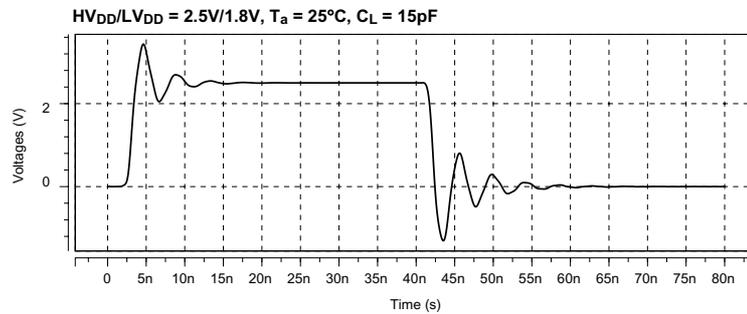


Figure 6-308 Output Waveform (HOB4AX)

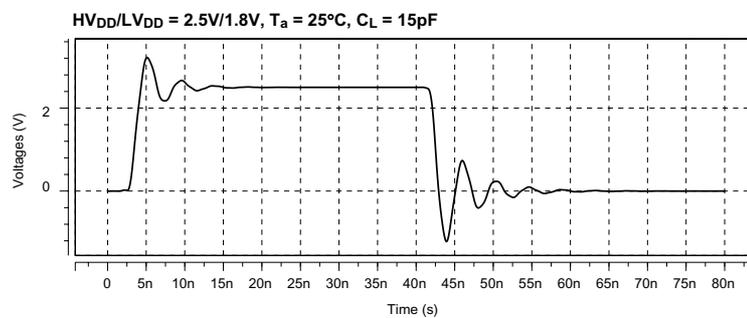


Figure 6-309 Output Waveform (HOB4BX)

- $1.8\text{ V} \pm 0.15\text{ V}$

Type 1

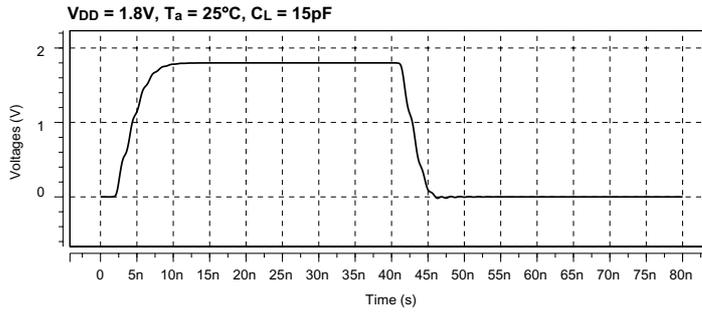


Figure 6-310 Output Waveform (MOB1AX)

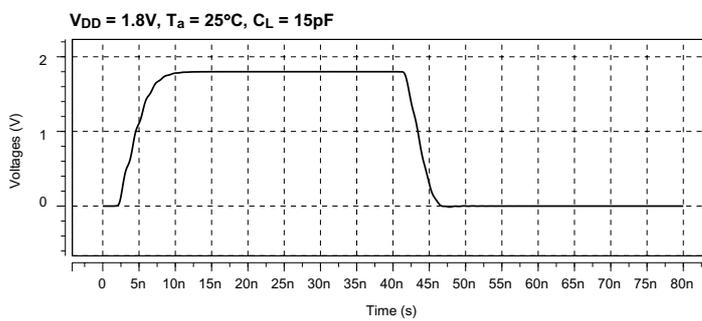


Figure 6-311 Output Waveform (MOB1BX)

Type 2

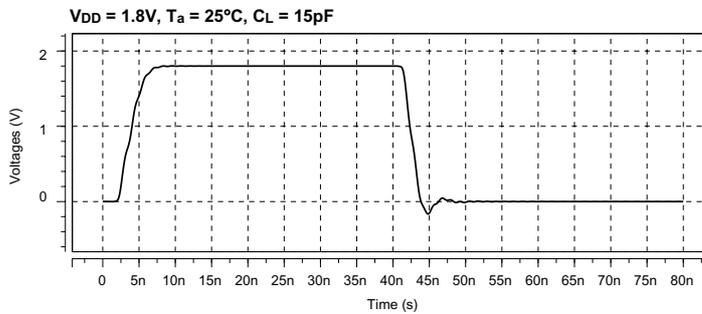


Figure 6-312 Output Waveform (MOB2AX)

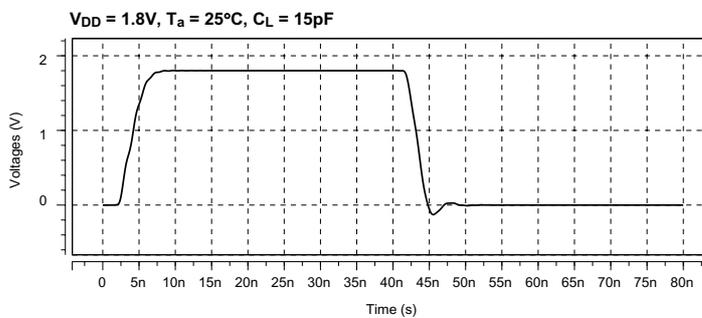


Figure 6-313 Output Waveform (MOB2BX)

Type 3

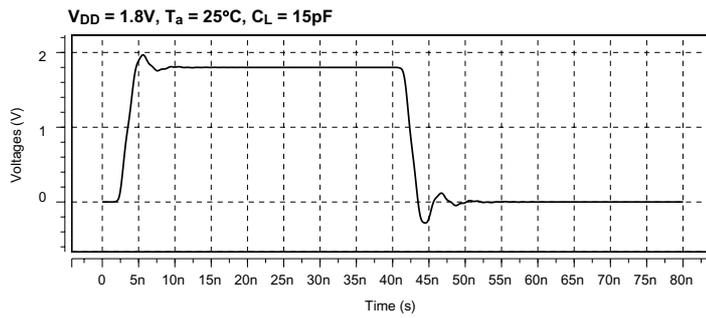


Figure 6-314 Output Waveform (MOB3AX)

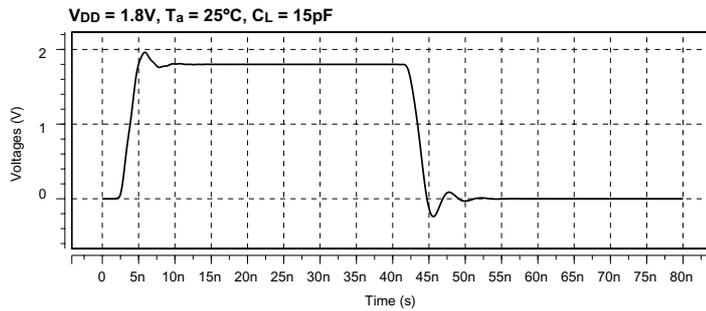


Figure 6-315 Output Waveform (MOB3BX)

Type 4

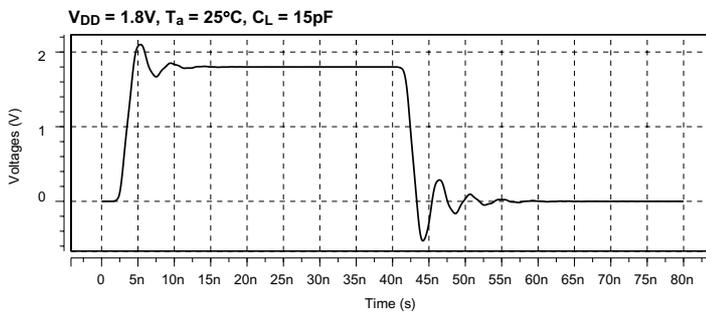


Figure 6-316 Output Waveform (MOB4AX)

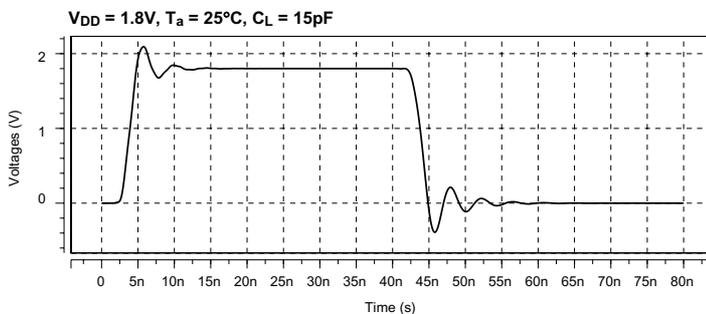


Figure 6-317 Output Waveform (MOB4BX)

- 1.5 V ± 0.1 V

Type 1

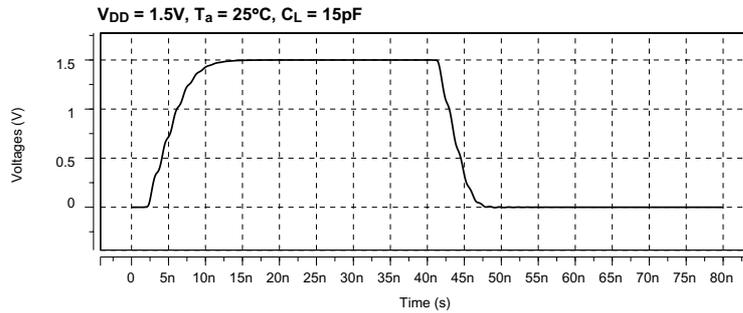


Figure 6-318 Output Waveform (MOB1AX)

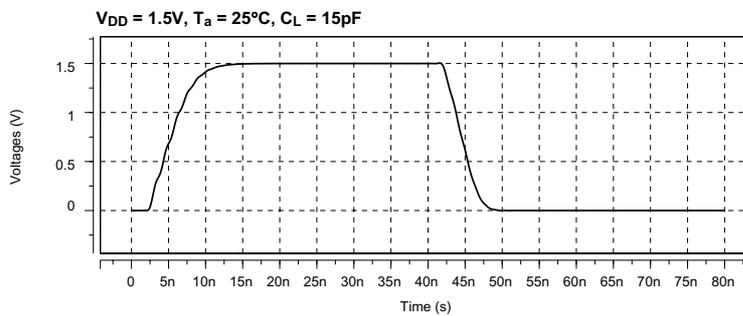


Figure 6-319 Output Waveform (MOB1BX)

Type 2

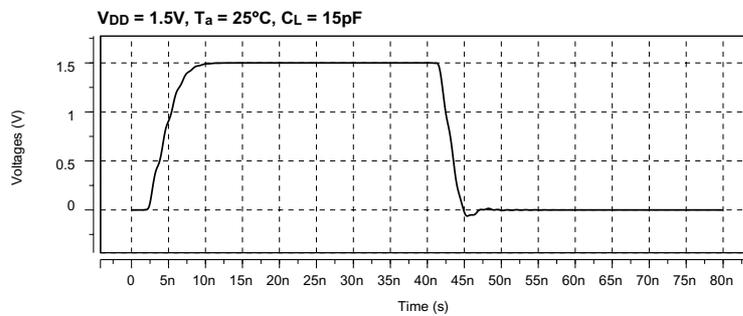


Figure 6-320 Output Waveform (MOB2AX)

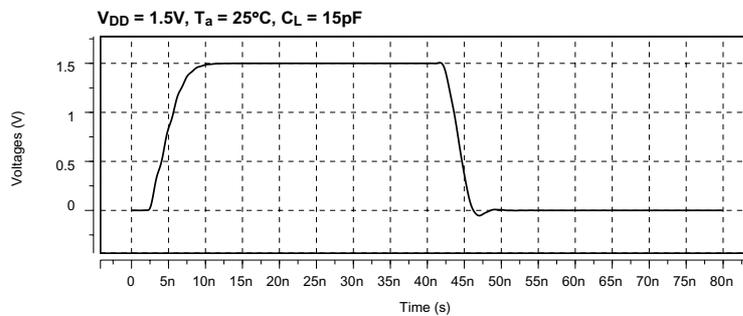


Figure 6-321 Output Waveform (MOB2BX)

Type 3

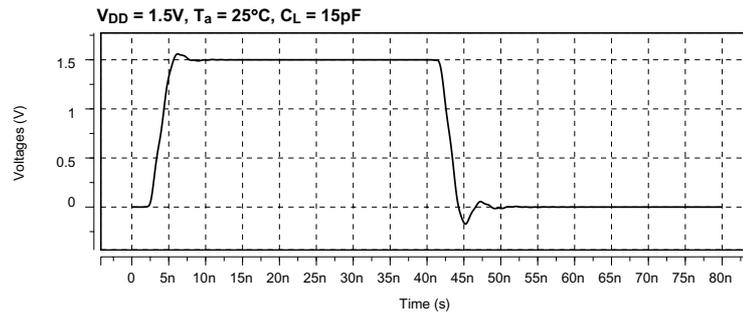


Figure 6-322 Output Waveform (MOB3AX)

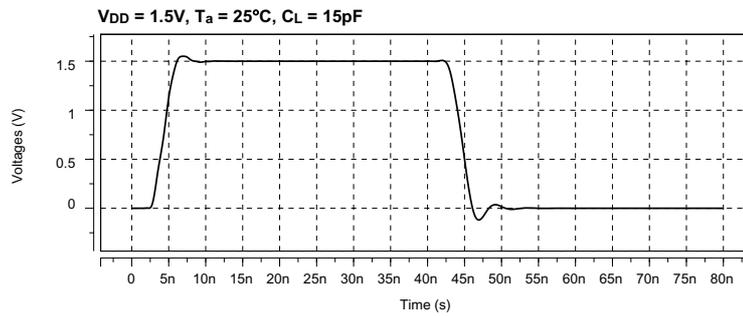


Figure 6-323 Output Waveform (MOB3BX)

Type 4

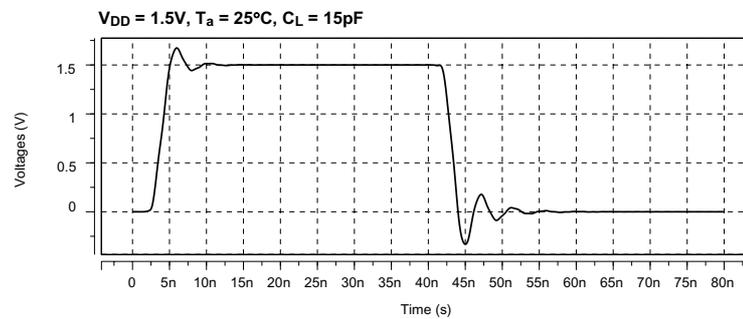


Figure 6-324 Output Waveform (MOB4AX)

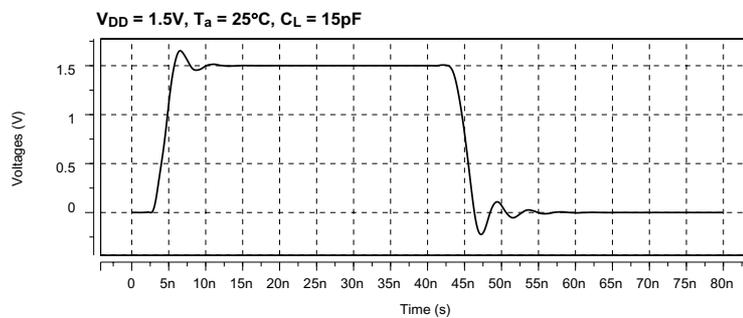


Figure 6-325 Output Waveform (MOB4BX)

Chapter 7 Circuit Design

7.1 Basic Circuit Configuration

7.1.1 Inserting Input/Output Buffers

Signals outside and inside an LSI can only be exchanged via input/output buffers. Always be sure to insert input or output buffers between the external pins and the internal cells of an LSI.

This is necessary because CMOS LSIs are extremely susceptible to static electricity, and the input/output buffers contain a circuit that protects them against static electricity.

7.1.2 Limitations on Logic Gate Output Load

CMOS circuits are such that, as the load capacitance of the output increases, so does the propagation delay time of signals (t_{pd}). At the same time, the rise and fall times of signal waveforms (t_{slew}) increase.

If logic gates have an excessively large output load capacitance, signal delay may concentrate at a specific circuit node, thereby limiting the operating speed or deteriorating the simulation accuracy of the logic gate's propagation delay time, which in turn could cause the logic gate to operate erratically. Furthermore, because the change period of signals is extended, the logic gate may become susceptible to noise.

To ensure that logic gates have an appropriate load in the circuit design stage, limitations known as "fan-out" limits are provided to limit the load that can be connected to the logic gate. The input pins of logic gates each have a specific input capacitance defined as the "fan-in," which is a relative quantity referenced to the input capacitance of inverter cell (IN1) = 1. On the other hand, fan-out limits are expressed as the sum total of fan-in counts, which can be connected to the output pin of each logic gate. In the design of your circuit, make sure the sum total of the fan-in counts connected to the output pin of each logic gate will not exceed the fan-out limits for that output pin. For logic gates such as clock lines that operate at high speed (operating frequency of 60 MHz or higher), make sure the load on their output pins is approximately half the ordinary fan-out limits.

The output-pin load capacitance of logic gates in an actual LSI consists of the input capacitance of gates in the next stage plus the wiring capacitance of signals. Because the exact wiring capacitance is determined through placement and routing in the circuit, a large load capacitance may be applied to specific nodes during placement and routing, depending on how the work is performed. The load condition at each circuit node can be verified from the output results of t_{slew} . If the output results suggest that the load condition exceeds the rated value, customers may be requested to correct the circuit in order to suppress the load to within the limits. To suppress increases in load capacitance after placement and routing work has been performed, minimize circuit branches at a single node or, if branching, use buffers with large fan-out.

7.1.3 Wired Logic Forbidden

Because the S1K70000-series cells use CMOS transistors, they cannot be configured with wired logic as in bipolar transistors. As a result, the output pins of cells cannot be connected together, as shown in Figure 7-1. Only in the bus circuit configuration is it possible to connect the output pins together.

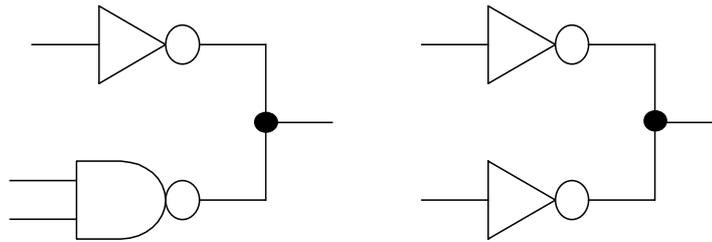


Figure 7-1 Examples Forbidden Wired Logic

7.1.4 Synchronized Design Recommended

For the logic circuit design, we recommend synchronized design in which all registers are basically clocked from a common timing signal source. Synchronized design provides numerous advantages. For example, it is suitable for high-speed circuits because register-to-register operations can easily be timed. It can make use of various EDA tools, such as Clock Tree Synthesis, DFT, and STA. In addition, because it does not depend on technology-inherent characteristics, circuits can easily be reused.

Ideally speaking, synchronized circuits have the following characteristics:

1. All registers in the circuit operate with either the rising or falling edge of a single clock signal.
2. No feedback loops are based on a combinational circuit (see Figure 7-2).
3. No pulse generator circuits that make use of a circuit delay are included (see Figure 7-3).
4. Other than the system reset, no asynchronous resets are used (this also applies to asynchronous sets).

Although in reality it may be difficult to design a circuit in which registers are clocked by a single clock signal, we recommend using as few clock signals as possible. The greater the number of clock signals used and the greater the complexity of the mutual relationships between them, the more time is required for circuit design, including the operation of said EDA tools, and the less likely it is to obtain satisfactory output results.

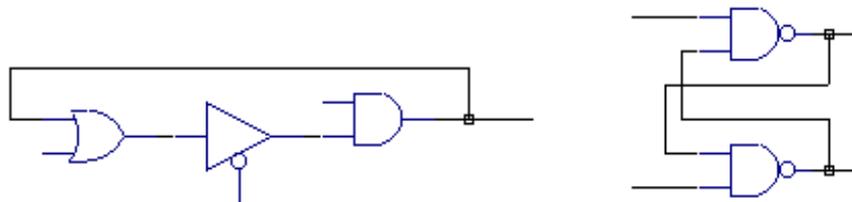


Figure 7-2 Example of a Feedback Loop

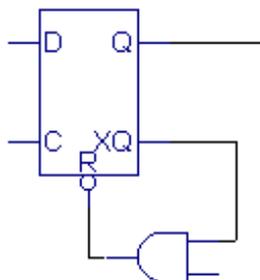


Figure 7-3 Example of a Delay-Based Pulse-Generator Circuit

7.2 Use of Differentiating Circuits Forbidden

The propagation delay time of each element in an LSI, t_{pd} , varies depending on the working environment (e.g., voltage and temperature) and manufacturing conditions. For this reason, care must be taken in the use of differentiating circuits that make use of the difference in relative t_{pd} times(see Figure 7-4), as a sufficient pulse width may not be obtained depending on the working environment and manufacturing conditions, causing the circuit to operate erratically.

When a differentiating circuit is needed, avoid using the circuit shown in Figure 7-4 and, instead, use a circuit built with FFs like the one shown in Figure 7-5.

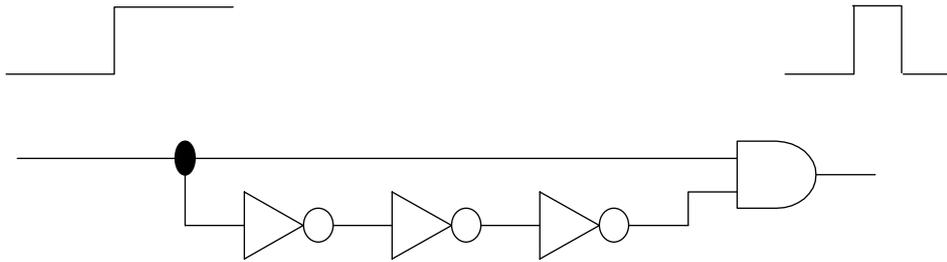


Figure 7-4 Example of a Bad Differentiating Circuit

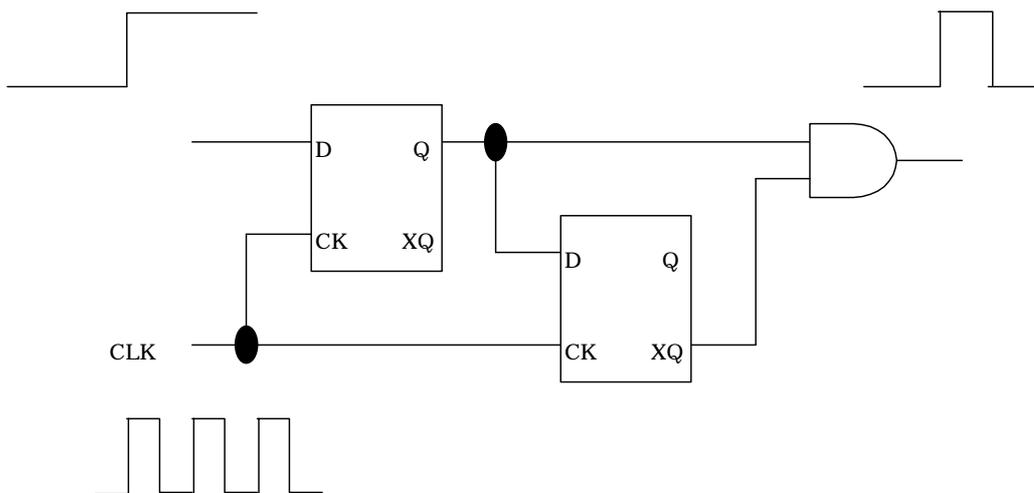


Figure 7-5 Example of a Differentiating Circuit Built with FFs

7.3 Clock Tree Synthesis

7.3.1 Overview

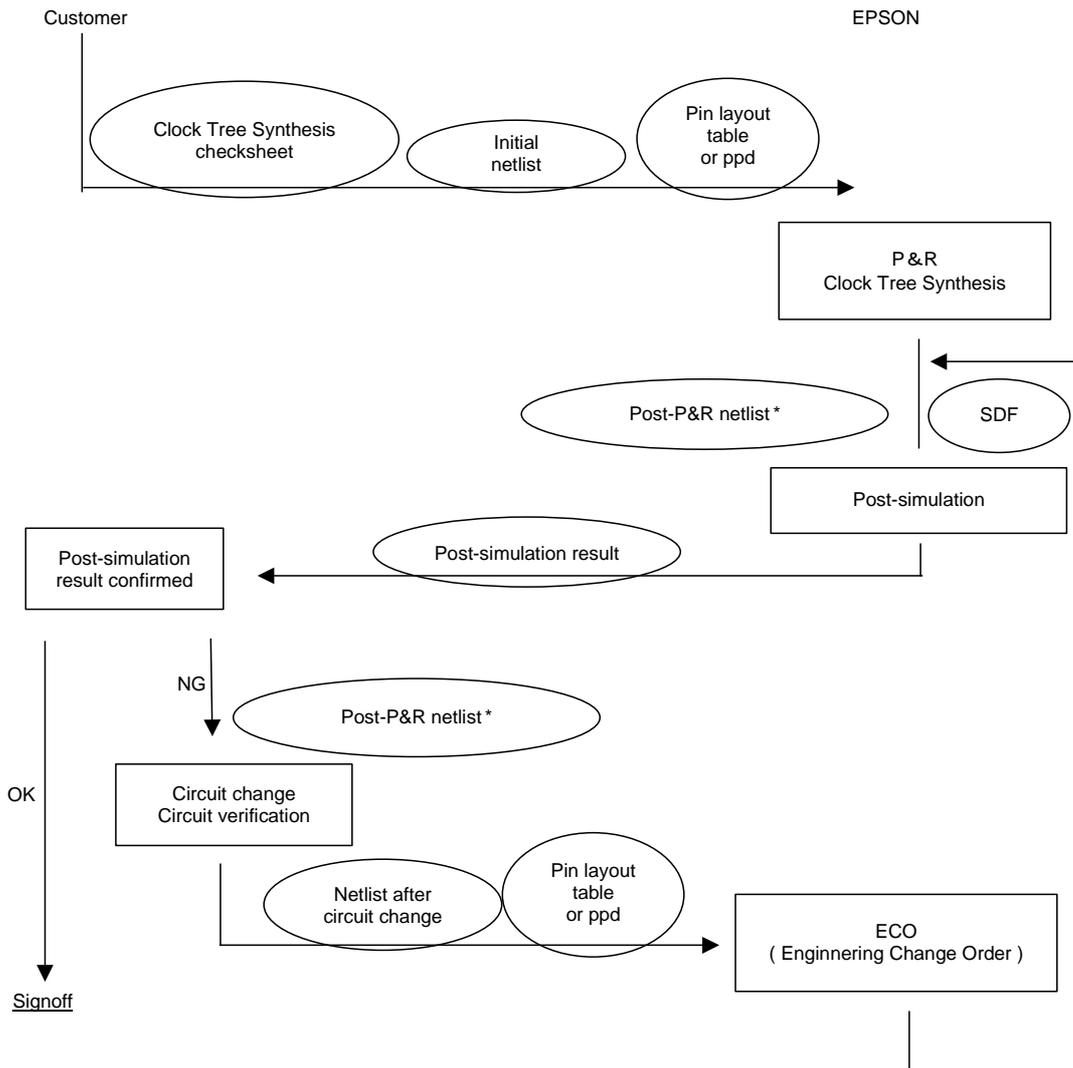
Clock Tree Synthesis is a service that allows a tree of buffers to be inserted automatically in order to optimize the skew and delay values of clock lines. When circuits are designed by customers, they often insert clock trees as a means of adjusting the fan-out of clock lines or for other purposes. In such a case, because clock trees are placed and routed so as to be suitable for the placement and routing tool, the clock skew and wiring delay tend to increase. Therefore, we recommend that buffers not be inserted in clock lines for fan-out adjustment purposes; instead, we recommend that you receive this service from Epson.

For circuits that also contain gated cells (simple gates) in clock lines, Clock Tree Synthesis helps optimize the skew and delay values of clock lines.

Before Clock Tree Synthesis can be applied, customers are requested to insert dedicated buffers or dedicated gated cells in clock lines for the following three purposes:

- (1) To determine the location at which Clock Tree Synthesis is applied
- (2) To perform temporary wiring-level simulation (pre-simulation) using the predicted delay values of clock trees to be inserted
- (3) To back-annotate after replacing the inserted clock trees with delay information, in order to perform precise post-simulation

7.3.2 Design Flow



(ECO is a method for performing placement and routing only in locations where the circuit has been changed.)

[Notes]

- The post-P&R netlist contains buffers that have been added in Clock Tree Synthesis.
- Post-simulation uses the netlist and sdf, which contain the buffers that have been added in Clock Tree Synthesis.
- If the result of post-simulation is No Good (NG), correct the post-P&R netlist. If the initial netlist has been corrected, P&R must be reexecuted.
- If circuit changes are made to the clock net part (dedicated buffer, dedicated gated cell, and DEF), P&R must basically be reexecuted. If it is necessary to change the clock net part, please consult with Epson.

7.3.3 Applying Clock Tree Synthesis

Refer to Table 7-2, “Dedicated Buffers,” for the selection of Clock Tree Synthesis-only buffers, and to Table 7-3, “Cell Names of Dedicated Gated Cells,” for the selection of Clock Tree Synthesis-only gated cells. In addition, after gaining an understanding of the Limitations and Notes in Section 7.3.4, refer to Reference Circuit Diagram 1 when inserting the dedicated buffers or dedicated gated cells that you’ve selected.

For logic-synthesis-based design, because the dedicated buffers and dedicated gated cells cannot be automatically inserted, use direct language descriptions. In such a case, to ensure that the clock line in which dedicated buffers or dedicated gated cells have been inserted will not have other buffers or the like synthesized in it, execute the following command in the Design Compiler:

```
set_dont_touch_net net_name
```

Table 7-1 Criteria for Appropriate Skew Values

Standard Fan-Out Counts	Without Gated Cells	With Gated Cells
0–500	±200ps	±300ps
500–3000	±250ps	±400ps
3000–10000	±300ps	±500ps
10000–	±350ps	±600ps

Notes:

- The criteria for appropriate skew values change according to the circuit size, wiring congestion, and number of clock lines.
- Make sure the number of gated cells inserted is not more than 20, and that the number of stages does not exceed three.
- The above criteria for appropriate skew values when gated cells are included apply to cases in which not more than 20 gated cells are inserted and there are not more than three stages.
- If more gated cells are inserted so as to exceed the limit of three stages, skew-derived timing errors may occur during post-simulation. To avoid delays in development schedules, try to minimize the number of gated cells used.

Table 7-2 Dedicated Buffers

S1K/S1X70000 Series			
Cell Name		T ₀ Max (ns)	Standard Fan-Out Counts
Sea of Gate	Cell Based		
L*CRBF2	K*CRBF2	2.00	0–500
L*CRBF3	K*CRBF3	3.00	500–3000
L*CRBF4	K*CRBF4	4.00	3000–10000
L*CRBF5	K*CRBF5	5.00	10000–
L*CRBF6	K*CRBF6	6.00	
L*CRBF7	K*CRBF7	7.00	
L*CRBF8	K*CRBF8	8.00	

An asterisk (*) represents a character that varies by type of transistor. See the table below.

Transistor Type	Standard 1	High-Performance	Low-Leakage	Standard 2
Character of *	1	2	3	4

Notes:

- The pre-simulation-time K value (delay values due to fan-out) for these cells is set to 0.
- The fan-out counts for these cells are set to infinite.
- The delay values relative to the fan-out counts fluctuate depending on the design size and usage efficiency. Therefore, use them for reference purposes only in the design of a circuit.

Table 7-3 Cell Names of Dedicated Gated Cells (Sea of Gate)

Circuit Configuration (Function)	Sea of Gate			
	Standard 1	High-Performance	Low-Leakage	Standard 2
AND	L1CAD2X4	L2CAD2X4	L3CAD2X4	L4CAD2X4
OR	L1COR2X4	L2COR2X4	L3COR2X4	L4COR2X4
2-1 Selector	L1CAO24AX4	L2CAO24AX4	L3CAO24AX4	L4CAO24AX4
NAND	L1CNA2X4	L2CNA2X4	L3CNA2X4	L4CNA2X4
NOR	L1CNO2X4	L2CNO2X4	L3CNO2X4	L4CNO2X4
2-1 Selector	L1CAN24AX1	L2CAN24AX1	L3CAN24AX1	L4CAN24AX1
INVERTER	L1CGINX4	L2CGINX4	L3CGINX4	L4CGINX4

Table 7-4 Cell Names of Dedicated Gated Cells (Cell-Based)

Circuit Configuration (Function)	Cell Based			
	Standard 1	High-Performance	Low-Leakage	Standard 2
AND	K1CAD2X4	K2CAD2X4	K3CAD2X4	K4CAD2X4
OR	K1COR2X4	K2COR2X4	K3COR2X4	K4COR2X4
2-1 Selector	K1CAO24AX4	K2CAO24AX4	K3CAO24AX4	K4CAO24AX4
NAND	K1CNA2X4	K2CNA2X4	K3CNA2X4	K4CNA2X4
NOR	K1CNO2X4	K2CNO2X4	K3CNO2X4	K4CNO2X4
2-1 Selector	K1CAN24AX1	K2CAN24AX1	K3CAN24AX1	K4CAN24AX1
INVERTER	K1CGINX4	K2CGINX4	K3CGINX4	K4CGINX4

Notes:

- The pre-simulation time delay value (T_0) for these cells is set to 0.
- The pre-simulation time K value (delay values due to fan-out) for these cells is set to 0.
- The fan-out counts for these cells are set to infinite.

7.3.4 Limitations and Notes

- When Clock Tree Synthesis is applied, the number of gates in the circuit for which it is applied increases by approximately 10% to 30%.
- If a large number of gated cells are inserted, skew-derived timing errors may occur during post-simulation. To avoid causing delays in development schedules, try to minimize the number of gated cells used.
- The dedicated buffers and dedicated gated cells can only be used in Clock Tree Synthesis, and cannot be used for any other purposes.
- Clock Tree Synthesis can also be used for data lines and control, or for other signal lines. However, applying Clock Tree Synthesis to a large number of nets results in an increase in the skew or delay. Therefore, make sure Clock Tree Synthesis is not applied to more than 10 nets, and that it is applied only to critical nets with large fan-out.
- If Clock Tree Synthesis is applied to nets with small fan-out, the delay or skew may increase. Make sure Clock Tree Synthesis is applied only to nets with a fan-out of several tens or more.
- If the clock line contains any cell other than the dedicated gated cells, skew may occur during pre-simulation. Therefore, make sure only the dedicated gated cells are inserted in the clock line.
- Always be sure to use the dedicated gated cells in combination with the dedicated buffers. Note that if only the dedicated gated cells are used inadvertently, the skew and delay values cannot be optimized.
- As the number of dedicated gated cells inserted in one clock net increases, so do the skew and delay values. Therefore, limit the number of dedicated gated cells inserted in one clock net to a maximum of 20.

- As the number of stages comprised of dedicated gated cells increases, so do the skew and delay values. Therefore, limit the number of stages comprised of dedicated gated cells to a maximum of three.
- Skew adjustment, by default, is applied to cells such as DFFs and latch cells that contain clock pins. If skew adjustment is required for other than DFFs and latch cells, i.e., cells without clock pins, please contact Epson.
- If the net for which Clock Tree Synthesis is used is connected to megacell input pins, skew adjustment is not applied beyond the megacell input pins.
- Do not insert the dedicated buffers in two or more stages. Note that if the clock net contains dedicated buffers, the skew and delay cannot be optimized.

7.3.5 Clock Tree Synthesis Checksheet

When applying Clock Tree Synthesis, customers are requested to provide Epson with the following information. Your cooperation is appreciated.

- Target Skew Value and Target Delay Value

Instance Name of CRBF*	Target Skew Value (Max.) (SIM condition: Max.)	Target Delay Value (Min./Max.) (SIM condition: Max.)

Notes:

- The target values are used for reference purposes only when they are applied to Clock Tree Synthesis, and cannot be guaranteed to be satisfied.

1. Is the number of clock lines within 10? Yes No
2. Does the clock net contain dedicated gated cells? Yes No

If you answered Yes to both of the above two questions, please answer questions 3 to 8 below.

3. Is the number of dedicated gated cells included in each clock net within 20? Yes No
4. Is the number of stages comprised of dedicated gated cells within 3? Yes No
5. Does the clock net contain dedicated buffers? Yes No
6. Does the clock net contain any cell other than the dedicated gated cells? Yes No

If Yes, write the cell name below.

[Notes]

- If 3-input ANDs are handled as special gated cells, for example, the 3-input ANDs in all clock lines are handled as special gated cells.
- DFFs and latches cannot be handled as special gated cells.

7. Do you want skew adjustment to be applied to other than DFFs and latches? Yes No
If Yes, specify the cell names and input-pin names.

Cell name:_____ Pin name:_____ Cell name:_____ Pin name:_____

[Notes]

If you specify inverters to be skew-adjusted, for example, the inverter cells in all clock lines are adjusted for skew.

8. Does any circuit configuration like Reference Circuit Diagram 2 included herein exist? Yes No

[Notes]

The clock net for both DFFs, one in part A and one in part B of the diagram, cannot be optimized for skew. If the DFFs in both parts A and B must be adjusted for skew, add dummy cells "L1CAO24AX4" as shown in Reference Circuit Diagram 2.

9. Does any circuit configuration like Reference Circuit Diagram 3 included herein exist? Yes No

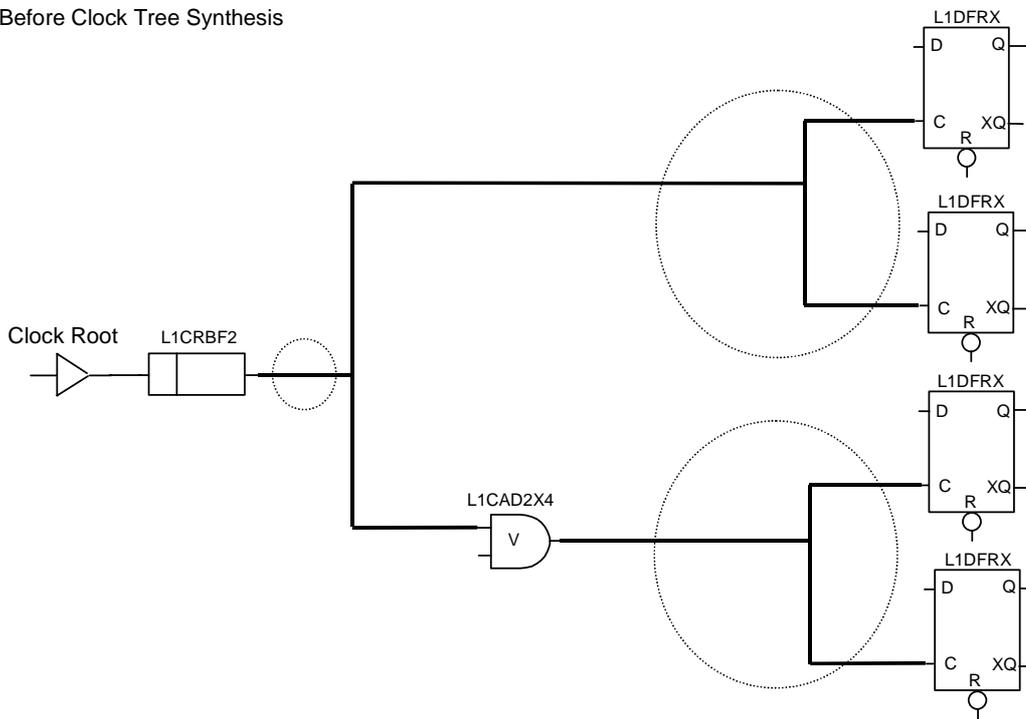
[Notes]

The DFF in part A of the diagram is driven from both clock roots A and B. The DFF in part A cannot be adjusted for skew in both clock roots A and B. The "CRBF" for clock root B in Reference Circuit Diagram 3 must be deleted.

7.3.6 Attached Materials

7.3.6.1 Concept of the Implementation of Clock Tree Synthesis

Before Clock Tree Synthesis



Clock Tree Synthesis optimizes the skew value for the thick-lined parts.

After Clock Tree Synthesis

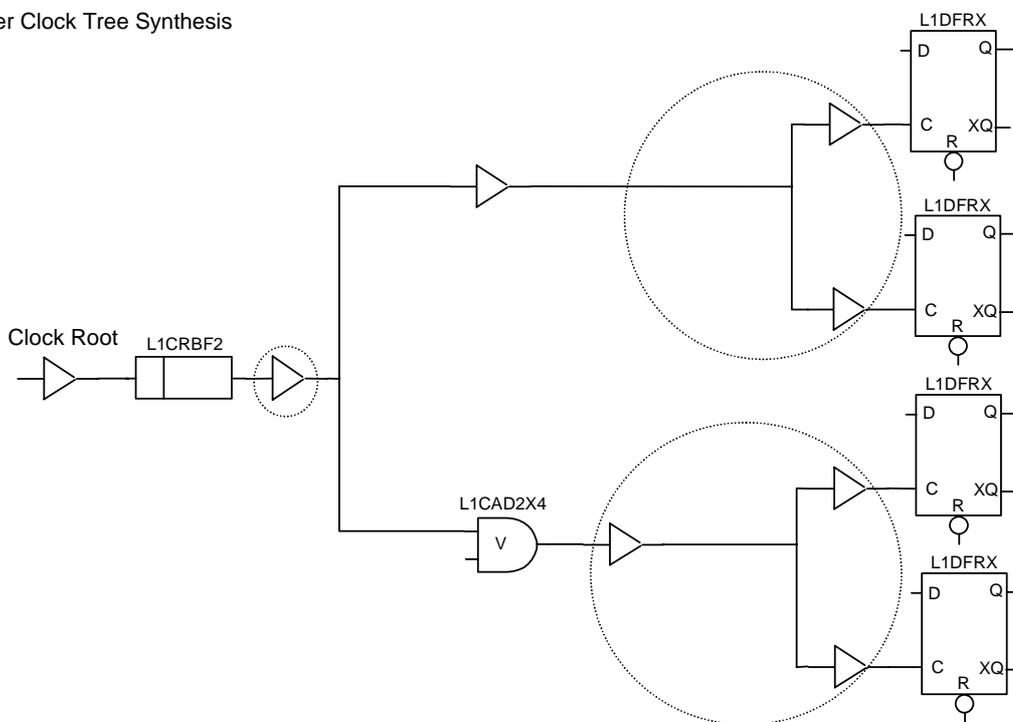
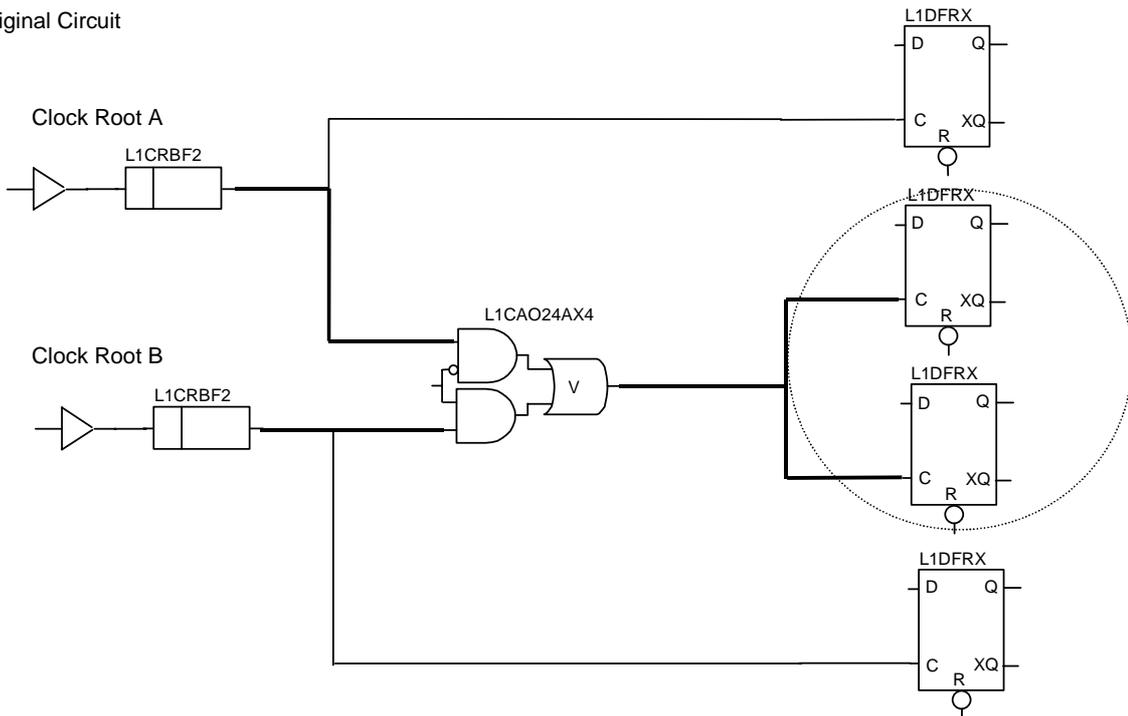


Figure 7-6 Reference Circuit Diagram 1

When Clock Tree Synthesis is applied, buffers are inserted within the dotted circles of the above circuit.

7.3.6.2 Example of Handling of a Problem Circuit-1

Original Circuit



Clock Tree Synthesis cannot be executed for the DFFs connected in the thick-lined part, as they are driven from both clock roots A and B.

Modified circuit

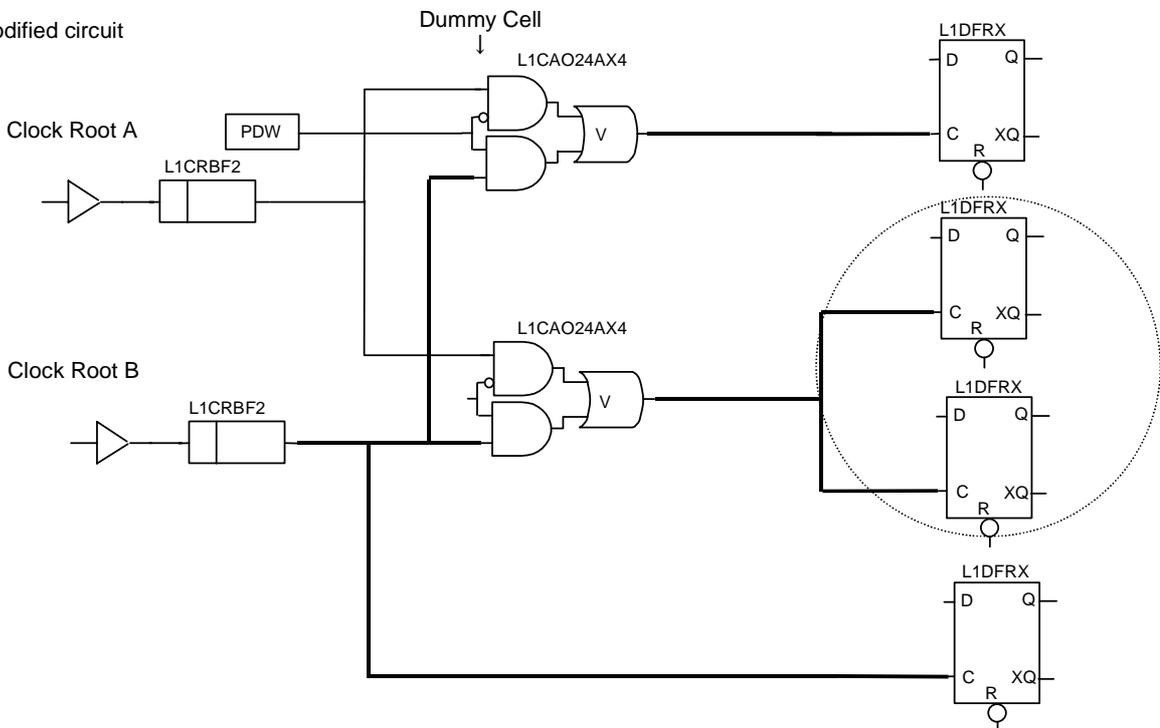


Figure 7-7 Reference Circuit Diagram 2

The DFFs within the dotted circle of the original circuit are driven from both clock roots A and B. Clock Tree Synthesis cannot be applied to any circuit in this manner. In the case of a circuit such as that in this example, insert a dummy cell “L1CAO24AX4,” as shown in the corrected circuit. In such a case, Clock Tree Synthesis optimizes the skew value of the thick-lined part of the circuit.

7.3.6.3 Example of Handling of a Problem Circuit–2

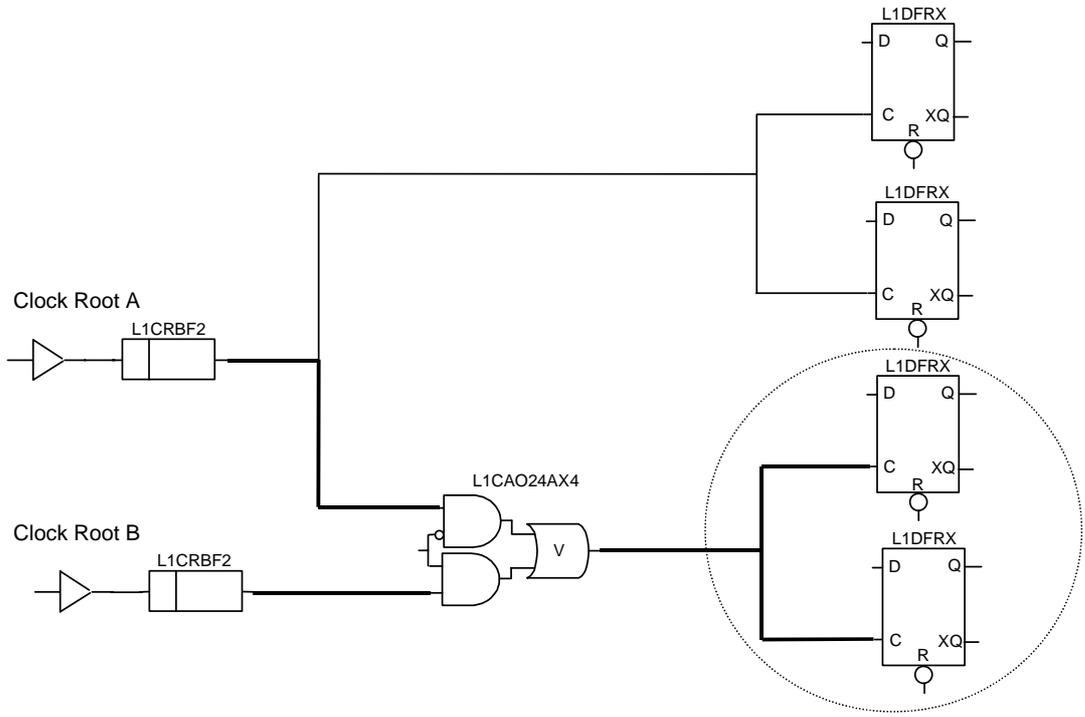


Figure 7-8 Reference Circuit Diagram 3

In the above circuit, the DFFs within the dotted circle are driven from both clock roots A and B. Clock Tree Synthesis cannot be applied to any circuit in this manner. In the case of a circuit such as that in this example, delete the cell “CRBF” that is inserted in clock root B.

7.3.6.4 Problem Circuit

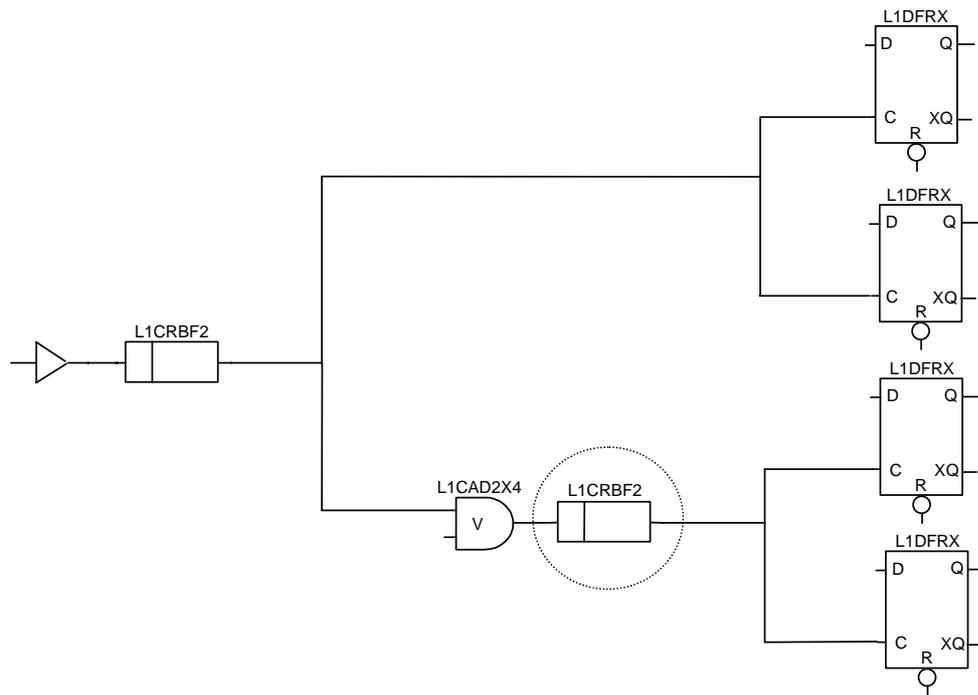


Figure 7-9 Reference Circuit Diagram 4

In the above circuit, the cell “L1CRBF” is inserted in the stage following that of the L1CAD2X4 cell, which comprises multiple dedicated-buffer stages. The L1CRBF cell in the stage following that of the L1CAD2X4 cell is unnecessary; therefore, it should be deleted.

7.4 Designing Fast-Operating Circuits

For fast-operating circuits (operating frequency of 60 MHz or more), due to the reduced per-cycle time, the operable delay time has a small margin with respect to the propagation delay time. Therefore, devise appropriate countermeasures to minimize propagation delays by taking the precautions described below into consideration in the design of a circuit.

<Countermeasures for minimizing propagation delay>

- Avoid using NOR gates to configure the circuit. Instead, use NAND gates.*1
- Do not use a number of multi-input logic elements unless absolutely necessary.*1
- For circuit parts with large branch counts, use tree structures that require few branches per drive element.*2 Reduce the branch counts to a maximum of 10 or less.
- For fast-operating logic elements (operating frequency of approximately 60 MHz), or for circuits with strict delay specifications, make sure the load on their output pins is approximately half or 1/3 of the ordinary fan-out limits in the design of a circuit.*2
- For logic elements connected at entry to separate modules or connected to macros and I/Os, select the high-drive type.*2
- Remove restrictions, as much as possible, from circuit parts with large timing margins. (Because optimization by synthesis tends to start from paths with strict timing constraints, the run time can be reduced by deleting unnecessary timing constraints as much as possible. If circuits that have small timing margins or are in violation of timing specification exist in your design, please consult Epson before conducting synthesis.)

Notes) *1: Because the drive capability differs between the High and Low logic levels, delay time in the circuit may be smaller when the circuit is configured with NAND gates than when it is configured with NOR gates. Similarly, delay time in the circuit can be reduced by eliminating the use of multi-input logic elements in the circuit.

*2: In the circuit layout of the actual LSI, the load capacitance not only consists of the input capacitance of the next-stage element, but also includes the wiring capacitance of signals. Because the exact wiring capacitance is determined by placement and routing in the circuit, a specific node may be subjected to large load capacitance as a result of placement and routing. To suppress increases in load capacitance following placement and routing work, reduce the number of circuit branches at a single node as much as possible.

7.5 Metastable State

If the input signals for flip-flops or latch cells are in violation of timing specifications (such as the clock and data setup and hold times, or the clock and set/reset release or removable times), the output signals of the flip-flops or latch cells may be oscillating or at an intermediate voltage level, neither High nor Low, for a certain period of time. The instable state of output signals as in this case is referred to as the “metastable” state.

The metastable state ends after the elapse of a certain length of time, and the output is fixed to the High or Low level. However, because this fixed output level does not depend on the level of the input data, the output is indeterminate.

If the setup/hold or release/removal timing specification cannot be met, be sure to incorporate corrective measures in circuit design in order to ensure that such an instable state will not propagate to the entire circuit.

For the S1K70000 series, the duration of the metastable time in cases in which the designated values of the setup/hold or release/removal times cannot be satisfied is defined as a standard value, as follows:

$$\text{Metastable time} = T_{pd} \times 6$$

where, T_{pd} : delay time from the active edge of the clock or set/reset signal for a flip-flop or latch cell, until its output changes.

Because delay values in such a metastable state are not taken into consideration during logic simulation, always make sure a circuit being designed satisfies the timing specification.

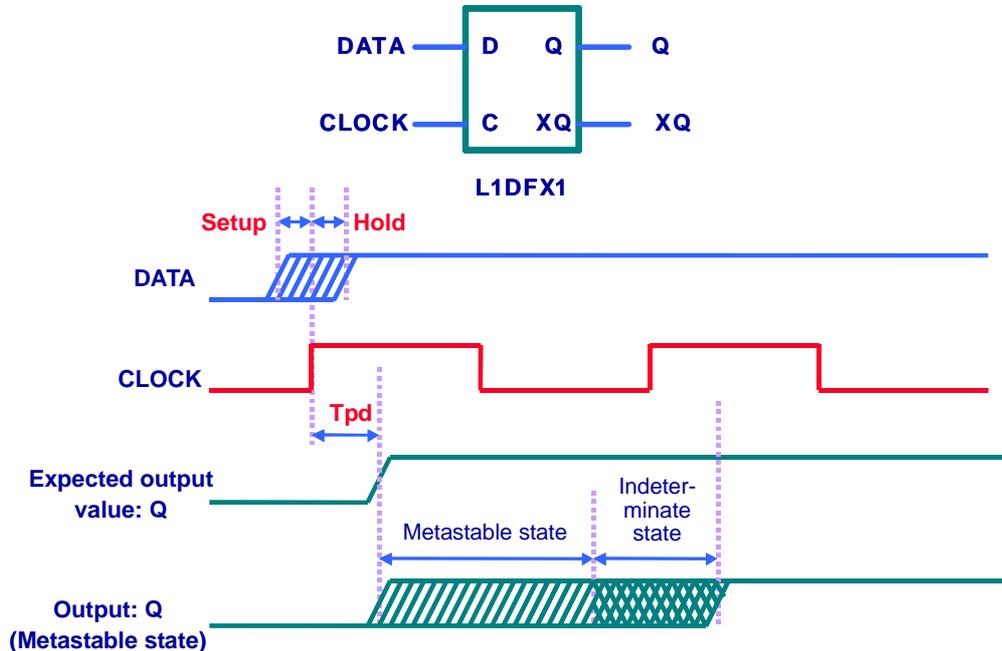


Figure 7-10

7.6 Configuration of the Internal Bus

The bus circuit is configured using 3-state logic circuits; therefore, one of the outputs connected to the bus is driven active (while the other output is placed in the high-impedance state) through manipulation of the control signals for the bus, allowing one transmission signal line to be time-shared.

The following describes the precautions to be taken when configuring an internal bus circuit using internal tri-state buffers.

- Bus cells can only be used in a bus circuit, and not in any other circuit (see Table 7-5 for the bus cells in the S1K70000 series).
- When configuring a bus circuit, add the bus latch cell *BLT.*
- Of the bus cells connected to one bus, only one output can be in an active state (logic 0 or 1), and all other bus-cell outputs must be placed in the high-impedance (Hi-Z) state.*1
- The number of bus cells that can be connected to one bus must be within the fan-out limits.*2
- The bus circuit tends to have a large propagation delay time due to fan-out, making it unsuitable for high-speed operation.*2
- The data retained by a bus latch cell can only be used to prevent the bus from floating, and cannot be used as a logic signal.*3
- When creating test patterns, exercise caution to ensure that the initial state of the bus can be determined easily.*4
- Make sure control signals for the bus change state only once within one cycle.

Notes) *1: If two or more of the bus cells connected to one bus are in an active state (logic 0 or 1) at the same time, the output voltage may not only become instable, but may also cause a steady current to flow between V_{DD} and GND. This limitation should always be taken into consideration.

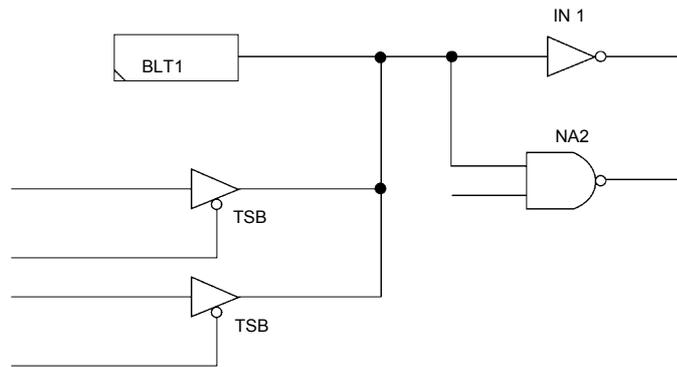
*2: If an excessively large load is placed on the internal bus, the signal rise and fall times increase due to the increased wiring length and increased number of driven cells. This may result in a difference between the delay time in logic simulation and the delay time in the actual device.

*3: Even though all of the bus cells connected to one bus enter a high-impedance (Hi-Z) state, data is retained by a bus latch cell. However, the latch's holding capability is restrained so as not to adversely affect operation. Do not use the retained output data as valid data.

*4: Configure the bus so as to improve its testability by, for example, adding test pins in order to increase the bus' controllability.

Table 7-5 Bus Cells Available in the S1K/S1X70000 Series

Cell Type	Cell Name		
	1BIT	4BIT	8BIT
Bus latches	*BLT1	*BLT4	*BLT8
Bus driver	*TSB*	—	—
Inverting bus driver	*TSV*	—	—

**Figure 7-11** Typical Configuration of a Bus Cell Circuit

7.7 Preventing Contention with External Buses

In a system built using gate arrays and other LSIs, if they are connected in a bus configuration, take appropriate measures, in addition to the precautions described in Section 7.6, "Configuration of the Internal Bus," by inserting pull-up/pull-down resistors, for example. To prevent external buses from floating, input/output cells with pull-up/pull-down resistors or input/output cells with a bus hold function (*) may be used.

Note that if appropriate measures are not taken prior to use, due to the indeterminate input level, functional failure or increased input leakage current may be encountered.

*: Bus hold circuit

Input/output buffers with a bus hold function are available in the S1K/S1X70000 series. To prevent the output pins or bi-directional pins from entering a high-impedance state, these buffers hold the data at the output pins intact.

However, because the bus hold circuit's holding capability is restrained so as not to adversely affect normal operation, do not use the retained output data as valid data. In the event any data is supplied from the outside, the retained data may change state easily.

For details on the bus hold circuit's output retention current, refer to the electrical characteristics specified in this manual.

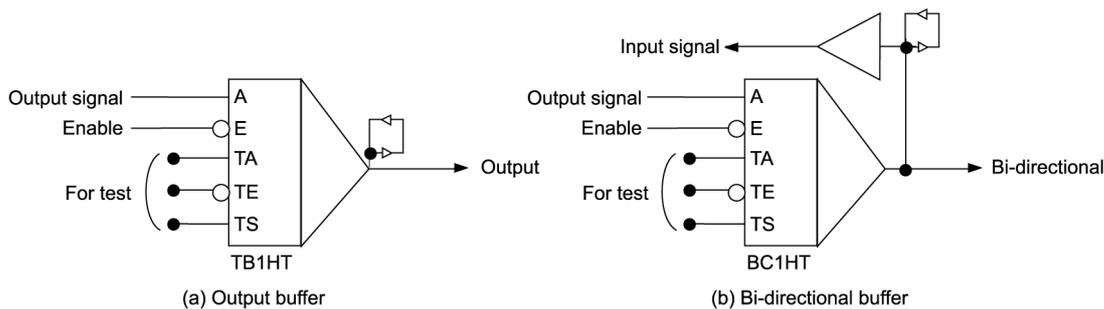


Figure 7-12 Example of a Bus-Hold-Circuit Symbol

7.8 Oscillation Circuits

7.8.1 Configuration of Oscillation Circuits

Two types of dedicated oscillation cells are used to configure an oscillation circuit: one for a crystal oscillation, and one for an CR oscillation. Furthermore, there are two types of cells for crystal-oscillation use, a steadily oscillating type and an intermittently oscillating type, and either type can be placed in an internal-cell area or an I/O-cell area. The oscillation circuit may be configured in various ways, depending on which type of oscillation cell is used, as shown below.

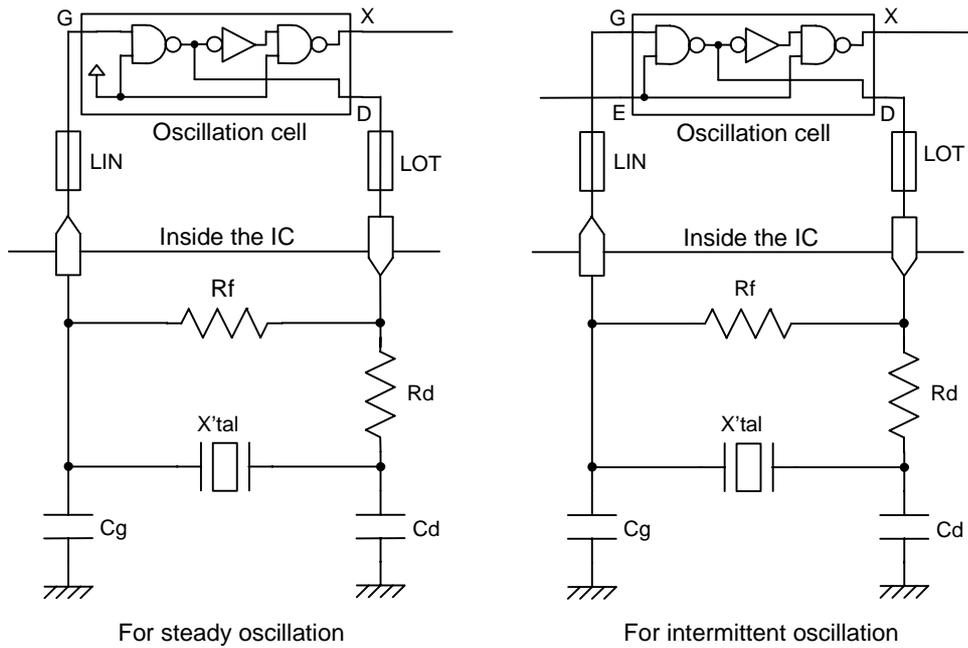


Figure 7-13 Crystal-Oscillation Circuit (Internal-Cell Type)

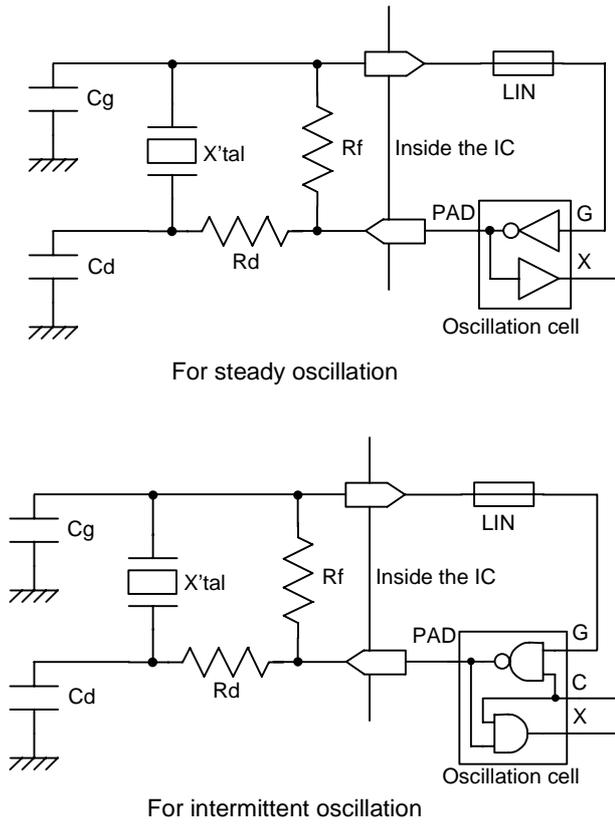


Figure 7-14 Crystal-Oscillation Circuit (I/O-Cell Type)

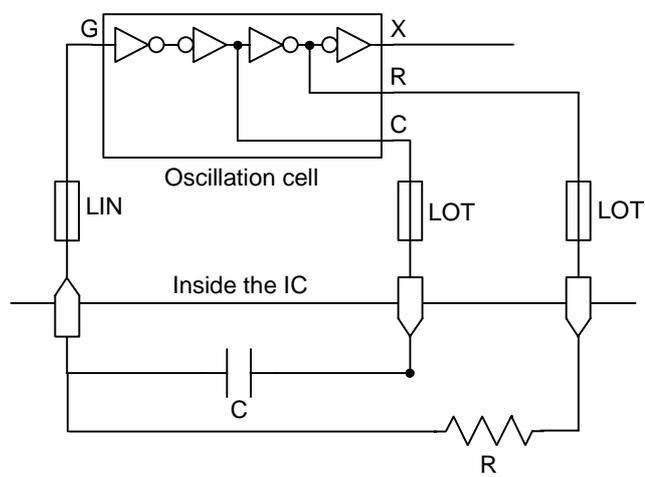


Figure 7-15 CR Oscillation Circuit

7.8.2 Notes Regarding the Use of Oscillation Circuits

(1) Pin layout

- The input/output pins of the oscillation circuit must be placed close to each other, and must be enclosed with the power-supply pins (V_{DD} , V_{SS}) at both ends.
- The input/output pins of the oscillation circuit must be placed away from other output pins. In particular, they must be separated from outputs that are in phase or are 180 degrees out of phase with the oscillation waveform. Make sure these outputs are placed on the other side of the package, opposite the oscillation circuit.
- The input/output pins of the oscillation circuit must be placed away from other input pins such as a clock input, which operate at high speed.
- The input/output pins of the oscillation circuit must be placed as close to the center of one edge of the package as possible.
- When incorporating two or more oscillation circuits in the design, make sure those oscillation circuits are placed apart from each other in order to prevent interference.
- When using area array packages such as BGA, consult the sales division of Epson for the pin layout of the package.

(2) Test pattern generation

For details on how to create test patterns for designs using an oscillation circuit, refer to Section 9.5, “Notes Regarding the Use of Oscillation Circuits,” in Chapter 9, “Test Pattern Generation.”

(3) Selecting oscillation cells

The oscillation frequencies available with the oscillation cells are in the range of several tens of kHz to tens of MHz. For more information, contact the sales division of Epson.

(4) Setting external resistor and capacitor values

The oscillation characteristics of an oscillation circuit depend on its constituent elements (IC, X'tal, Rf, Rd, Cg, Cd, and board). Therefore, before determining the values of external Rf, Rd, Cg, or Cd, sufficiently evaluate those components while they are mounted on the actual board. In this way, attempt to select the most appropriate values for those components.

(5) Guaranteed level

The oscillation characteristics of an oscillation circuit depend on its constituent elements (IC, X'tal, Rf, Rd, Cg, Cd, and board). Therefore, Epson cannot guarantee the oscillation performance and characteristics of oscillation circuits designed by customers. The oscillation characteristics of those oscillation circuits must be verified by customers themselves through sufficient evaluation using ES samples.

(6) Oscillation-circuit configuration in a dual-power-supply system

The oscillation circuit in a dual-power-supply system can basically be configured in the same way as a single-power-supply system. In this configuration, the oscillation cells are connected to the LV_{DD} power supply. For the input/output cells LIN and LOT used in this configuration, therefore, select those labeled “LLIN” and “LLOT,” i.e., those prefixed with “L.”

7.9 Hazard Protection

Circuits or decoder cells comprised of a combination of NAND and NOR gates tend to generate very short pulses, depending on the difference in propagation delays between those gates. These short pulses are known as a “hazard.” If such a hazard enters the clock or reset pins of an FF (flip-flop), it causes the FF to operate erratically.

For circuits in which such a hazard is likely to occur, therefore, protective measures must be taken by, for example, devising a circuit configuration that prevents the hazard from propagating or using a decoder circuit provided with an “Enable” pin.

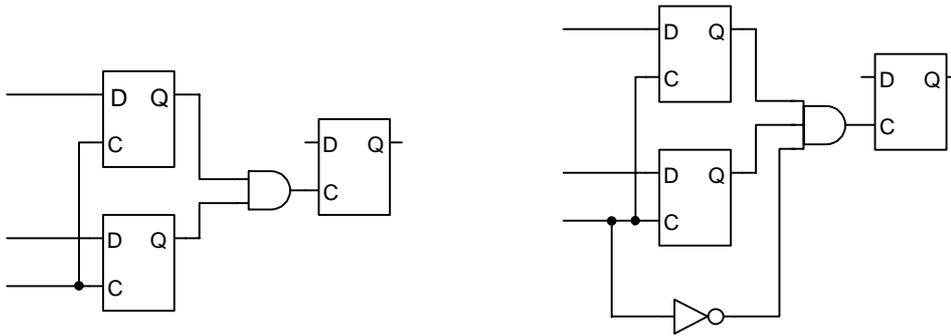


Figure 7-16 Example of Hazard Protection

7.10 Restrictions and Constraints on VHDL/Verilog-HDL Netlist

The VHDL/Verilog-HDL netlist to be interfaced to Epson shall be a pure gate-level netlist (not containing function and description of operation). The restrictions and constraints in developing Epson ASIC using VHDL/Verilog-XL are as follows.

7.10.1 Common Restrictions and Constraints

(1) Names of external pin (I/O pin)

- Use only upper-case letters.
- Number of characters: 2 to 32
- Bus description is prohibited.
- Usable characters: Alphanumeric characters and “_.” Use an alphabetical letter at the head.
- Examples of prohibited character strings:
 - 2 INPUT: A digit is at the head.
 - \2INPUT: “\” is at the head.
 - InputA: Lower-case letters are included.
 - _INPUTA: “_” is at the head.
 - TNA[3:0]: A bus is used for the name of the external pin.
 - INA[3]: A bus is used for the name of the external pin.

(2) Names of internal pin (including bus net names)

Upper-and lower-case letters can be used in combination, except the following.

Combinations of the same words expressed in upper-and lower-case letters, such as “_RESET_” and “_Reset_.”

- Number of characters: 2 to 32
- Usable characters: Alphanumeric characters, “_”, “[_]” (Verilog bus blanket), and “_()_” (VHDL bus blanket) with an alphabetical letter at the head.

(3) Module names

In systems, module names are discriminated between the uppercase and lowercase. In design rules, however, mixed use of uppercase and lowercase module names is prohibited.

Example: Mixed use of “AND” and “And”

Because cells are case-sensitive, be careful about upper- and lowercase when you enter module names.

(4) Bus description is prohibited at the most significant place of the module.

Examples:

DATA [0:3], DATA [3], and DATA [2] are prohibited.

DATA0, DATA1, and DATA2 are all allowed.

- (5) You can use I/O cells of the same library series, but cannot combine those of different series.
- (6) It is not possible to describe operations in behaviors, in RTL, or in the C language. Such descriptions existing in the netlist are invalid.
- (7) Precision of the time scale of the library of each series is 1ps.

7.10.2 Restrictions and Constraints for Verilog Netlist

- (1) Descriptions using the functions “assign” and “tran” are prohibited in the gate-level Verilog netlist.
- (2) Descriptions of connection with cell pin names are recommended in the Verilog netlist.

Examples:

Possible: IN2 inst_1 (.A(inst_2),.X(inst_3))

Not Possible: IN2 inst_1(net1, net2)

- (3) You cannot use the Verilog command “force” as a description of flip-flop operation.

Example: force logic .singal = 0

- (4) The time scale description is added at the head of the gate-level netlist generated by the Synopsys design compiler. Set it at the value described in the Epsos Verilog library. Time scale of each series is 1ps.

Example: ‘timescale 1ps/1ps

- (5) Epsos prohibits combination of a bus single port name and a name that includes “_ _”, such as the following, in the same module.

```
input A [0]
```

```
wire \A [0]
```

- (6) The following letter strings are reserved for Verilog, which cannot be used as a user-defined name.

always	and	assign	begin	buf	bufif0
bufif1	case	design	default	defparam	disable
else	end	endcase	endfunction	endmodule	endtask
event	for	force	forever	fork	function
highz0	highz1	if	initial	inout	input
integer	join	large	medium	module	nand
negedge	nor	not	notif0	notif1	or
output	parameter	posedge	pull0	pull1	reg
release	repeat	scalared	small	specify	strong0
strong1	supply0	supply1	task	time	tri
tri0	tri1	trinand	trior	trireg	vectored
wait	wand	weak0	weak1	while	wire
wor	xor	xnor			

7.10.3 Restrictions and Constraints on VHDL Netlist

- (1) In addition to the constraints in 7.10.1 (1), the following letter strings are also prohibited. Because the simulation is performed using TEXTIO package, the name of functions used in TEXTIO package cannot be defined for users.

INPUTA_: “_” is used at the end.

INPUT_ _A: “_” is used twice or more in succession.

read: Used in the system.

write: Used in the system.

- (2) The following letter strings are reserved for VHDL, which cannot be used as a user-defined name.

abs	access	after	alias	all
and	architecture	array	assert	attribute
begin	block	body	buffer	bus
case	component	configuration	constant	disconnect
downto	else	elsif	end	entity
exit	file	for	function	generate
generic	guarded	if	in	inout
is	label	library	linkage	loop
map	mod	nand	new	next
nor	not	null	of	on
open	or	others	out	package
port	procedure	process	range	record
register	rem	report	return	select
severity	signal	subtype	then	to
transport	type	units	until	use
variable	wait	when	while	with
xor				

- (3) To use Epson utilities and tools, it is necessary to change the VHDL format into the Verilog format. Therefore, the letter strings reserved for Verilog in 7.10.2 (5) are also prohibited.

7.10.4 Description of Oscillation Cell and AC/DC Test Circuit Cell L1TCIR2

It is recommended that oscillation cells be described after being turned into instances, and that the dont_touch attribute be attached to the input and output nets by using the set_dont_touch command, in order to ensure that no buffers are inserted into the oscillation cells' external-pin connecting nets when synthesized.

As AC/DC test circuit cell L1TCIR2 are available as hard macros, it is recommended that they be entered in the form of gate descriptions, as shown in the examples below.

– Example of Verilog HDL description –

```
L1OSC1 inst1 (.G(gate_in), .D(drain_out), .X(clk_out) );
```

```
L1TCIR2 inst2 (.TM0(i_net0), .TM1(i_net1), .TM2(i_net2), .TM3(i_net3),  
              .TST(i_net4), .MS(MS), .TD(TD), .TE(TE), .TS(TS), .TAC(TAC) );
```

– Example of VHDL description –

```
inst1 : L1OSC1 port map (G => gate_in, D => drain_out, X => clk_out);
inst2 : L1TCIR2 port map (TM0 => i_net0, TM1 => i_net1, TM2 => i_net2,
                        TM3 => i_net3, TST => i_net4,
                        MS => MS, TD => TD, TE => TE, TS => TS, TAC => TAC );
```

7.10.5 Clock Buffer Description

When performing hierarchical design, please make sure that the clock root buffers are inserted in the upper layers (to the extent possible), so that gated cells will not have multiple linked stages.

For clock root buffers and gated cells, it is recommended that gated cells be written directly in RTL description.

When using Epson gate libraries in RTL simulation, please make sure a sufficient input delay is allowed in the test patterns you create, as there will be some delay in the clock root buffers.

– Verilog description –

```
module TOP (CLK, RESET, ....., );
  input CLK, RESET, ... ;
  output OUT1, OUT2, ... ;

  LIBCY pad1 (.PAD(CLK), .X(iCLK) );
  L1CRBF2 U0_L1CRBF2 (.A(iCLK), .X(wCLK) );
  .
  .

  CLKGEN U_CLKGEN (.CLK(wCLK), .ACLK(ACLK), .BCLK(BCLK) ...);
  AIF U_AIF (.ACLK(ACLK), .....,);
  BIF U_BIF (.BCLK(BCLK), .....,);

endmodule

module CLKGEN (CLK, ACLK, BCLK);
  input CLK;
  output ACLK, BCLK ;

  L1CAD2X4 GATEDCLKAND0 (.A1(CLK), .A2(A_gate),.X(ACLK) );
  L1CAD2X4 GATEDCLKAND1 (.A1(CLK), .A2(B_gate),.X(BCLK) );

  ...

endmodule
```

```

-- VHDL description --
library IEEE;
library s1k70000_typ;

use IEEE.std_logic_1164.all
use s1k70000_typ.primitives_tables.all;
use s1k70000_typ.mos_switches.all;

entity TOP is
  port ( CLK      ; in std_logic ;
        RESET ; in std_logic ;
        ...
        );
end TOP;
architecture RTL of TOP is

  component LIBCY
    port (PAD : in std_logic; X: out std_logic);
  end component;
  component L1CRBF2
    port (A : in std_logic; X: out std_logic);
  component CLKGEN
    port ( CLK, ACLK, BCLK : in std_logic; ... );
  end component;
  component AIF
    port (... );
  end component;
  signal
    wCLK, .....;

  begin

  PAD1 : LIBCY port map ( PAD => CLK, X => iCLK );
  PAD2 :
  U_CLKGEN : CLKGEN port map ( CLK => wCLK, ACLK => ACLK, ... );
  U_AIF : AIF port map ( ACLK => ACLK, ... );

end RTL;

```

7.11 Pin Layout and Simultaneous Operation

This section describes the points to be noted in the layout of pins and the procedure for adding power supplies for simultaneous output-buffer operation.

7.11.1 Estimating the Number of Power-Supply Pins

The necessary number of power-supply pins must be estimated according to the LSI's power consumption and the number of output buffers. In particular, a rather large transient current flows through the output buffers when they switch on or off. The amount of this transient current is greater for output buffers with greater drive capability.

The number of power-supply pins required for an LSI may be estimated with respect to its current consumption, as described below.

(1) For single-power-supply systems

Letting the current consumption be I_{DD} [mA], the number of power-supply pins may be estimated with respect to this current consumption as follows:

$N_{IDD} \geq I_{DD} / 30$ (pairs): With the V_{DD} and V_{SS} pins counted as one pair, 30 mA per pair can be supplied.

Note 1: There must be at least four pairs of power-supply pins, that is, one pair on each side of the LSI. I_{DD} represents a value equal to the power consumption obtained in Chapter 6, Section 6.1, "Calculation of Power Consumption," divided by the operating voltage.

2: If output buffers have DC loads connected to them with current steadily flowing, power-supply pins must be added. For more information, contact the sales division of Epson.

(2) For dual-power-supply systems

Even for dual-power-supply systems, the allowable amount of current that can be flowed per pair of power-supply pins (both HV_{DD} and LV_{DD} power supplies) is the same as that for single-power-supply systems. Calculate the necessary number of power-supply-pin pairs separately for the HV_{DD} and LV_{DD} power supplies.

(1) Number of HV_{DD} power-supply pins

Letting the current consumption in the HV_{DD} power-supply system be I_{DD} (HV_{DD}) [mA], the number of power-supply pins, N_{IDD} (HV_{DD}), may be calculated with respect to this current consumption as follows:

$N_{IDD} (HV_{DD}) \geq I_{DD} (HV_{DD}) / 30$: 30 mA per pin can be supplied

(2) Number of LV_{DD} power-supply pins

Letting the current consumption in the LV_{DD} power-supply system be I_{DD} (LV_{DD}) [mA], the number of power-supply pins, N_{IDD} (LV_{DD}), may be calculated with respect to this current consumption as follows:

$N_{IDD} (LV_{DD}) \geq I_{DD} (LV_{DD}) / 30$: 30 mA per pin can be supplied

(3) Number of V_{SS} power-supply pins

$N_{IDD} (V_{SS}) \geq \{I_{DD} (HV_{DD}) + I_{DD} (LV_{DD})\} / 30$: 30 mA per pin can be supplied

Note 1: For the power-supply pins HV_{DD} , LV_{DD} , and V_{SS} , there must be at least four pairs of power-supply pins, that is, one pair on each side of the LSI.

I_{DD} represents a value equal to the power consumption obtained in Chapter 6, Section 6.1, "Calculation of Power Consumption," divided by the operating voltage.

2: If output buffers have DC loads connected to them with current steadily flowing, power-supply pins must be added. For more information, contact the sales division of Epson.

3: If it is necessary to add a power supply due to simultaneous changes in output, add the HV_{DD} , LV_{DD} , and V_{SS} pins for each power-supply system, separately for the HV_{DD} output buffers and the LV_{DD} output buffers.

Calculation example: The following shows an example of the procedure for estimating the number of power-supply pins.

Here, the number of power-supply pins is estimated using the power consumption obtained in Chapter 6 for an IC, which has the following power-supply characteristics.

- Power-supply voltage: $HV_{DD}/LV_{DD} = 3.3\text{ V}/1.8\text{ V}$
- Power consumption: $P(HV_{DD}) = 224\text{ [mW]}$
 $P(LV_{DD}) = 684\text{ [mW]}$

(1) Estimating the number of HV_{DD} power-supply pins

Letting the number of HV_{DD} power-supply pins be $N_{IDD}(HV_{DD})$, then

$$\begin{aligned} N_{IDD}(HV_{DD}) &= 224\text{ [mW]} / 3.3\text{ [V]} / 30\text{ [mA]} \\ &= 2.26\text{ [pins]} \end{aligned}$$

Because there must be at least one power-supply pin on each side of the IC, the number of HV_{DD} power-supply pins to be inserted is 4.

(2) Estimating the number of LV_{DD} power-supply pins

Letting the number of LV_{DD} power-supply pins be $N_{IDD}(LV_{DD})$, then

$$\begin{aligned} N_{IDD}(LV_{DD}) &= 684\text{ [mW]} / 1.8\text{ [V]} / 30\text{ [mA]} \\ &= 12.67\text{ [pins]} \end{aligned}$$

Therefore, the number of LV_{DD} power-supply pins to be inserted is 13.

(3) Estimating the number of V_{SS} power-supply pins

Letting the number of V_{SS} power-supply pins be $N_{IDD}(V_{SS})$, then

$$\begin{aligned} N_{IDD}(V_{SS}) &= \{224\text{ [mW]} / 3.3\text{ [V]} + 684\text{ [mW]} / 1.8\text{ [V]}\} / 30\text{ [mA]} \\ &= 14.93\text{ [pins]} \end{aligned}$$

Therefore, the number of V_{SS} power-supply pins to be inserted is 15 (however, we recommend that V_{SS} pins be placed in pairs with the HV_{DD} and LV_{DD} power-supply pins).

Thus, the respective numbers of power-supply pins are as follows.

HV_{DD} power-supply pins : 4
 LV_{DD} power-supply pins : 13
 V_{SS} power-supply pins : 15

7.11.2 Simultaneous Operation and Adding Power Supplies

The noise generated by output buffers when they switch on or off simultaneously may cause the LSI to operate erratically. This section describes the simultaneous operation of output buffers and the points to be noted when placing pins in order to suppress the noise induced by simultaneous output operation.

7.11.2.1 Malfunction due to Simultaneous Operation

When a number of output buffers change state simultaneously, a transient charging and discharging of current occurs due to load capacitance. The charging and discharging acts upon the inductance of the lead frame or bonding wire on the system's substrate or package, resulting in the generation of noise.

The noise thus generated is expressed by the equation below.

$$V_n = L \times \frac{di}{dt} \dots\dots\dots \text{Equation (1)}$$

where, V_n : noise power supply
 L : power-supply inductance component
 $\frac{di}{dt}$: transient current

Here, because the transient current tends to increase in proportion to the number of simultaneously operating pins and their current drive capability and load capacitance, the voltage generated by the noise power supply varies depending on the following factors:

- (1) Number of power supplies
- (2) Number of simultaneously operating output buffers
- (3) Drive capability of simultaneously operating output buffers
- (4) Load capacitance of simultaneously operating output buffers

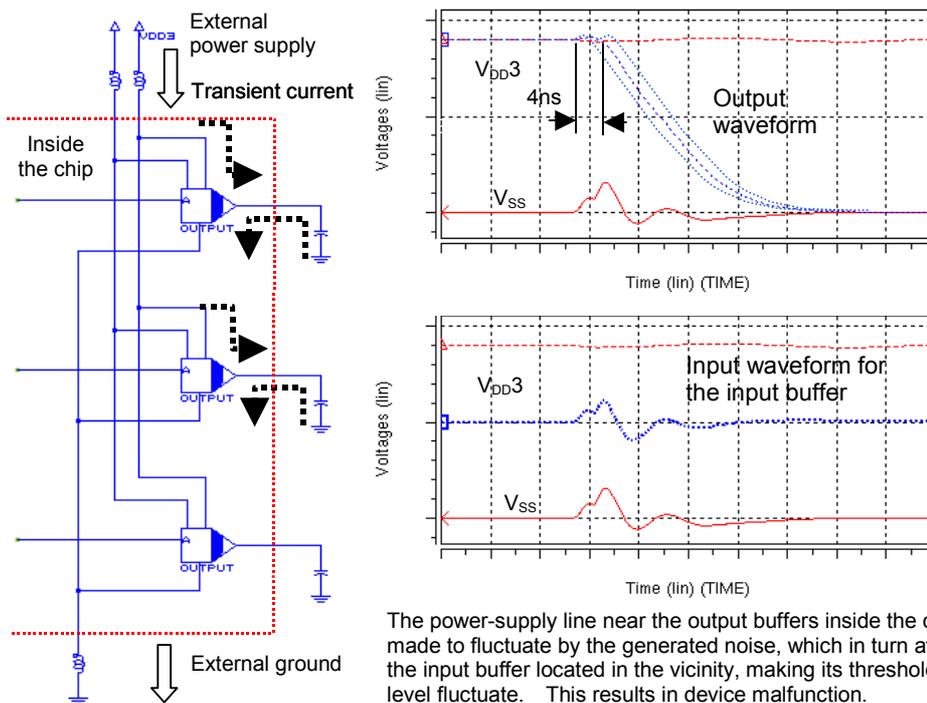


Figure 7-17 Noise due to Simultaneous Operation of Outputs

7.11.2.2 Definition of Simultaneous Operation of Outputs

The simultaneous operation of outputs refers to a phenomenon in which multiple output buffers change state in the same direction within a certain time (i.e., within 4 ns). The simultaneous operation of outputs is defined independently for each closed loop of power supplies.

The simultaneous operation of outputs in the same direction refers to the following operations:

- (1) H → L, HZ → L, X → L, or H → X output-signal operation
- (2) L → H, HZ → H, X → H, or L → H output-signal operation

where, HZ : high impedance
X : indeterminate

For bi-directional pins, the changeover of their functionality from input to output must also be taken into consideration.

7.11.2.3 Restrictions on Simultaneously Operating Output Buffers

The magnitude of the inductance of a closed loop in which output-buffer charging and discharging current flows determines the magnitude of the generated noise. The inductance of a closed loop varies with the LSI's pin layout and the board on which the LSI is mounted. To suppress the noise generated by the simultaneous operation of outputs, exercise caution in pin layout.

A closed loop here refers to a pin layout in which output-buffer pins are enclosed with the power-supply pins at both ends.

Determine whether there is simultaneous operation of outputs independently for each closed loop of power supplies.

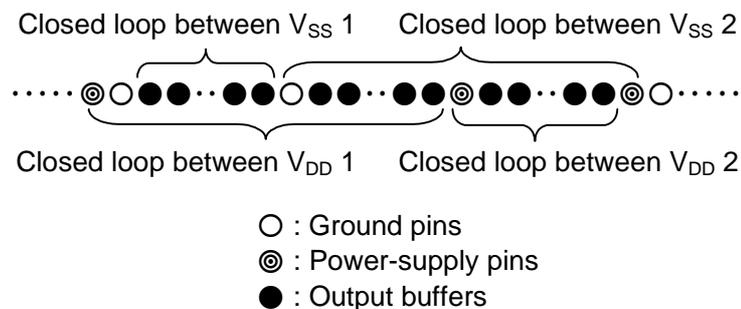


Figure 7-18 Closed Loops

Consider a case in which output buffers are placed in the manner shown above and change state simultaneously, resulting in the generation of noise. To prevent malfunction of the LSI due to noise in this case, determine whether the magnitude of noise is sufficiently large to cause malfunction from the number of output buffers and the load capacitance in each closed loop, using the coefficients in Tables 7-6 through 7-10 and the equation below.

$$\sum_k m_k \leq 1 \quad \dots\dots\dots \text{Equation (2)}$$

where, m_k : coefficient of each output buffer

For dual-power-supply systems, make this determination separately for the HV output cells in each closed loop between HV_{DD}'s, LV output cells in each closed loop between LV_{DD}'s, and for all output cells in each closed loop between V_{SS}'s.

Table 7-6 HV Output Cells, HV_{DD} = 3.3 V ± 0.3 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
1	0.048	0.053	0.059	0.063	0.063
2	0.077	0.083	0.091	0.100	0.100
3	0.100	0.111	0.125	0.143	0.143
4	0.200	0.250	0.250	0.333	0.333

Table 7-7 HV Output Cells, HV_{DD} = 3.3 V ± 0.3 V (When Using PCI)

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
1	0.077	0.083	0.091	0.100	0.100
2	0.125	0.143	0.167	0.167	0.167
3	0.167	0.200	0.200	0.250	0.250
4	0.250	0.333	0.333	0.333	0.333
PCI	0.167	0.200	0.200	0.250	0.250

Note: This applies when a PCI3V cell exists in the closed loop.

Table 7-8 HV Output Cells, HV_{DD} = 2.5 V ± 0.2 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
1	0.056	0.063	0.067	0.077	0.077
2	0.077	0.083	0.091	0.100	0.100
3	0.167	0.200	0.200	0.250	0.250
4	0.250	0.333	0.333	0.333	0.333

Table 7-9 LV Output Cells, V_{DD} or LV_{DD} = 1.8 V ± 0.15 V

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
1	0.016	0.018	0.019	0.021	0.021
2	0.038	0.042	0.045	0.050	0.050
3	0.063	0.071	0.077	0.083	0.083
4	0.125	0.143	0.167	0.167	0.167

Table 7-10 LV Output Cells, V_{DD} or $LV_{DD} = 1.5 V \pm 0.1 V$

Type	Load Capacitance				
	30 pF	50 pF	100 pF	150 pF	200 pF
1	0.014	0.016	0.017	0.019	0.019
2	0.026	0.029	0.031	0.034	0.034
3	0.043	0.048	0.053	0.059	0.059
4	0.083	0.091	0.100	0.111	0.111

Calculation example: Determine whether the magnitude of noise is sufficiently large to cause malfunction due to the simultaneous operation of outputs under the following voltage and pin-layout conditions.

- Power-supply voltage : 3.3 V/1.8 V
- Input interface : LVTTL for HV cells
LVC MOS for LV cells

Pin No.	Cells Used	Output Load Capacitance (pF)
(1)	V_{SS}	
(2)	HV_{DD}	
(3)	LV_{DD}	
(4)	HV cells, Type 4	125
(5)	HV cells, Type 4	100
(6)	HV cells, Type 4	175
(7)	HV_{DD}	
(8)	LV cells, Type 3	75
(9)	LV cells, Type 3	150
(10)	LV_{DD}	
(11)	V_{SS}	

First, because Tables 7-6 and 7-9 are used, round the output load capacitances up to the nearest whole value.

- (4) 125 pF → 150 pF
- (5) 100 pF → 100 pF
- (6) 175 pF → 200 pF
- (8) 75 pF → 100 pF
- (9) 150 pF → 150 pF

- Make determination for the closed loop between HV_{DD}'s ((2) to (7))

The HV output cells used in the closed loop between HV_{DD}'s are (4), (5), and (6).

From the input interface and the power-supply voltage, make determination using the coefficients given in Table 7-6.

$$\sum_k mk = 0.333 + 0.250 + 0.333 = 0.916$$

Thus, the result shows that the closed loop between HV_{DD}'s satisfies the determination criteria.

- Make determination for the closed loop between LV_{DD}'s ((3) to (10))

The LV output cells used in the closed loop between LV_{DD}'s are (8) and (9).

From the input interface and the power-supply voltage, make determination using the coefficients given in Table 7-9.

$$\sum_k mk = 0.077 + 0.167 = 0.244$$

Thus, the result shows that the closed loop between LV_{DD}'s satisfies the determination criteria.

- Make determination for the closed loop between V_{SS}'s ((1) to (11))

The output cells used in the closed loop between V_{SS}'s are (4), (5), (6), (8), and (9).

From the input interface and the power-supply voltage, make determination using the coefficients given in Table 7-6 for the HV output cells, and Table 7-9 for the LV output cells.

$$\sum_k mk = 0.333 + 0.250 + 0.333 + 0.077 + 0.167 = 1.160$$

Thus, the result shows that the noise restraints for malfunction due to the simultaneous operation of outputs are not met.

Therefore, change the pin layout by moving V_{SS} at (11) to a position between (8) and (9) so that the cells in the closed loop between V_{SS}'s are (4), (5), (6), and (8).

Pin No.	Cells Used	Output Load Capacitance (pF)
(1)	V _{SS}	
(2)	HV _{DD}	
(3)	LV _{DD}	
(4)	HV cells, Type 4	125
(5)	HV cells, Type 4	100
(6)	HV cells, Type 4	175
(7)	HV _{DD}	
(8)	LV cells, Type 3	75
(11)	V _{SS}	
(9)	LV cells, Type 4	150
(10)	LV _{DD}	

← V_{SS} moved to this point

Make determination for the closed loop between V_{SS}'s in this pin layout.

$$\sum_k mk = 0.333 + 0.250 + 0.333 + 0.077 = 0.993$$

Thus, the result shows that the closed loop between V_{SS} 's satisfies the determination criteria.

However, because V_{SS} has been moved, the closed loop between V_{SS} 's comprised of cells (9) and below the cells (9) requires caution.

7.11.3 Cautions and Notes Regarding the Pin Layout

When the package to be used has been decided, the pin layout on it must also be decided. For details on the power-supply pins and the number of usable input/output pins on each package in the S1K70000 series, refer to the designated "pin layout table" fill-out sheet.

When the pin layout has been decided, please provide Epson with a "pin layout table" after entering your pin layout on the designated sheet. Because placement and routing work at Epson is performed in accordance with the "pin layout tables" received from customers, carefully inspect your pin layout table before presenting it to Epson.

When the designated "pin layout table" fill-out sheet is required, please contact Epson.

The pin layout table is one of the important specifications determining the quality of the LSI. It is particularly important to prevent noise-induced malfunction of the LSI. Noise is a phenomenon that cannot easily be verified through simulation or the like.

To prevent your LSI from operating erratically for unknown reasons, we recommend that the contents below be thoroughly examined prior to the creation of your pin layout.

7.11.3.1 Fixed Power-Supply Pins

Depending on package combinations, there are several pins that can only be used for power supplies. Furthermore, some of those pins are fixed for V_{DD} use, while others are fixed for V_{SS} use. Therefore, check the "pin layout table" fill-out sheet when selecting the package to use.

7.11.3.2 Cautions and Notes Regarding the Pin Layout

The pin layout may affect the logical functions or electrical characteristics of the LSI. Furthermore, pin layout is subject to restrictions for reasons related to the LSI assembly or cell or bulk configurations. Therefore, there are several parameters that require caution in the determination of pin layout. These parameters include power-supply currents, the separation of input and output pins, critical signals, pull-up/pull-down-resistance inputs, the simultaneous operation of outputs, and large-current drivers. The following describes these parameters.

(1) Power-supply currents (I_{DD} , I_{SS})

The power-supply currents (I_{DD} , I_{SS}) specify the allowable value of the power-supply current flowing in the power-supply pins under operating conditions. If a current exceeding this allowable value flows in the power-supply pins, the current density of the LSI's internal power-supply wiring increases, causing the reliability of the LSI to degrade or the LSI to break down. Furthermore, the LSI's internal voltage increases or decreases by an amount equal to the magnitude of voltage that develops due to the current and wiring resistance. It causes the functional blocks of the LSI to operate erratically or adversely affects the DC and AC characteristics of the LSI.

To avoid these problems, the current density and the impedance of power-supply wiring must be reduced. To this end, in the design of a circuit, estimate its power

consumption and insert as many power-supply pins as necessary to ensure that the current flowing in each power-supply pin will not exceed the allowable value. For details on the power-supply pins, refer to Section 7.11.1, “Estimating the Number of Power-Supply Pins.” In addition, make sure these power-supply pins are well distributed, rather than being concentrated in one location.

It should be noted that the number of power-supply pins ultimately required for the LSI is not simply the number of power-supply pins determined above, but must also include the power-supply pins that are added for noise-protection purposes or the like. For details on the added power-supply pins, refer to Section 7.11.2, “Simultaneous Operation and Adding Power Supplies.”

(2) Noise generated by the operation of output cells

The noise generated by the operation of output cells is broadly classified into the two types specified below. To reduce these types of noise, it is helpful to install as many power-supply pins as possible.

a) Noise generated in the power-supply lines

The noise generated in the power-supply lines presents a problem when there are multiple operating outputs. It causes the LSI's input threshold level to change, which in turn causes the LSI to operate erratically. This type of noise is generated by a large current flowing into the power-supply lines due to the simultaneous operation of output cells.

Power-supply noise in particular is affected by the inductance component of the circuit. Therefore, the LSI's equivalent circuit can be expressed as shown in Figure 7-19. When the output in this circuit diagram changes state from High to Low, a current flows from the output pin into the LSI, with the current flowing through the equivalent inductance L_2 (due to the LSI package or the like) to the ground. At this time, the equivalent inductance L_2 causes the voltage of the LSI's internal V_{SS} power-supply line to change. A voltage fluctuation occurring in this V_{SS} power-supply line is referred to here as the noise generated in the power-supply line. Because this type of noise is caused mainly by the equivalent inductance L_2 , there is a tendency that the greater the surge of the power-supply current, the greater the magnitude of the noise generated.

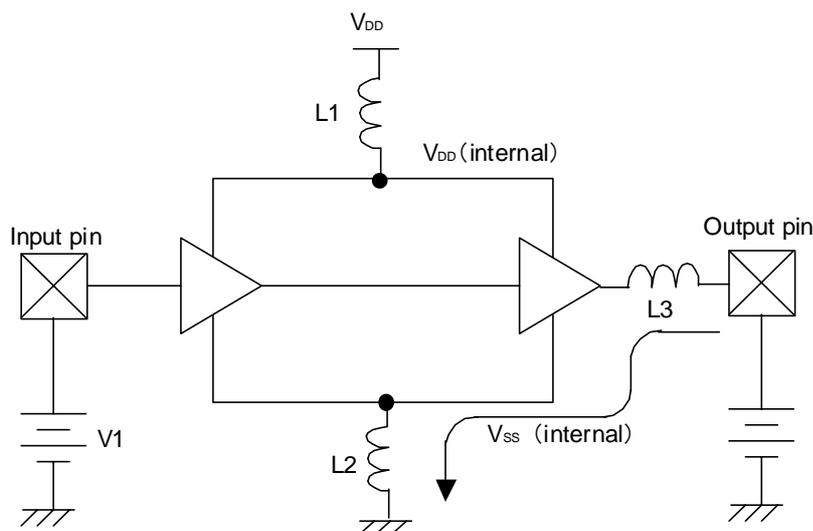


Figure 7-19 LSI Equivalent Circuit

b) Overshoot, undershoot, and ringing

Noises known as overshoot, undershoot, or ringing are generated by the equivalent inductance at the output pins. L3 in Figure 7-19 is an example of this equivalent inductance. Because inductance has the property of storing energy, even when the output goes low or high, overshoots and undershoots are proportional to the magnitude of the current flowing in the output and the change in rate of the current due to the stored energy.

The most efficient means of reducing overshoots and undershoots is the use of output cells with a small drive capability. Overshoots and undershoots tend to decrease as the load capacitance increases. Therefore, be particularly careful when using cells with a large drive capability.

(3) Isolating input and output pins

Separating the group of input pins from the group of output pins in design of the pin layout is an important technique for reducing the effect of noise.

Because the input pins and the bi-directional pins set for input are susceptible to noise, make sure they do not coexist with output pins in design of the pin layout. To this end, separate the group of input pins, the group of output pins, and the group of bi-directional pins according to the power-supply pins (V_{DD} , V_{SS}) when placing each group of pins.

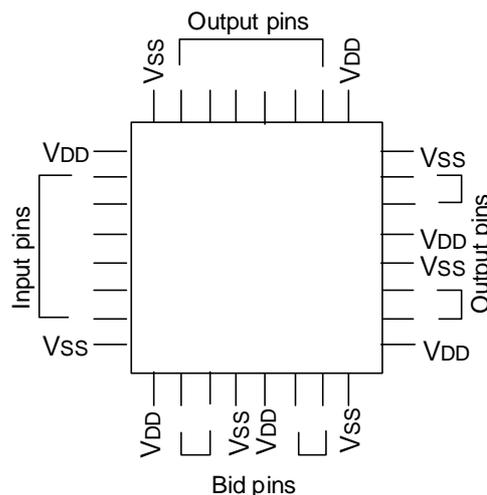


Figure 7-20 Example of Separating Input and Output Pins

(4) Critical signals

For critical signals such as input pins for clock and output pins operating at high speed, observe the precautions described below when placing pins.

- The clock and reset pins that are required to reduce the effects of noise must be placed away from the output pins at positions near the power-supply pins. (Figure 7-21)
- The input/output pins of the oscillation circuit (OSCIN, OSCOUT) must be placed close to each other, enclosed with the power-supply pins (V_{DD} , V_{SS}). In addition, make sure that no output pins synchronous with the oscillation circuit are placed near these pins. (Figure 7-22)
- Input and output pins operating at high speed must be placed near the center of one edge of the chip (package). (Figure 7-21)

- d) If the delay from specific input pins to specific output pins has only a minimal margin with respect to the customer specification, these input and output pins must be placed close to each other. (Figure 7-21)

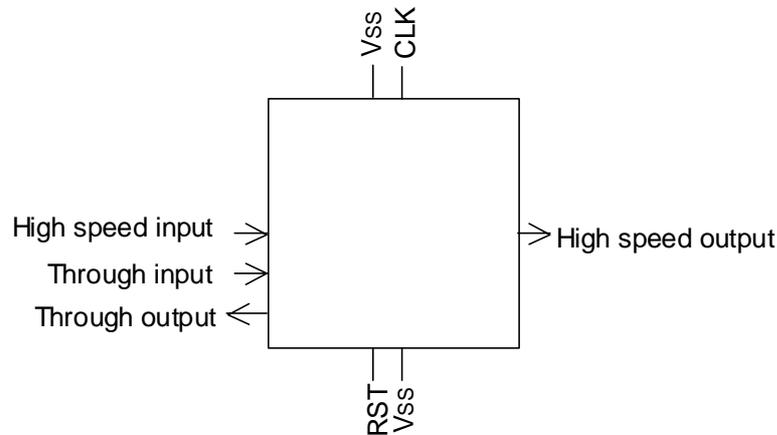


Figure 7-21 Example 1 of a Layout for Critical Signals

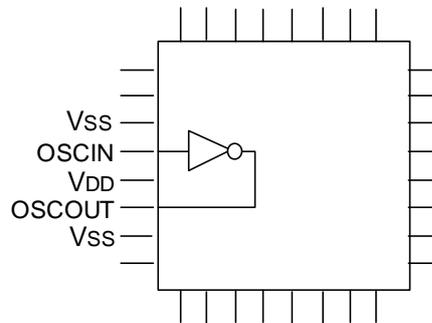


Figure 7-22 Example 2 of a Layout for Critical Signals

(5) Pull-up/pull-down resistor inputs

The pull-up/pull-down resistance values are rather large, ranging from several 10k to several 100k Ω , and have dependency on the power-supply voltage for reasons related to their structure.

Therefore, when using these inputs as test pins or for other purposes while they are left open, note the precautions described below, as these pins become susceptible to power-supply noise and could cause the LSI to operate erratically.

- The pull-up/pull-down resistor inputs must be placed as far as possible from the high-speed input-signal pins (e.g., clock input pins). (Figure 7-23)
- The pull-up/pull-down resistor inputs must be placed away from the output-signal pins (particularly large-current output pins). (Figure 7-24)

In addition to the precautions on pin layout, take the following points into consideration as well.

- Pull-up/pull-down resistor inputs must be processed on the circuit board (PCB) as much as possible.
- Pull-up/pull-down resistors with small resistance values are preferable.

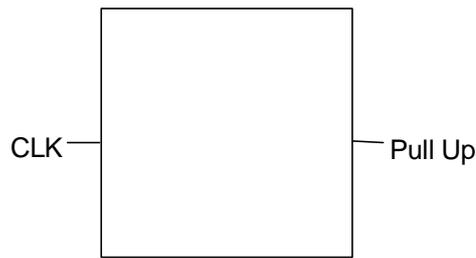


Figure 7-23 Example 1 of Placement of Pull-up/Pull-down Resistors

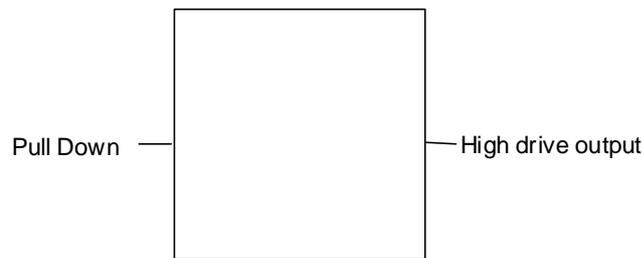


Figure 7-24 Example 2 of Placement of Pull-up/Pull-down Resistors

(6) Simultaneous operation of outputs

When multiple output pins operate simultaneously, they tend to generate noise, causing the LSI to operate erratically. When it is necessary to operate a number of output pins simultaneously, add power-supply pins to the group of output pins that change state simultaneously, in order to prevent noise-induced malfunction of the LSI. For details on the number of power-supply pins to add and the procedure for placing the additional power-supply pins, refer to Section 7.12.2, “Simultaneous Operation and Adding Power Supplies.”

As a means of reducing said noise, cells for delay use may be added in a stage preceding one group of output pins. This helps to reduce the number of output cells that change state simultaneously, thereby reducing the amount of noise generated. (Figure 7-26)

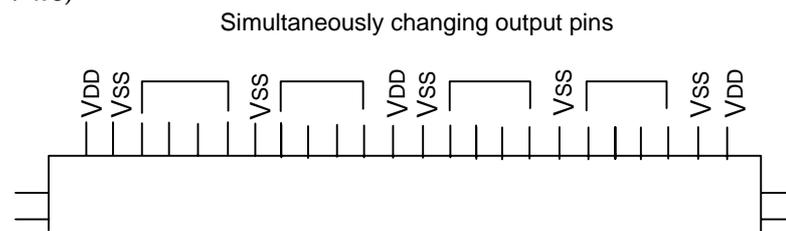


Figure 7-25 Example of Adding Power-Supply Pins

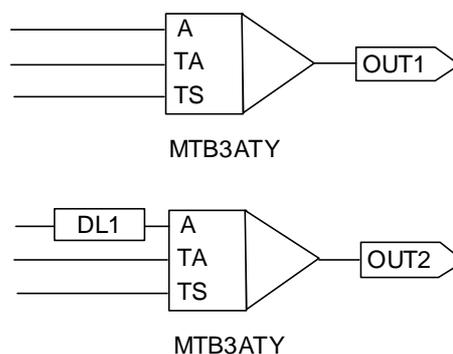


Figure 7-26 Example of Adding Delay Cells

(7) Large-current drivers

When using the output of large-current drivers ($I_{OL} = 12 \text{ mA}$, PCI), observe the restrictions described below when placing pins.

a) Constraints on Strengthening the power-supplies

Large-current drivers have large drive capability; therefore, the amount of noise generated by their output buffers during operation is also large. This noise may cause the LSI to operate erratically.

When using large-current drivers, add power-supply pins near their pins in order to secure the power supply needed for the large-current drivers. (Figure 7-27)

b) Low-noise pre-drivers

To reduce the amount of noise generated by the output buffers of large-current drivers during operation, low-noise-type output and bi-directional buffers available from Epson may be used. For details, refer to Chapter 4, "Types of Input/Output Buffers and Their Use."

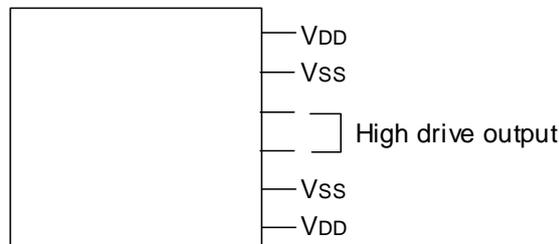


Figure 7-27 Example of Strengthening Power-Supplies

(8) Other precautions

a) Non-connection (NC) pins

If the number of pads of the LSI is smaller than the number of pins on the package, or if the package has pins that cannot be assembled, some pins on the package are unusable.

b) Tab hanger pins

Tab hanger pins are pins on the package that are connected directly to the LSI substrate. These pins are tied to the VSS (GND) level without being furnished with external power supplies for the aforementioned reasons. Normally, leave these pins open on the board.

7.11.4 Example of the Recommended Pin Layout

Pin layout is an important factor in ensuring that the LSI operates normally. The following shows a pin-layout diagram (Figure 7-28) based on the information given in this chapter. Refer to this example in determining the pin layout.

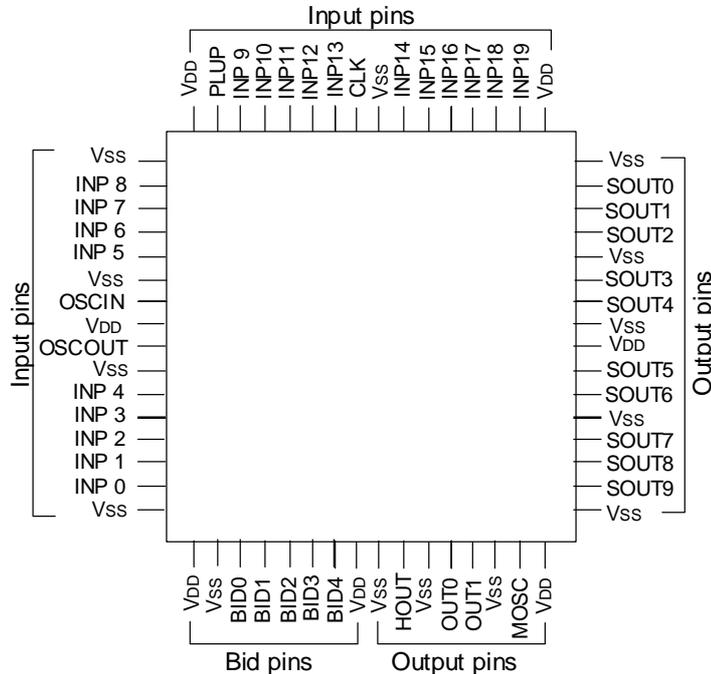


Figure 7-28 Example of the Recommended Pin Layout

Input pins are placed on the top and left sides of the package, with the output pins changing simultaneously on its right sides, and the bi-directional pins and other output pins changing simultaneously on its bottom side.

Table 7-11 Pin Layout Example

Placement	Pin Name	Explanation of Pin Name	Detailed Explanation of the Placement of Each Pin
Upper edge	PLUP	Input pins with pull-ups	Placed at positions less affected by noise
	CLK	Input pins for the clock	Placed near the center of the edge of the package or near the power-supply pins
Left edge	OSCIN	Oscillator pins	Placed near the center of the edge of the package or near the power supply pins
	OSCOU		Placed near the center of the edge of the package or near the power-supply pins
	INP0–19	Input pins	Placed apart from other pins, divided by power-supply pins
Right edge	SOUT0–9	Simultaneously changing output pins	Placed apart from other pins, divided by power-supply pins, with power-supply pins added
Bottom edge	BID0–4	Bi-directional pins	Placed apart from other pins, divided by power-supply pins
	MOSC	Oscillator monitor output pins	Placed near the power-supply pins away from the oscillator pins
	HOUT	High-drive output pins	Power-supply pins placed nearby
	OUT01	Output pins	Placed apart from other pins, divided by power-supply pins
Overall edges	V _{DD}	V _{DD} power-supply pins	
	V _{SS}	V _{SS} (GND) power-supply pins	

7.12 About Power Supply Cutoff

When S1K/S1X70000-series cells are used to create a chip designed to power-supply Cutoff specifications, note the following.

7.12.1 For Single-Power-Supply Systems

- (1) In cases in which input signals from the outside also enter High-Z state when the power supply is cut

Basically, all types of input/output buffers can be used. Even in cases in which input/output buffers are separated by pairs of power-supply pins and the power supply for part of the area is to be cut off, all types of input/output buffers can be used unless signals from the outside are applied.

(However, this is possible providing that the power supplies for all of the related circuits, including the internal cell area, are cut off.)

- (2) In cases in which input signals from the outside are applied when the power supply is cut off or pull-up resistors are incorporated external to the chip

If input signals from the outside are applied while the power supply is cut off, leakage current may occur, depending on the type of input/output buffer used.

Therefore, the following types of input/output buffers cannot be used in this design:

- Input buffers with pull-up resistors. However, this does not include Fail Safe cells.
- Output buffers other than Fail Safe buffers. However, the Open drain type can be used.
- Bi-directional buffers other than Fail Safe buffers. However, the Open drain type can be used.

(Even in cases in which input/output buffers are separated by pairs of power-supply pins and the power supply for part of the area is to be cut off, the input/output buffers listed above cannot be used in the relevant area.)

7.12.2 For Dual-Power-Supply Systems

- (1) In cases in which LV_{DD} is cut off while HV_{DD} remains on

In this design, the output mode of the HV_{DD} output buffers or HV_{DD} bi-directional buffers may become uncontrollable. In the worst-case scenario, current may even continue to flow into those buffers. Therefore, the power supply cannot be cut off in this design.

- (2) In cases in which HV_{DD} is cut off while LV_{DD} remains on

- a) If inputs from the outside also enter High-Z state when the HV_{DD} power supply is cut off

- LV_{DD} cells

If the LV inputs also enter High-Z state, use Gated cells (LVCMOS-AND cells). Current can be prevented from flowing in the initial input stage by pulling the control pin C Low in the internal circuit.

No specific restrictions apply if LV inputs do not enter High-Z state.

- HV_{DD} cells

HV -use Gated cells are not available in the S1K/S1X70000 series. However, Cutoff cells are available for use in power-supply cutoff design. This I/O cell allows the current flowing in input circuits to be shut off by pulling the control pin C Low in the internal circuit. (In this case, the output pin X outputs a High-level signal.)

Note, however, that control pin C of Cutoff cells must always be fixed high during normal operation.

- b) If input signals from the outside are applied when the HV_{DD} power supply is cut off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

If the LV inputs enter High-Z state, use Gated cells (LVCMOS-AND cells). Current can be prevented from flowing in the initial input stage by pulling control pin C Low in the internal circuit.

No specific restrictions apply if the LV inputs do not enter High-Z state.

- HV_{DD} cells

For output buffers, use Open drain-type cells.

For input buffers, use Cutoff cells (input buffers with pull-up resistors cannot be used, however). For bi-directional buffers, use Open drain-type Cutoff cells. (If bi-directional buffers of the ordinary Cutoff type are used here, leakage current will occur.) These types of input/output buffers allow the current flowing in input circuits to be shut off by pulling control pin C Low in the internal circuit. (In this case, output pin X outputs a High-level signal.)

Note, however, that control pin C of Cutoff cells must always be fixed high during normal operation.

For details on the Gated and Cutoff cells mentioned above, refer to Section 4.2.5, "Gated Cells," and Section 4.3.6, "Cutoff Cells." Even in cases in which

input/output buffers are separated by pairs of power-supply pin and the power supply for part of the area is to be cut off, no input/output buffers other than those mentioned above can be used in the relevant area.

(3) In cases in which both HV_{DD} and LV_{DD} are cut off

- a) If inputs from the outside also enter High-Z state when the power supplies are cut off

Basically, all types of input/output buffers can be used. Even in cases in which input/output buffers are separated by pairs of power-supply pins and the power supplies for part of the area are to be cut off, all types of input/output buffers can be used unless signals from the outside are applied.

(However, this is possible provided that the power supplies for all of the related circuits, including the internal cell area, are cut off.)

- b) If input signals from the outside are applied when the power supplies are cut off or pull-up resistors are incorporated external to the chip

- LV_{DD} cells

If input signals from the outside are applied while the power supplies are cut off, leakage current may occur, depending on the type of input/output buffer used.

Therefore, the following types of input/output buffers cannot be used in this design:

- Input buffers with pull-up resistors. However, this does not include Fail Safe cells.
- Output buffers other than Fail Safe buffers. However, the Open drain type can be used.
- Bi-directional buffers other than Fail Safe buffers. However, the Open drain type can be used.

- HV_{DD} cells

As with LV_{DD} cells, leakage current may occur depending on the type of input/output buffer used. The following types of input/output buffers cannot be used in this design.

- PCI cells and input buffers with pull-up resistors
- Output buffers other than Open drain buffers
- Bi-directional buffers other than Open drain buffers

(Even in cases in which input/output buffers are separated by pairs of power-supply pins and the power supplies for part of the area are to be cut off, the input/output buffers mentioned above cannot be used in the relevant area.)

Chapter 8 Circuit Design that Takes Testability into Account

When ICs are shipped from the Epson factory, they are tested for product fitness through the use of an LSI tester. This requires that circuits be designed in consideration of the testability of the IC. Therefore, be sure to take the points specified below into consideration in the design of a circuit. The contents described here do not apply to combined use with JTAG circuits. If JTAG circuits are desired, refer to Section 8.8, "Boundary Scan Design," and create test patterns that are capable of performing DC testing. Furthermore, if test circuits cannot be added, contact the sales division of Epson for confirmation.

8.1 Consideration Regarding Circuit Initialization

Although a number of flip-flops (FFs) are used in a circuit, the initial state of all FFs is X (indeterminate) when the circuit is tested using an LSI tester or simulated on a simulator. For this reason, depending on the circuit configuration, the circuit cannot be initialized or requires a huge number of test patterns for initialization. To avoid this problem, in the design of a circuit, be sure to use FFs with reset inputs or other means in order to enable the circuit to be initialized easily.

8.2 Consideration Regarding Compressing the Test Patterns

As the circuit size increases, so does the size of test patterns. Be aware, however, that the size of test patterns is subject to the following limitations imposed by the use of an LSI tester.

Number of events per test pattern	: Up to 256K events
Number of test patterns	: Up to 30
Total number of events in all test patterns	: Up to 1M events

These limitations apply to test patterns for DC testing, including test patterns for Z inspection, test patterns for test circuits, and test patterns for ROM or megacells prepared by Epson. For details on the number of ROM or megacell test patterns and the number of events in those test patterns, contact the sales division of Epson. For RAM test patterns, note that although the reference patterns prepared by customers are subject to said limitations, the test patterns for complete RAM-pattern verification prepared by Epson are not subject to limitations.

In the design of a circuit, be sure to use an appropriate means of improving the circuit's testability and thereby reducing the number of necessary test patterns by, for example, installing test pins that enable a clock to be input in the middle of a multi-stage counter, or by adding test pins that allow the LSI's internal signals to be monitored.

8.3 Test Circuit Which Simplifies DC and AC Testing

For the S1K/S1X70000 series, customers are expected to configure a test circuit and add it to the test circuit in order to allow shipment testing such as DC and AC testing by Epson to be performed efficiently. If a test circuit cannot be added to your circuit, please contact Epson for confirmation.

8.3.1 Circuit Configuration When Output Buffers with a Test Circuit are Used

Figure 8-1 shows the configuration of the test circuit “L1TCIR2” recommended by Epson.

Figure 8-3 shows DC and AC test circuits and a practical example of a test circuit for 2-word x 2-bit RAM (this memory configuration does not actually exist, however). Refer to these circuits and (1) through (4) below when configuring a test circuit. If RAM or functional cells are included in your circuit, also refer to Section 8.4, “RAM and ROM Test Circuits,” and Section 8.6, “Function Cell Test Circuits.”

(1) Adding and selecting pins for testing

To configure pins for testing, add the three types of test pins specified below. For these test pins, select appropriate cells or buffers available.

- Test enable pin: 1 pin.
- Test mode select input pin: 4 pins.
- Monitor output pin for AC testing: 1 pin.

Table 8-1 Test Pins Constraints

Test Pin Type	Number of Pins	Name of Pins (ex.)	Constraints, Notes, etc.
Test enable pin	1 pin.	TSTEN	Dedicated input pin. Use ITST1 for the input buffer. H: test mode; L: normal mode
Test mode select input pin	4 pins.	INP0–INP3	Input pin shareable with the user functions, but cannot be shared with bi-directional pins. Avoid sharing this pin with other input pins that have a critical path.
Monitor output pin for AC testing	1 pin.	OUT3	Input pin shareable with the user functions, but cannot be shared with N channel open drain cells
Output and input/output pins	—	—	Output buffer with test mode (Input/output pins allowed)

- About DC testing

This test checks whether all input and output pins satisfy the designated specifications for DC characteristics. If no test circuits are included, customers will be requested to create test patterns to enable measurement of DC characteristics, which may require a huge number of man-hours. Use of a test circuit facilitates the creation of test patterns and therefore makes it easy to measure DC characteristics.

- AC testing

This test involves measuring pin-to-pin delays (delays in input pins to output pins). If the actual operating frequency cannot be inspected using an LSI tester, the operating speed will be guaranteed by measuring the delay in a specific path. If the Epson-recommended test circuit “L1TCR2” is used, variations between lots will be evaluated by measuring the dedicated AC path using an AC-test monitor output pin. Because the recommended test circuit “L1TCR2” does so by judging the difference in measured values between the tested device’s delay and the bypass delay, consistent delay measurement that is not dependent on the intra-chip

location of the test circuit or measurement conditions external to the chip is always possible.

(2) Adding a test-mode control circuit

a: Add a test-mode control circuit (L1TCR2).

b: Connect output X pin for the input buffer (LITST1) of the dedicated test-mode input pin to the input TST pin of the “L1TCIR2”.

c: Connect the outputs for the input buffers of test-mode select input pins to the input pins of the “L1TCR2”.

Connect the output for the INP0 input buffer to the TM0 pin of the “L1TCR2”.

Connect the output for the INP1 input buffer to the TM1 pin of the “L1TCR2”.

Connect the output for the INP2 input buffer to the TM2 pin of the “L1TCR2”.

Connect the output for the INP3 input buffer to the TM3 pin of the “L1TCR2”.

d: Connect the output pins of the test-mode control circuit (TCIR2) to the input pins of the input/output buffers.

- Connect the output pin (TAC) of the L1TCIR2 to the TA pin of the input/output buffer of the AC-test monitor output pin (OUT3).
- Connect the output pin (TS) of the L1TCIR2 to the TS pins of all input/output buffers.
- Connect the output pin (TD) of the L1TCIR2 to the TA pins of all input/output buffers other than the test monitor output pin (OUT3).
- Connect the output pin (TE) of the L1TCIR2 to the TE pins of the input/output buffers for the 3-state pin (OUT2) and bi-directional pin (BID1).
- Use the output pin (MS) of the L1TCIR2 for control of each macro when RAM or function cells are included in your circuit.

e: Even if the signals connected to the TA, TE, or TS pins of input/output buffers exceed the fan-out limits, the violation of the fan-out limits can be ignored without causing any problem.

(3) Typical examples for setting test mode

a: DC test

- Quiescent-current measurement mode
TSTEN ... High
- Output-characteristic (V_{OH}/V_{OL}) measurement mode
TSTEN ... High
INP0 ... Low
INP1 ... High or low
INP2 ... Low
Measured pins*1 ... High or low

*1: This includes all output and all bi-directional pins other than the AC-test monitor output pin.

- Leakage-current measurement mode
TSTEN ... High
INP0 ... High
INP1 ... Low

Table 8-2 Truth Table for Test Circuit

INPUT					OUTPUT				
TST	TM3	TM2	TM1	TM0	TS	TD	TE	TAC	MS
0	x	x	x	x	0	0	0	0	0
1	x	x	x	x	1	x	x	x	x
1	x	x	x	x	1	x	x	x	x
1	x	1	1	1	1	1	1	1	0
1	x	1	1	0	1	1	1	1	0
1	x	1	0	1	1	1	1	1	0
1	x	0	1	1	1	1	1	1	0
1	x	0	0	1	1	1	0	1	1
1	x	0	1	0	1	1	0	1	0
1	0	1	0	0	1	0	0	1	0
1	0	0	0	0	1	0	0	0	0
1	1	1	0	0	1	0	0	1	0
1	1	0	0	0	1	0	0	0	0

(4) Generating the test patterns

To ensure that DC and AC testing are conducted efficiently, customers will be requested to design both a test circuit and a test pattern. Figure 8-4 shows a practical example of a test pattern for the example test circuit shown in Figure 8-3. Note the following points in generating the test pattern.

- a. Generate a test pattern like the one shown in the example, separately from a pattern for circuit verification.
- b. This test pattern must contain a description of all pins used in the circuit.
- c. A test pattern for measuring both delay-cell delay and bypass delay for AC testing is required. Referring to Figure 8-4, generate a test pattern that allows two pulses to be applied in each mode.
- d. In a pattern for circuit verification as well, write test pins (e.g., TSTEN). In such a case, set the input level for the test pin (e.g., TSTEN) to logic 0.
- e. When the input level for the test pin is logic 1, all of the pull-up/pull-down resistors enter an inactive state.

(5) Circuit configuration of the test circuit “L1TCIR2”

Shown in Figure 8-1 is the circuit configuration of the test circuit “L1TCIR2” recommended by Epson. The L1TCIR2 places the entire circuit in test mode and provides an efficient means of conducting DC and AC testing for the LSI.

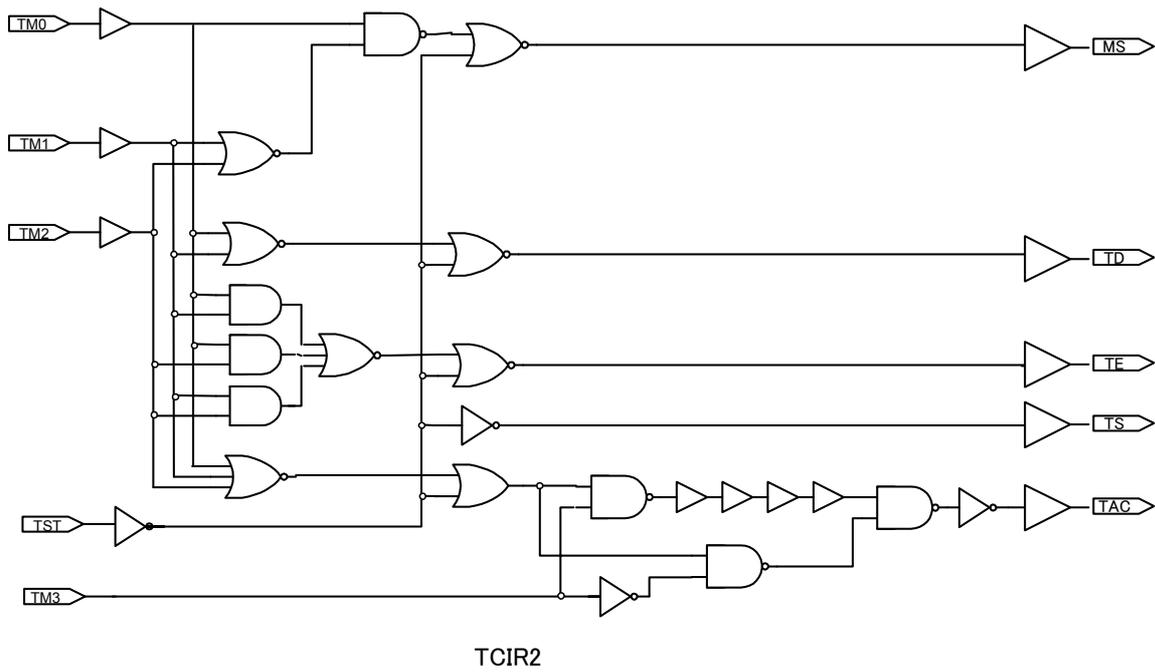


Figure 8-1 Internal Circuit of the TCIR2

(6) Circuit configuration for input-logic-level verification testing

The input logic levels of all input and input/output cells in the S1K/S1X70000 series are managed using values that have been preliminarily design-guaranteed in the design stage at Epson. However, if the customer specification requires verification of the input logic levels, customers will be requested to insert an input-logic-level verification circuit (e.g., an AND-chain circuit) and generate a test pattern for verification purposes. In so doing, refer to the example of an AND-chain circuit shown below. An AND-chain circuit consists of input and input/output cells connected in a chain, and it is used to perform verification by sequentially changing all connected pins from High to Low or Low to High using a test pattern.

Example:

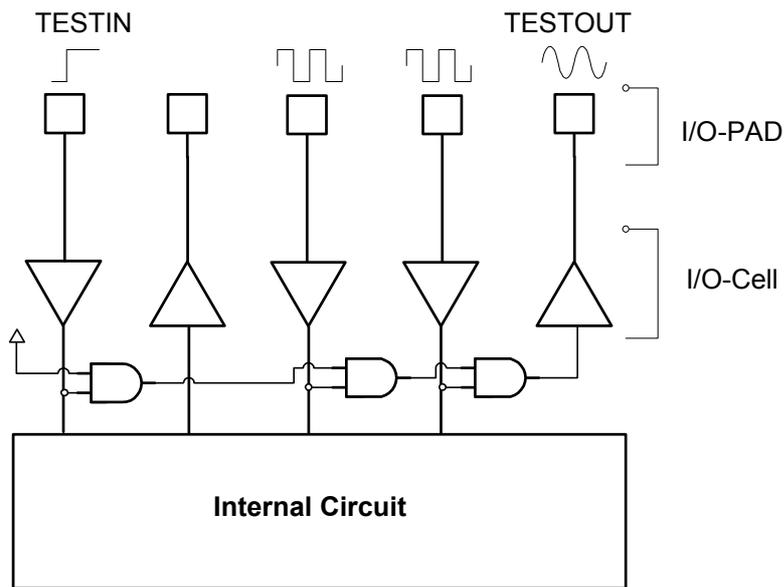


Figure 8-2 AND-chain circuit

(7) Other

The S1K70000 series uses active pull-up/pull-down resistors. When the test circuit “L1TCIR2” is used in a customer’s circuit, the pull-up/pull-down resistors are forcibly disabled in quiescent-current measurement mode. In such a case, the properties of the customer’s pull-up/pull-down-resistor control pin “PC” are ignored. If control of the pull-up/pull-down resistors is unnecessary, the PC pin must be fixed to the Low level. In that case as well, the pull-up/pull-down resistors are disabled while in test mode.

8.3.2 Circuit Configuration When Output Buffers without a Test Circuit are Used

If, due to the configuration of the customer’s circuit design, output buffers with a test function or the Epson-recommended test circuit “L1TCIR2” cannot be used, the operating speed of the customer’s circuit will be guaranteed by measuring the critical paths it contains. In that case, customers will be requested to generate a test pattern that is capable of measuring the customer’s critical paths.

If critical paths in the customer’s circuit are not particularly specified, a delay measurement device “L1ACP1” and a selector circuit that selects between the customer’s circuit and the “L1ACP1” will be inserted by Epson. In addition, by measuring the dedicated AC path in this configuration, variations between lots will be evaluated and the operating speed guaranteed. In such a case, customers will be requested to select two input pins and one output pin from the customer’s circuit. Because the delay measurement device “L1ACP1” does this by judging the difference in measured values between the tested device’s delay and the bypass delay, it is always possible to achieve consistent delay measurement not dependent on the intra-chip location of the test circuit or measurement conditions external to the chip.

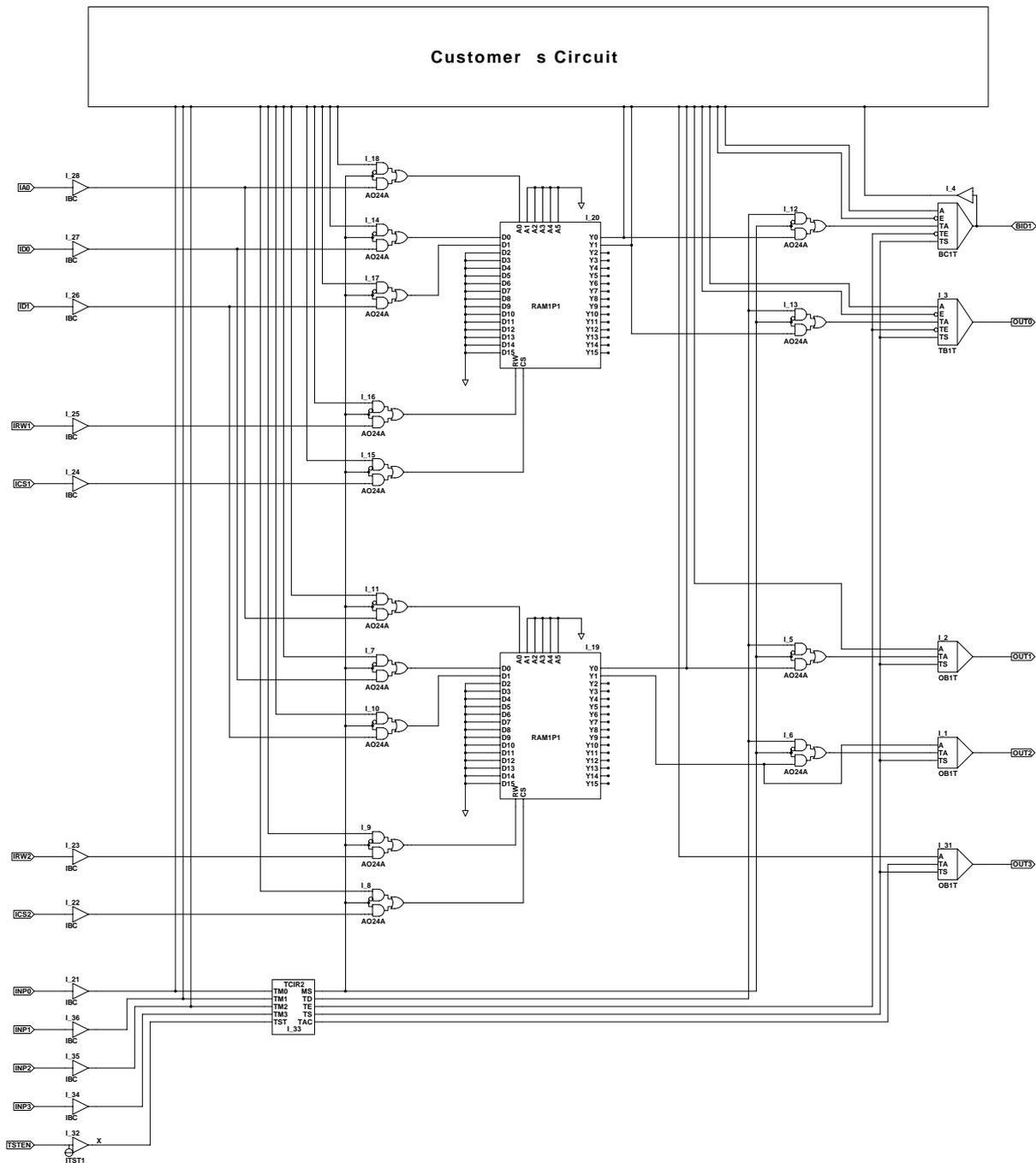


Figure 8-3 Example of a Test Circuit

● Example of the APF format

```
# EXAMPLE of Test Pattern for AC & DC Test by TCIR2
$RATE 200000
$RESOLUTION 0.001ns
$STROBE 185000
$NODE
TSTEN          ID  0
INP0           I  0
INP1           I  0
INP2           I  0
INP3           I  0
IA0            I  0
ID0            I  0
ID1            I  0
ICS1           I  0
ICS2           I  0
IRW1           I  0
IRW2           I  0
BID1           B  0
OUT0           0
OUT1           0
OUT2           0
OUT3           0
$ENDNODE
$PATTERN
#      TIIIIIIIIIIIB0000
#      SNNNNADDCCRRUUUU
#      TPPPP001SSWWDTTT
#      E0123  121210123
#      N
#
#      IIIIIIIIIIIIB0000
#      U
#
0 0000. .... XXXX
1 1000. .... LLLL: Dedicated-AC-path measurement 1 (bypass)
2 1001. .... LLLH      ↑
3 1000. .... LLLL      ↑
4 1001. .... LLLL: Dedicated-AC-path measurement 2 (delay path)
5 1001. .... LLLH      ↑
6 1000. .... LLLL      ↑
7 1101. .... 0ZHHH: Off-state leakage-current measurement
8 1101. .... 1ZHHH      ↑
9 1000. .... LLLL: Output-characteristic measurement
10 1010. .... HHHH      ↑
$ENDPATTERN
#
# EOF
Note: The '.' Denotes logic 1 or 0.
```

Figure 8-4 Example of the Generation of a Test Pattern When There is a Test Option

8.4 RAM and ROM Test Circuit

8.4.1 Basic-Cell-Type RAM

When a RAM is used it is necessary to test all bits before shipping the product. RAM terminals must be accessible via primary I/O pins.

RAM test circuitry can be implemented, which multiplexes existing pin functionality with direct RAM access functionality so as to avoid increasing the design's pin count.

No bi-directional pins can be used for input as they all are placed in an output state during RAM test. If input pins are inadequate, attach a control circuit to the target bi-directional TE pin.

Also, when multiple RAMs are used, we recommend that each RAM's pins be accessible via unique I/O pins. However, when the number of external I/O pins is inadequate, each RAM's pins may share common external I/O pins.

The example test circuit in Figure 8-3 performs normal operations unless in test mode; when placed in test mode, the circuit allows data to be written directly to RAM from external pins ICS1-2, IRW1-2, ID0-1, and IA0. At the same time, RAM output in this circuit can be read out to external pins AY0 and AY1.

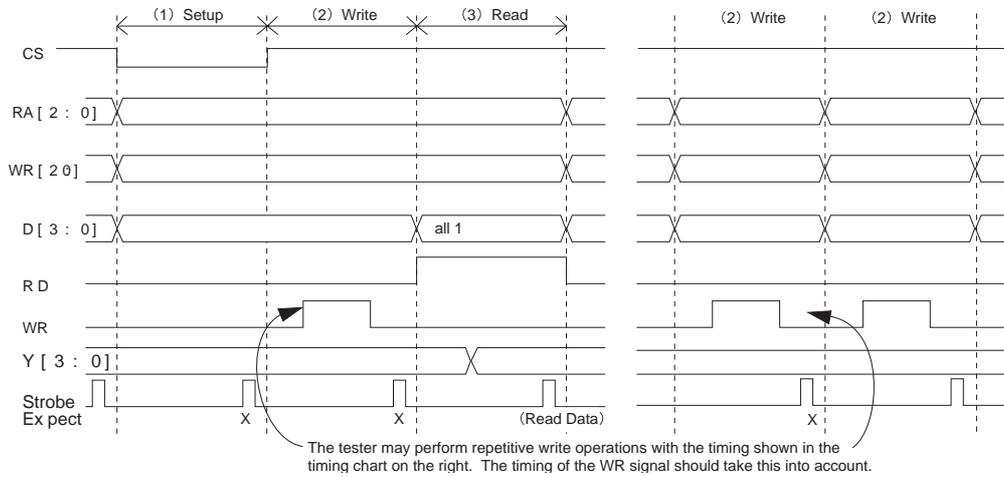
Although it is possible to share the RAM pins with bi-directional pins or 3-state output pins, it is necessary to tie the bi-directional pins to either an input or an output state during RAM test. However, please do not allocate an input buffer with a pull-up resistor to CS, because doing so would make it impossible to measure the quiescent current.

8.4.1.1 RAM Test Patterns

After incorporating RAM test circuitry, it is necessary to make test patterns for both the normal operating state and the test state of the chip. Checks are performed in the normal state to verify the connection with the customer's circuits, and are performed to insure that the test circuit is correct in the test state. Also, we request a test pattern to serve as a template when Epson generates the RAM test pattern. See Figures 8-5 and 8-6 for an outline of how to generate this test pattern.

This pattern serves as a template for 2-port RAM tests.

• Timing chart



• Example of APF Format

```

$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns

$NODE
INPA I 0
INPB I 0
INPC I 0
INPD I 0
INPE I 0
INPF I 0
INPG I 0
INPH N 20000 120000
INPI I 0
.
OUTA 0
OUTB 0
OUTC 0
OUTD 0
.
$ENDNODE

$PATTERN
# AAADDDDRC YYY
# 0120123WS 0123
#
0 000101010..XXXX..
1 0001010N1..XXXX..
2 000101011..HLHL..
3 101111110..XXXX..
4 1011111N1..XXXX..
5 101111111..HHHH..
6 111010110..XXXX..
7 1110101N1..XXXX..
8 111010111..LHLH..
    
```

Please provide all I/O pins used in performing simulation.
Reference the timing chart below to set timing.

It is useful to place comments here.

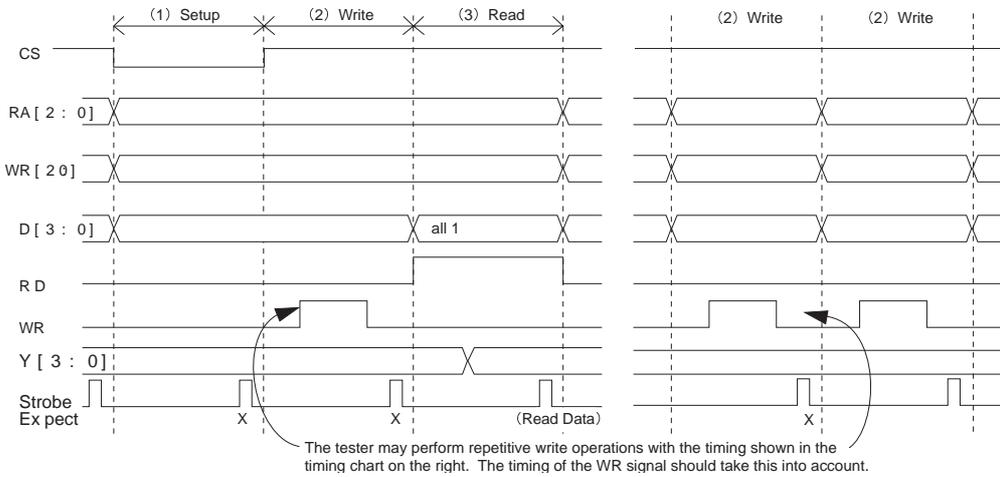
When a sequence is necessary to set the test mode, input the pattern here.

- [1] Access the lowest address, a middle address and the highest address.
- [2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.
- [3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.
- [4] Change the data to be written for each address tested.
- [5] Verify that the results are the same as expected from the results of the simulations.

Figure 8-5 Generating 1-port RAM Test Pattern

This pattern serves as a template for 2-port RAM tests.

• Timing chart



• Example of APF Format

```
$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
```

```
$NODE
INPA I 0
INPB I 0
INPC I 0
INPD I 0
INPE I 0
INPF I 0
INPG I 0
INPH I 0
INPI I 0
INPJ I 0
INPK I 0
INPL P 20000 120000
INPM I 0
.
.
.
OUTA 0
OUTB 0
OUTC 0
OUTD 0
.
.
$ENDNODE
```

Please provide all I/O pins used in performing simulation.
Reference the timing chart below to set timing.

```
$PATTERN
# RRRWWW
# AAAAAADDDDRWC.YYYY..
# 0120120123DRS.0123..
#
0 0000001010000.XXXX..
1 00000010100P1.XXXX..
2 0000001111101.HLHL..
3 1011011111000.XXXX..
4 10110111110P1.XXXX..
5 1011010000101.HHHH..
6 1111110101000.XXXX..
7 11111101010P1.XXXX..
8 1111111111101.LLHL..
```

- It is useful to place comments here.
- When a sequence is necessary to set the test mode, input the pattern here.
- [1] Access the lowest address, a middle address and the highest address.
- [2] Structure a single access from 3 events (test cycles). In the first event, set the data and the address. In the next event, perform a write. In the third event, perform a read.
- [3] Use an RZ waveform to describe the RW signal so that the write operation can be completed in a signal event.
- [4] Change the data to be written for each address tested.
- [5] Verify that the results are the same as expected from the results of the simulations.
- [6] Set all bits of data to " 1 " when reading. However, if all bits of the data to write are 1's, all bits of data during reading must be 0's.

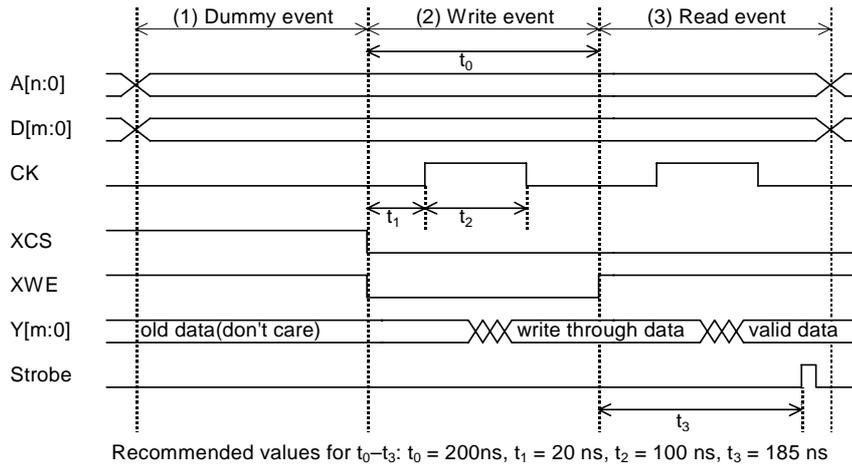
Figure 8-6 Generating 2-port RAM Test Pattern

8.4.2 High-Density-Type 1-Port RAM

For high-density-type 1-port RAM, as for Basic-cell-type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (Epson will use the test-state test patterns as templates as it creates dedicated RAM test patterns.) (For details, refer to Section 8.4.1, “Basic-Cell-Type RAM.”)

When creating test-state test patterns for high-density-type 1-port RAM, please follow the prescribed procedure.

- Timing chart



- Example for APF format (16 words x 4 bits)

```

$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3 I 0
IA2 I 0
IA1 I 0
IA0 I 0
ICK P 20000 120000
IXCS I 0
IXWE I 0
ID3 I 0
ID2 I 0
ID1 I 0
ID0 I 0
...
OY3 O
OY2 O
OY1 O
OY0 O
$ENDNODE

$PATTERN
# AAAACXXDDDD...YYYY
# 3210KCW3210...3210
# SE
0 00000010000...XXXX
1 0000P100000...XXXX
2 0000P110000...LLLL
3 01010010101...XXXX
4 0101P100101...XXXX
5 0101P110101...LHLH
6 11110011111...XXXX
7 1111P101111...XXXX
8 1111P111111...HHHH
$ENDPATTERN
                
```

Be sure to write all I/O pins to ensure that simulations are performed.

- (1) Access the test pattern for the dummy, write, and read events in one operation (one tester cycle) and perform the test three times: first the lower address, then the middle address, then the upper address.
- (2) Set the address and data at the beginning of a dummy event, write the data in a write event, and read the data in a read event.
- (3) Apply CK as a pulse (RZ waveform).
- (4) Change the write data after each access operation.
- (5) If there is a test-mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)
- (6) After creating a test pattern, always confirm its functionality through logic simulation. When simulated, the test pattern will produce an output during a dummy event (old data) and an output during a write event (write-through data). However, because these outputs do not need to be verified, we recommend that they be rewritten to indeterminate values before being interfaced to the tester.

Figure 8-7 Procedure for Creating Test Patterns for High-density-type 1-port RAM

8.4.3 High-Density-Type Dual-Port RAM

For high-density-type dual-ported RAM, as for Basic-cell-type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (Epson will use the test-state test patterns as templates as it creates dedicated RAM test patterns.) (For details, refer to Section 8.4.1, “Basic-Cell-Type RAM.”)

When creating test-state test patterns for high-density-type dual-ported RAM, although essentially the same procedure applies as is described in Section 8.4.2, “High-Density-Type 1-Port RAM,” please follow the specific procedure described below, so that test patterns will be created separately (depending on how the ports are used).

- (1) When using as dual-ported RAM (reading and writing on both ports A and B), create the following two test patterns:
 - Test pattern 1: Write from port A, read from port A
 - Test pattern 2: Write from port B, read from port B
- (2) When using as 2-port RAM (writing on port A, reading on port B), create the following (one) test pattern.
 - Test pattern 1: Write from port A, read from port B
- (3) When using as 3-port RAM (reading and writing on port A, reading on port B), create the following two test patterns:
 - Test pattern 1: Write from port A, read from port A
 - Test pattern 2: Write from port A, read from port B

* To prevent possible simultaneous access of the same address, please avoid writing the same test pattern for test patterns 1 and 2.

8.4.4 Large-Capacity-Type RAM

For large-capacity-type RAM, as for Basic-cell-type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (The test-state test patterns become a template which Epson will use as it creates dedicated RAM test patterns.) (For details, refer to Section 8.4.1, “Basic-Cell-Type RAM.”)

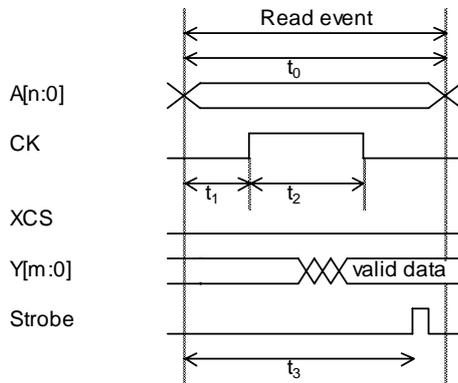
Regarding test-state test patterns for the large-capacity-type RAM, essentially the same procedure applies as is described in Section 8.4.2, “High-Density-Type 1-Port RAM.”

8.4.5 Mask ROM

For mask ROM, as for Basic-cell-type RAM, please incorporate a test circuit which can be accessed directly from external pins and create test patterns in both normal and test states. (For details, refer to Section 8.4.1, “Basic-Cell-Type RAM.”)

When creating the mask ROM test-state test patterns, please follow the procedure described below in order to ensure that data can be read out from all addresses.

• Timing chart



Recommended values for t_0 - t_3 : $t_0 = 200$ ns, $t_1 = 20$ ns, $t_2 = 100$ ns, $t_3 = 185$ ns

• Example for APF format (16 words x 4 bits)

```

$RATE 200000
$STROBE 185000
$RESOLUTION 0.001ns
$NODE
IA3 I 0
IA2 I 0
IA1 I 0
IA0 I 0
ICK P 20000 120000
IXCS I 0
...
OY3 O
OY2 O
OY1 O
OY0 O
$ENDNODE

$PATTERN
# AAAACX...YYYY
# 3210KC...3210
# S
0 0000P0...LLHH
1 0001P0...LLHL
2 0010P0...LLLL
3 0011P0...LHLL
...
12 1100P0...HHHL
13 1101P0...HHLH
14 1110P0...HLHH
15 1111P0...LHHH
$ENDPATTERN
    
```

Be sure to write all I/O pins to ensure that simulations are performed.

- (1) Perform read operations on all addresses, based on the read event shown above. Addresses may be changed in any order, as desired.
- (2) CK must be applied as a pulse (RZ waveform). There is no need to stop the clock.
- (3) If there is a test-mode setup sequence, be sure to insert it prior to event 0. (Event numbers need to be reassigned.)

Figure 8-8 Procedure for Creating Mask ROM Test Patterns

8.5 Memory BIST Design

The S1K70000 series comes equipped with a memory self-diagnostic circuit called the “Memory BIST (Built-In Self-Test),” which may be used as a test circuit for testing the LSI’s internal memory. Use of the memory BIST provides numerous advantages, including those specified below.

- Eliminates the need for customers to design a memory test circuit
- Allows the number of external pins for memory testing to be reduced
- Capable of testing memory at an actual high operating speed
- Allows the time required for memory testing using an LST tester to be reduced

In addition, it offers versatile optional functions such as a bypass circuit (transparent circuit) for memory inputs, as a means of increasing fault detection rates for the entire chip.*1

Note *1: If fault detection rates are to be increased, the LSI must be modified so as to be suitable for SCAN testing following the insertion of a bypass circuit. If it is necessary to make the entire chip suitable for SCAN testing, a bypass circuit must also be optionally included in the memory BIST.

8.5.1 Outline of the Memory BIST Circuit Block

The memory BIST generates a circuit known as a “collar” in the periphery of the memory, and a circuit known as a “controller” that controls the collar. If multiple pieces of memory are included, multiple collars are generated that can be controlled by a single controller (for purposes of overhead reduction).

In addition, a bypass circuit or a fault diagnosis function may be added to inputs for memory as necessary. Under no circumstances can the number of elements inserted for memory inputs exceed the number of multiplexer stages, however. When the memory BIST is inserted, a circuit block becomes similar to that depicted in Figure 8-9, and a bypass circuit becomes similar to that depicted in Figure 8-10 (in both, memory BIST design is applied to synchronous-type RAM).

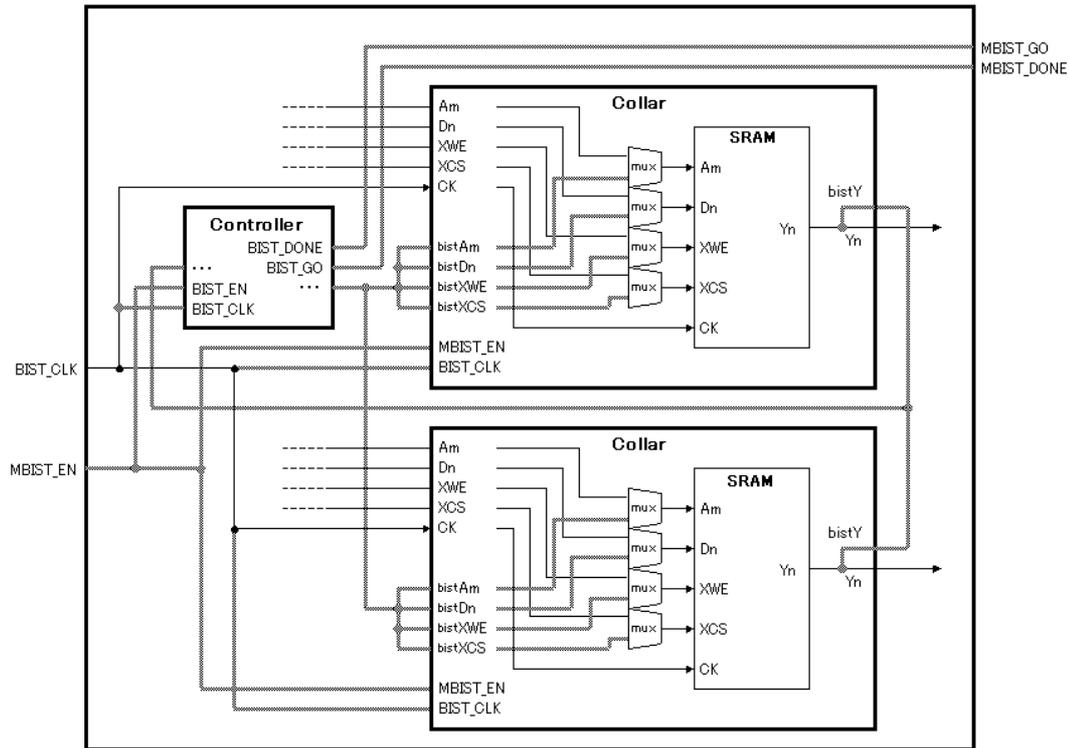


Figure 8-9 Block Diagram After Insertion of the Memory BIST Circuit

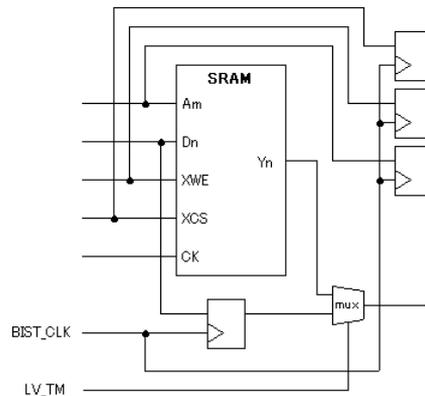


Figure 8-10 Bypass Circuit

8.5.2 Outline of the Memory-BIST-Circuit Test Sequence

Memory testing is started by applying a clock to the memory BIST and memory devices, and driving the enable signal (MBIST_EN) from Low to High. Immediately after testing begins, the test judge signal (MBIST_GO) goes High and the test end signal (MBIST_DONE) goes Low. Provided that the test is performed normally, the judge and end signals do not change state until completion of the test. Conversely, if any problem is encountered in the test, the judge signal goes Low (once the judge signal has gone Low, it never returns High). Testing is completed when the end signal goes High. If the judge signal is held high at this time, the test has terminated normally; if it is held Low, a problem has been encountered in the test. The test sequence of the memory BIST is similar to that depicted in Figure 8-11.

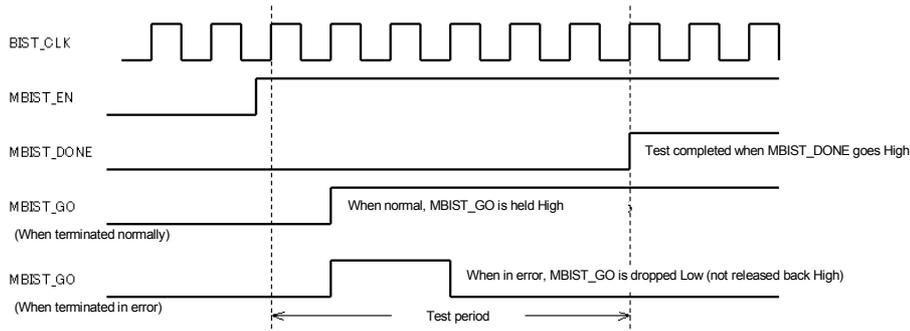


Figure 8-11 Test Sequence of the Memory BIST Circuit

8.5.3 Types of Memory Suitable for Memory BIST

The types of memory available from Epson that are suitable for the memory BIST are listed below.^(*2)

- Synchronous 1-port/2-port SRAM of the basic cell type
- Synchronous 1-port/dual-port SRAM of the high-density type
- One-port SRAM of the large-capacity type
- Synchronous mask ROM^(*3)

Note *2: Certain types of memory other than those listed above are suitable for BIST. For more information, contact the sales division of Epson.

*3: For mask ROM, if ROM data is modified, the BIST circuit must be regenerated, as it contains the expected signed values.

8.5.4 Estimating the Memory BIST Circuit Size

The circuit size of the memory BIST circuit varies significantly depending on the type and number of SRAMs, the test configuration, the BIST-circuit options, and the limitations on logic synthesis. For more information, contact the sales division of Epson. For estimates, refer to Table 8-3, which lists the typical memory BIST circuits and circuit sizes in the respective cases.

Table 8-3 Circuit Sizes of Typical Memory BIST Circuits

Typical Memory Configuration	Number of Pcs.	Number of Collar Gates	Number of Controller Gates	Total
Synchronous 1-port 1024 words x 8 bits	5	1210	1553	2763
Synchronous 1-port 1024 words x 8 bits	10	2420	1723	4143
Synchronous 1-port 1024 words x 8 bits	20	4840	1888	6728
Synchronous 1-port 1024 words x 8 bits	40	9680	2219	11899
Synchronous 1-port 1024 words x 32 bits	5	2970	3471	6441
Synchronous 1-port 1024 words x 32 bits	10	5940	4081	10021
Synchronous 1-port 1024 words x 32 bits	20	11880	4624	16504
Synchronous 1-port 1024 words x 32 bits	40	23760	5766	29526
Synchronous Dual-port 1024 words x 8 bits	5	2500	1571	4071
Synchronous Dual-port 1024 words x 8 bits	10	5000	1745	6745

Typical Memory Configuration	Number of Pcs.	Number of Collar Gates	Number of Controller Gates	Total
Synchronous Dual-port 1024 words x 8 bits	20	10000	1910	11910
Synchronous Dual-port 1024 words x 8 bits	40	2000	2254	22254
Synchronous Dual-port 1024 words x 32 bits	5	6335	3491	9826
Synchronous Dual-port 1024 words x 32 bits	10	12670	4102	16772
Synchronous Dual-port 1024 words x 32 bits	20	25340	4646	29986
Synchronous Dual-port 1024 words x 32 bits	40	50680	5802	56482

- The number of gates shown above is the result of logic synthesis performed using the Basic Cell-type MSI cell.
- In each case, the circuit is configured with a single controller.
- In each case, a bypass circuit (for SCAN testing) is added.
- If 1-port and dual-port memory coexist, estimate the necessary number of gates by adding up both gate numbers for collar gates, or using dual-port gate number alone for controller gates.

8.5.5 About Memory BIST Circuit Design

At Epson, memory BIST is inserted for the RTL or gate-level netlists received from customers. To facilitate this operation, customers will be requested to exercise caution in the design of a circuit, as described below.

1) Test input/output pins for the memory BIST

In memory BIST, BIST_CLK is normally substituted for by the memory clock (system clock). Therefore, the test input/output pins required for the memory BIST are basically the following three (*3):

- MBIST_EN (mode set signal): Input pin ... *Dedicated pin recommended* (or can be shared with another pin if the necessary conditions are met)
- MBIST_GO (test judge signal): Output pin ... Can be shared with another pin
- MBIST_DONE (test end signal): Output pin ... Can be shared with another pin

Furthermore, if a bypass circuit is optionally included, the pin specified below is required. However, this pin is unnecessary if it is separately assigned when the entire chip is made suitable for SCAN testing.

- LV_TM (SCAN-mode set signal): Input pin ... Can be shared with the SCAN-mode set pin for the entire chip

To facilitate design, we recommend that MBIST_EN be provided as a dedicated pin. If it is necessary that MBIST_EN be shared with another pin, the entire circuit, including the customer's circuit, must be configured so as to satisfy the following initialization requirements:

- Memory BIST can be set to MBIST_EN = 0 (normal-operation mode) and BIST_CLK (= memory clock) can be applied to at least two pulses.
- After the above operation has been conducted, the memory BIST can be set to MBIST_EN = 1 (BIST mode) and BIST_CLK (= memory clock) can be applied continuously.

2) Restrictions during normal operation

Circuits are added in the periphery of memory when memory BIST is applied, and this peripheral circuit must be initialized in normal operation, not just in BIST mode (unless it is initialized, the memory cannot be accessed during simulation).

Therefore, the entire circuit, including the customer's circuit, must be configured so as to satisfy the following initialization requirements (*4):

- Memory BIST can be set to MBIST_EN = 0 (normal-operation mode) and BIST_CLK (= memory clock) can be applied to at least two pulses.

3) Skew adjustment of the memory clock

Because the memory BIST circuit (collars and controller) is comprised of multiple sequential circuits, clock skews must be adjusted between the memory's clock signal and the clock signals for the internal flip-flops of the BIST circuit (collars and controller). Therefore, make sure the clock for the memory to which memory BIST is to be applied is designed for optimization by Clock Tree Synthesis. For more detailed contents of the design, refer to the application cases described below.

- (1) If multiple system clocks are associated with memory operation in the circuit, clock skews are generally adjusted by assigning one BIST controller to each clock (multiple BIST controllers as a whole). In such a case, the circuit must be configured so as to allow clock skews to be adjusted individually for each memory clock.
- (2) Even when multiple system clocks are associated with memory operation in the circuit, if the clocks can be integrated into one line for operation in BIST mode, the memory BIST circuit can be configured with a single BIST controller. In such a case, the circuit must be configured so as to allow clock skews to be adjusted for all memory clocks in BIST mode.
- (3) In cases in which multi-port memory has different clocks for the respective ports, the clock skews must be adjusted using a multiplexer. In such a case, insert a multiplexer for clocks other than the selected clock.

Note *3: Although the BIST circuit requires BIST_CLK as its clock input when operating singly, BIST_CLK can normally be substituted for by the memory clock (system clock) or other internal clock, as initialization, skew adjustment, and the like are required. Furthermore, if the BIST circuit is configured with multiple BIST controllers, there must be as many MBIST_GO and MBIST_DONE outputs as the number of BIST controllers. For MBIST_EN input, however, a single input will suffice.

*4: This circuit configuration can also include initialization of the customer's own circuit. If the required circuit configuration cannot be designed, contact the sales division of Epson.

8.5.6 Other

- Memory BIST can be applied without concern for the restrictions associated with hierarchical design, regardless of where in the customer's circuit memory exists.
- It does not matter whether the customer's circuit contains memory for which memory BIST is applied or memory for which memory BIST is not applied.

- Before memory BIST can be inserted, customers will be requested to furnish Epson with temporary RTL or temporary netlists for the purpose of preliminary examination. A period of approximately three days is required for preliminary examination. Following completion of preliminary examination, a period of approximately one day is required for insertion of the BIST circuit. Furthermore, to facilitate insertion of memory BIST, customers are requested to present the checksheet attached herein, along with said temporary RTL or temporary netlists.

● **Checksheet**

- (1) Have you prepared an outline drawing of the circuit blocks? Yes/No
- (2) Have you specified the cells for memory BIST in the circuit? Yes/No
- (3) Have you integrated memory clocks into one line for the purpose of BIST? Yes/No
(However, this is not an essential requirement.)
- (4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? Yes/No
- (5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock *

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

- (6) Test-pin information

Pin Name	External Pin Name, etc.
BIST_CLK	Shared-input-pin name: Clock net name: , Instance name of module: Mode setting:
MBIST_EN	Dedicated-input-pin name: Net name:
MBIST_GO	Shared-output-pin name: Instance name of MUX:
MBIST_DONE	Shared-output-pin name: Instance name of MUX:

● **Explanation of the checksheet**

- (1) Outline drawing of circuit blocks

Prepare an outline drawing for memory-clock-related circuits, like the one shown in Figure 8-12.

- When using separate memory clock lines (with clocks for multi-port memory used in common)
- When combining memory clocks into a single line (with clocks for multi-port memory used in common)

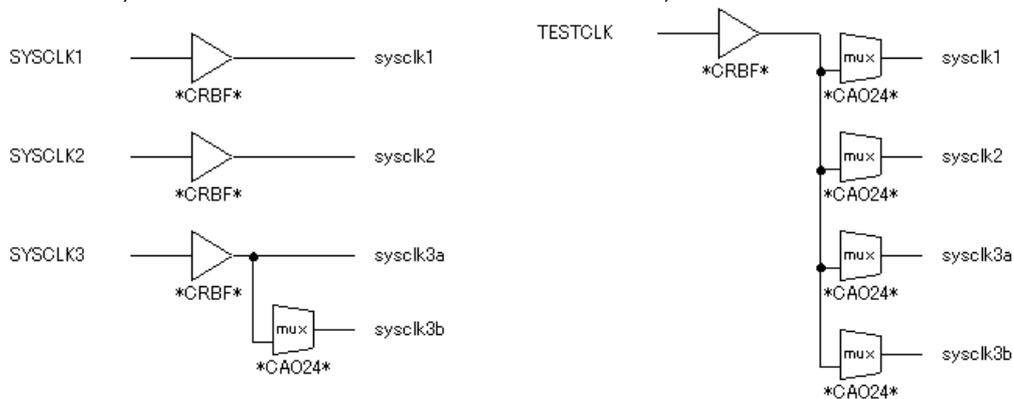
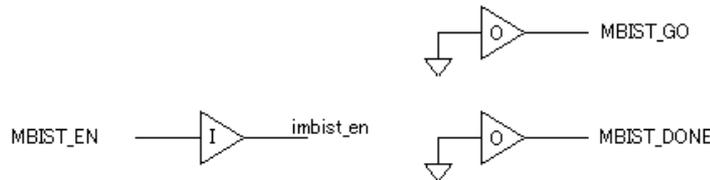


Figure 8-12 Outline Block Diagram

(2) Circuit description

In the design of a circuit, specify the dedicated memory BIST pins and multiplexers for shared pins in the RTL or netlist. At this time, make sure the dedicated input pins have their outputs written as “open,” and that the dedicated output pins have their inputs written as “pull-down.” Similarly, make sure the multiplexers for shared pins have their select signal written as “MBIST_EN” and their inputs on the BIST side written as “pull-down.” Figure 8-13 shows an image of a circuit description.

- When MBIST_EN, MBIST_GO, and MBIST_DONE are used as dedicated pins



- When MBIST_EN is used as a dedicated pin and MBIST_GO and MBIST_DONE are used as shared pins

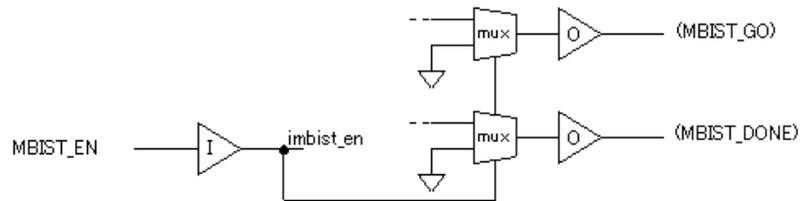


Figure 8-13 Image of a Circuit Description

(3) Memory clocks integrated into one line for the purpose of BIST

If the circuit uses multiple memory clocks and is configured so as to integrate those clocks into one line for operation in memory BIST mode, please notify Epson to that effect. In addition, provide detailed information on it in (5) and (6) below.

(4) Clocks for multi-port memory multiplexed for the purpose of BIST

If the circuit has multi-port memory, it is necessary that clocks for the respective ports be equal; otherwise, the clocks must be multiplexed for operation in memory BIST mode. If you’ve multiplexed these clocks, please notify Epson to that effect. In addition, provide detailed information on it in (5) and (6) below.

(5) SRAM information

Provide information on the SRAM as shown in the checksheet description examples below.

(6) Test-pin information

Provide information on the test pin as shown in the checksheet description example below.

● **Checksheet description example 1: Memory clocks integrated into one line (Multi-port memory clocks multiplexed)**

- (1) Have you prepared an outline drawing of the circuit blocks? Yes/No
- (2) Have you specified the cells for memory BIST in the circuit? Yes/No
- (3) Have you integrated memory clocks into one line for the purpose of BIST? Yes/No
(However, this is not an essential requirement.)
- (4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? Yes/No
- (5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock*
1-port 1024 words x 8 bits	top.sys1.sram1	sysclk1
1-port 1024 words x 8 bits	top.sys1.sram2	sysclk1
1-port 1024 words x 8 bits	top.sys2.sram3	sysclk2
1-port 1024 words x 8 bits	top.sys2.sram4	sysclk2
Dual-port 512 words x 16 bits	top.sys3.sram5	sysclk3a, sysclk3b

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

(6) Test-pin information

Pin Name	External Pin Name, etc.
BIST_CLK	Shared-input-pin name: TESTCLK Clock net name: sysclk1; , Instance name of module: sys1 Clock net name: sysclk2; , Instance name of module: sys2 Clock net name: sysclk3a and sysclk3b; , Instance name of module: sys3 Mode setting: TEST = 1, MBIST_EN = 1, with clocks integrated into one and multiplexed
MBIST_EN	Dedicated-input-pin name: MBIST_ENABLE Net name: imbist_en
MBIST_GO	Shared-output-pin name: SIGNAL1 Instance name of MUX: go_mux
MBIST_DONE	Shared-output-pin name: SIGNAL2 Instance name of MUX: done_mux

● **Checksheet description example 2: Memory clocks not integrated into one (Multi-port memory clocks multiplexed)**

- (1) Have you prepared an outline drawing of the circuit blocks? Yes/No
- (2) Have you specified the cells for memory BIST in the circuit? Yes/No
- (3) Have you integrated memory clocks into one line for the purpose of BIST? Yes/No
(However, this is not an essential requirement.)
- (4) Have you multiplexed clocks for multi-port memory for the purpose of BIST? Yes/No
- (5) SRAM information

Memory Type	Instance Name of Memory	Net Name of Memory Clock*
1-port 1024 words x 8 bits	top.sys1.sram1	sysclk1
1-port 1024 words x 8 bits	top.sys1.sram2	sysclk1
1-port 1024 words x 8 bits	top.sys2.sram3	sysclk2
1-port 1024 words x 8 bits	top.sys2.sram4	sysclk2
Dual-port 512 words x 16 bits	top.sys3.sram5	sysclk3a, sysclk3b

*: If you've integrated clocks into one line or multiplexed clocks for the purpose of BIST, clearly specify the BIST mode.

- (6) Test-pin information

Pin Name	External Pin Name, etc.
BIST_CLK	Shared-input-pin name: SYSCLK1 Clock net name: sysclk1; , Instance name of module: sys1 Mode setting: None
	Shared-input-pin name: SYSCLK2 Clock net name: sysclk2; , Instance name of module: sys2 Mode setting: None
	Shared-input-pin name: SYSCLK3 Clock net name: sysclk3a, sysclk3b; , Instance name of module: sys3 Mode setting: MBIST_EN = 1, with clocks multiplexed
MBIST_EN	Dedicated-input-pin name: MBIST_ENABLE Net name: imbist_en
MBIST_GO	Shared-input-pin name: SIGNAL1 Instance name of MUX: go_mux1
	Shared-input-pin name: SIGNAL2 Instance name of MUX: go_mux2
	Shared-input-pin name: SIGNAL3 Instance name of MUX: go_mux3
MBIST_DONE	Shared-input-pin name: SIGNAL4 Instance name of MUX: done_mux1
	Shared-input-pin name: SIGNAL5 Instance name of MUX: done_mux2
	Shared-input-pin name: SIGNAL6 Instance name of MUX: done_mux3

8.6 Function Cell Test Circuits

If function cells are used, a huge number of test patterns and a large amount of time are needed to confirm the operation of the entire circuit (including the customer's circuit). For this reason, customers are requested, as in the case of RAM, to design a test circuit so as to enable the function cells and the user circuit to be operated singly for the confirmation of circuit operation.

Please take the notes described below into consideration in the design of a test circuit. For more information, consult the Function Cell Design Guide.

8.6.1 Test Circuit Structures

- (1) Add a test circuit so as to enable the function cells to be individually separated from the user circuit and measurements to be taken for each block, with the pins of the function cells led out to the IC's external pins.
- (2) Even when inputs for the function cells are fixed to V_{SS} or V_{DD} , install a test circuit to allow inputs for testing.
- (3) Even when the output pins of the function cells are unused, install a test circuit to enable all outputs of the function cells to be observed from the IC's external pins.
- (4) Do not combine the multiple output or input pins of the function cells for use as a single test-shared pin.
- (5) Do not use a sequential circuit in the test circuit you are generating to test the function cells.
- (6) Do not invert the input signals from the test input pins before they are supplied to the function cells. Nor can the output signals of the function cells be inverted before they are forwarded to the test output pins.
- (7) If the input and output pins of the function cells are led out directly, as with the IC's pins, there is no need to install a test circuit.

8.6.2 Test Patterns

Broadly classified, the following are the three types of test patterns:

- 1) Test patterns for testing only the user circuit
- 2) Test patterns for testing the entire circuit
- 3) Test patterns for testing only the function cells

Of these test patterns, customers are requested to generate test patterns 1) and 2). It is not necessary for customers to generate test patterns 3). Existing test patterns at Epson will be used.

Note, however, that the function cell test patterns (Epson's test patterns) cannot be used by customers.

8.6.3 Test Circuit Data

This information is required when the function cells are tested during simulation and shipping inspection. Please provide Epson with the following information on your test circuit:

- (1) Clearly specify which pins of the IC are connected to which function cell pins in test mode.
- (2) If the test circuit is configured so as to enable multiple function cells to be tested on a single test pin, clearly specify the relationship between test modes and the function cell names selected.
- (3) In particular, if multiple instances of the same function cell are used, assign the function cell names in the drawing serial numbers and clearly specify which function cells are connected to the test pin.
- (4) Clearly specify how the circuit can be switched to test mode.

If function cells are used in your circuit, be sure to consult the Function Cell Design Guide in addition to this manual.

8.7 Scan Design

To prevent defective products from becoming mixed into the market, devices must be tested using test patterns that activate logic for testing. For large designs, however, this test method requires a huge number of man-hours. Scan design provides one means of solving this problem. When generating test patterns with increased fault detection rates, it is helpful to base design on certain rules and the execution of ATPG (Auto-Test-Pattern Generation).

This chapter describes the design rules to be followed in order to make the circuit suitable for scan testing (hereinafter referred to as “scan”) and to use the ATPG service from Epson. Because the implementation of scan is greatly affected by the design configuration, it is important to follow these rules from the beginning in the design of a circuit. If any design contrary to these rules is included, the purposes of ATPG may be impaired and customers may therefore be unable to use this service.

8.7.1 About the Scan Circuit

All registers (D-FFs, JK-FFs) included in your design are converted to scan-type registers in order to create a scan path (full-scan design). Then, through the use of this design, ATPG (Auto-Test-Pattern Generation) is executed. This helps to generate test patterns featuring a high fault-detection rate.

Note: The test patterns generated by ATPG are not intended for the verification of design specifications. Transparent latches are not scanned.

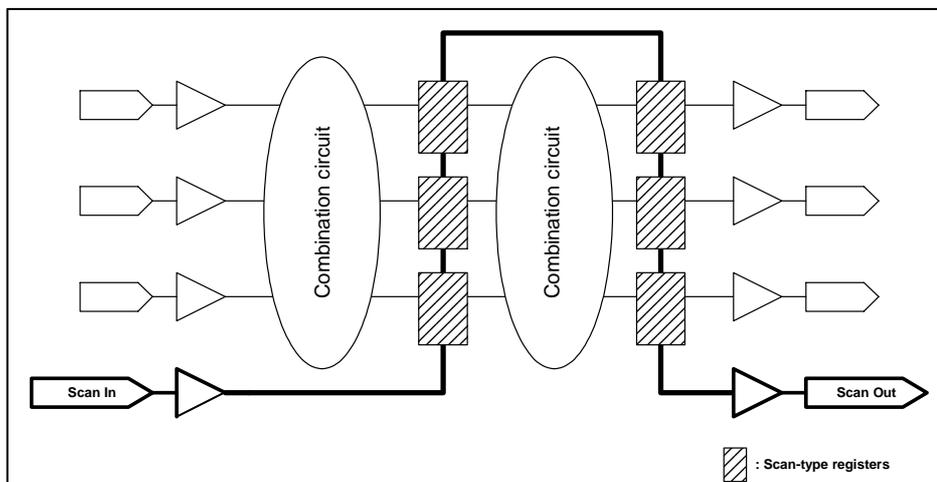


Figure 8-14 Example of a Scan Circuit

8.7.2 Scan Design Flow

The following shows the design flow in cases in which the circuit is scanned and ATPG is executed at Epson. To scan the circuit or execute ATPG yourself, consult the sales division of Epson.

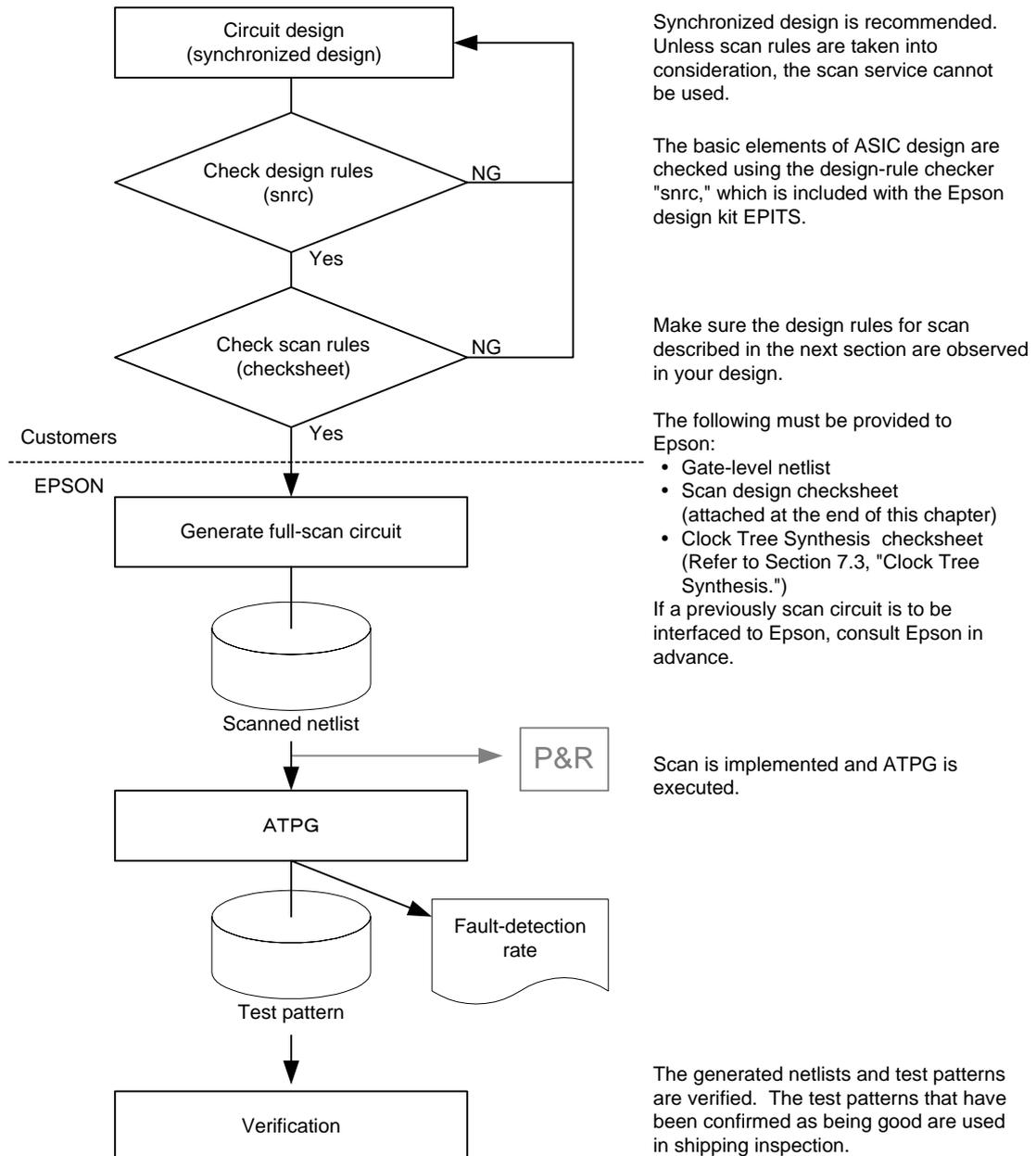


Figure 8-15 Scan Design Flow

8.7.3 Design Rules

The following section describes the design rules to be followed in order for the scan service to be used. If the desired fault-detection rate is 90% or higher, make sure all of the contents described herein are reflected in your design. In addition, when interfacing your design to Epson, make sure it is accompanied by the **Scan Design Checksheet** attached at the end of this chapter.

a. Scan external pins

For the circuit to be scanned, all of the external pins described below are required.

- Scan-enable input pin (SCANEN) [Dedicated pin]

This dedicated external input pin selects between the ordinary data path (parallel operation) and the scan path (shift operation). It cannot be shared with ordinary functions or other mode functions. Provide an input cell and external pin in the design for use as a dedicated external pin.

- Scan-data input pins [Shareable]

These external input pins are used to set data in the scan registers that have been incorporated into the design by scan. There must be several instances of these input pins corresponding to the number of scan registers. Prepare one input pin for every 300 to 500 scan registers. As many of these input pins as the number of scan-data output pins are required.

These pins may be shared with external input pins that are used in normal operation. However, clock pins, asynchronous set/reset pins, and analog signal input pins cannot be used. Note that if any pin is shared, fan-out in its net increases. Avoid sharing pins for critical paths.

The scan-data input pins are connected to the external pins at Epson during scan of the design. Please specify the external input pin names that can be used for this connection. Unless specified, pin assignments will be made by Epson.

- Scan-data output pins [Shareable]

These external output pins are used to output the observation data from the scan registers that have been incorporated into the design by scan. There must be several instances of these output pins corresponding to the number of scan registers. Prepare one output pin for every 300 to 500 scan registers. As many of these output pins as the number of scan-data input pins are required.

These pins may be shared with external output pins that are used in normal operation (two-state output pins are recommended). However, analog signal output pins cannot be used. Note that if any pin is shared, the number of cell stages in its net increases. Avoid sharing pins for critical paths.

The scan-data output pins are connected to the external pins at Epson when the design is scanned. Please specify the external output-pin names that can be used for this connection. Unless specified, pin assignments will be made by Epson.

- Scan clock input pin [Same as an ordinary clock or dedicated pin]

This clock input pin is used in the test patterns generated by ATPG. Because Epson scan cells employ the MUX scan type, this clock input pin must generally be the same system clock used in normal operation. However, if an internally generated clock exists, a dedicated clock pin for scan use may be required. For details, refer to paragraph b, "Clock design," discussed later in this section.

- ATPG enable input pin (ATPGEN) [Dedicated pin]

This external input pin activates ATPG run mode. If any design exists that requires that the state be fixed, or for the outputs of blocks (including those that become black boxes during simulation), functional macros, and RAM cells for which the internal logic becomes unstable, this pin must be used to fix (determine) the values. Unless this procedure is used, the fault-detection rate decreases considerably.

Prepare this external input pin as a dedicated pin.

b. Clock design

For the circuit to be scanned, clock design is very important. If the clock design is complicated, not only is the fault-detection rate reduced, but the generated test pattern also becomes unstable. In such a case, the intended purposes of scan and ATPG cannot be achieved. Therefore, we basically recommend synchronized design. Follow the rules described below in the design of a clock.

Keep in mind, as well, that the clock lines require optimization by CTS (Clock Tree Synthesis). For details, refer to Section 7.3, "Clock Tree Synthesis."

- Directly controllable structure from the outside [Essential]

The scan clock must propagate from an external input pin to the internal registers without being distorted in the clock waveform. Although it does not matter whether an internally generated clock is present during normal operation, there must logically be no internally generated clocks in ATPG run mode. Examples are shown in Figures 8-16 through 8-19.

Ideal clock

Shown in Figure 8.16 is an example of an ideal clock design. If the circuit is designed from the beginning in such a way that the clock for all registers is supplied from an external input pin as in this case, processing the clock lines by CTS makes it unnecessary to correct them for purposes of scan design. Because clock-line corrections affect the timing of the entire circuit, it is important to take scan design into consideration from the beginning of your design work.

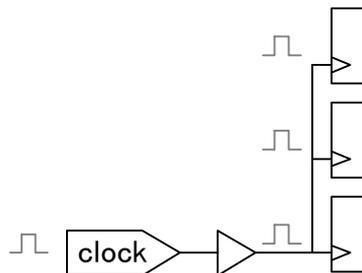


Figure 8-16 Ideal Clock

Processing of internally generated clocks 1

If an internally generated clock is used, insert a circuit that bypasses the clock-generating part (see Figure 8-17) and employ a design that applies CTS processing to ATPG run mode. However, employment of this processing requires caution, as MUX cells are added to the clock lines in that processing, which may make it difficult to adjust the timing with the clocks used for other circuit blocks.

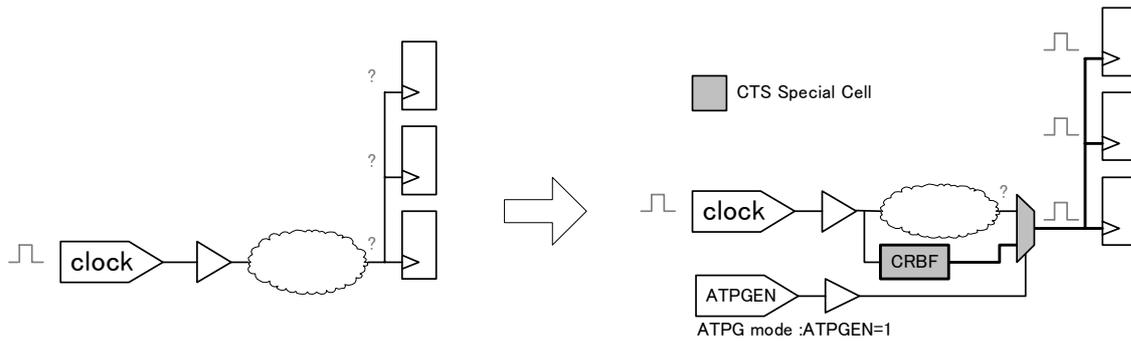


Figure 8-17 Processing of Internally Generated Clocks

Processing of internally generated clocks 2 (treatment of clock gating)

To avoid adding cells to the clock line for an internally generated clock, there is a method for controlling the enable line by which the clock signal is gated. An example is shown in Figure 8-18. Adoption of this method eliminates the need for MUX cells placed in the clock line as in Figure 8-17, and therefore helps create a design with relatively small clock skew.

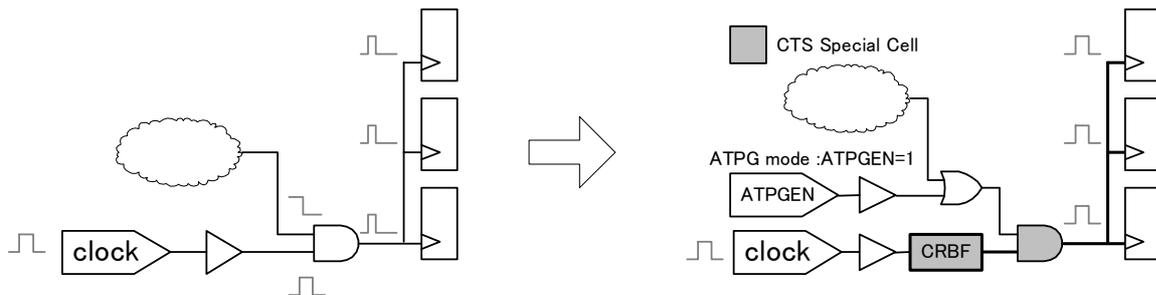


Figure 8-18 Treatment of Clock Gating

Relationship between multiple clock groups

For a design with multiple clock blocks including internally generated clocks, the usable treatment method may be limited, depending on the relationship between those clock blocks. Unless the circuit blocks using different clocks are physically interconnected, there will be no problems. However, caution must be exercised if for reasons of design specification they comprise either a false path (although physically connected, there is no logical communication during normal operation, or timing is not taken into consideration during logic synthesis) or a multi-cycle path (asynchronously communicating, with several latch misses tolerated).

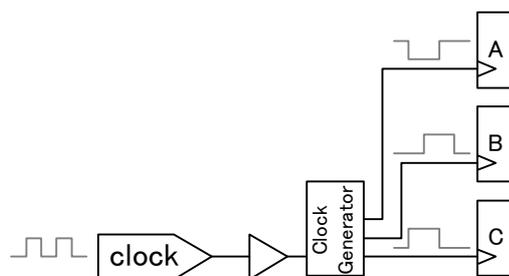


Figure 8-19 (a) Example with Multiple Internally Generated Clocks

Shown in Figure 8-19 (b) is an example of a corrective measure that can be taken in cases in which blocks A, B, and C are not physically interconnected. Because there are no physical connections, clocks can be processed collectively without causing a timing problem. If clock skews in each group are resolved by CTS, timing during ATPG run will be stabilized.

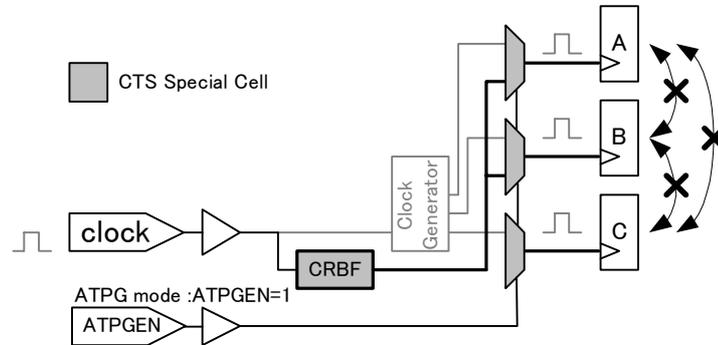


Figure 8-19 (b) Example of a Corrective Measure for Multiple Internally Generated Clocks 1 (When Blocks are Not Interconnected)

* Assumed in this example is a method that helps to efficiently create the scan chain by applying CTS processing to three clocks collectively.

However, if the blocks are physically connected, though there may be no problems from a specification perspective, corrective measures for ATPG must be taken. Figure 8-19 (c) shows an example of treatment in such a case. Because ATPG generates test patterns at random, they may cause an operation in which signals are communicated via a false path that is nonexistent in the specification. In such a case, the timings associated with the data paths between blocks A, B, and C cannot be guaranteed. Therefore, to ensure that the timings will be controlled for each internally generated clock, bypass these clocks on a one-for-one basis to external pins. In addition, *we recommend the use of dedicated pins* for these bypass clock pins. If the use of shared pins is unavoidable, the clock signals entering from those shared pins must be gated to prevent them from propagating to other than the registers (see Figure 8-19 (d)). In such a case, because the values of those nets are fixed, the fault-detection rate decreases.

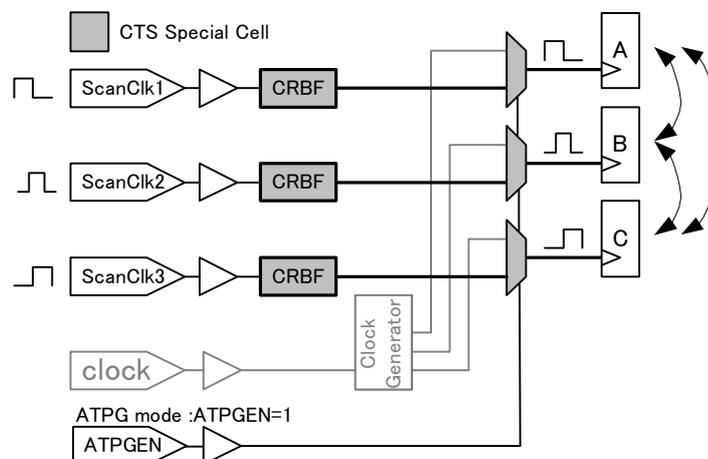


Figure 8-19 (c) Example of a Corrective Measure for Multiple Internally Generated Clocks 2 (When Blocks are Interconnected)

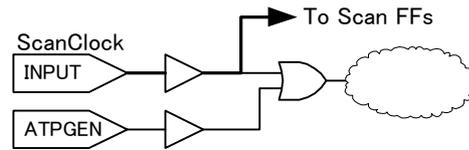


Figure 8-19 (d) Example of Scan-Clock Processing Using Shared Pins

- **As few clock lines as possible** [Recommended]

If multiple clocks exist as in the above case, the amount of work to be performed by customers will increase, such as due to the need to change or add a design or an increase in the number of timing reverification items. Furthermore, the presence of multiple clocks may cause the length of test patterns to increase or the fault-detection rate to drop. Reduce the number of clock blocks as much as possible in design. This should help increase the efficiency of work when testing is conducted later.

- **Minimized coexistence of rising and falling edges of a clock** [Recommended]

If both rising and falling edges are used in each clock, the efficiency of scan operation and ATPG run may decrease. In some cases, the fault-detection rate may drop. We recommend that scan clocks be designed using only one edge as much as possible.

- **Completely separated scan-clock signals and data signals** [Recommended]

Make sure the scan-clock signals and data signals are completely separated. If the scan-clock signals affect the data lines, clock signals and data signals cannot be controlled independently of each other, and faults therefore cannot be detected.

c. Asynchronous set/reset signals of registers [Essential]

A circuit is recommended in which the asynchronous set/reset signals for the flip-flops and transparent latch cells can all be controlled directly from the outside. When asynchronous set/reset signals internally generated in the design are used, take the following into consideration:

- The signals cannot be asserted (= made active) for at least the period for which scanning remains enabled.
- When internally generated asynchronous set/reset signals are used, make sure they are fed directly from the flip-flop outputs without being routed via combinational circuits, to ensure that minimum pulses will not occur. If signals routed via combinational circuits are used, take the appropriate corrective measure by, for example, using gray code.

* Unless such a corrective measure is taken, problems such as reduced fault-detection rates or unstable test patterns may occur.

d. Handling of transparent latches [Recommended]

Transparent latches are not converted into scan cells. Avoid using transparent latches as much as possible, as they are detrimental to improving the fault-detection rate.

When transparent latches are used, take the following into consideration:

- For the clock signals, take corrective measures similar to those discussed in paragraph b, "Clock design."

- Make sure the off-state levels of the transparent latches match those of other registers connected to the same clock line.

Example: Through at the Low level when the FF is for a rise operation (Return To Zero), or through at the High level when the FF is for a fall operation (Return To One)

However, if the scan clock is active on either edge or multiple instances of the scan clock exist, no improvements can be expected, depending on the design configuration. In such a case, take the corrective measure described below.

- If the above two points cannot be taken into consideration in your design, make sure the latches are fixed to the through state in ATPG run mode. At this time, care must be taken to avoid creating a feedback loop.

* Unless these corrective measures are taken, problems such as reduced fault-detection rates or unstable test patterns may occur.

e. Unusable cells or design [Essential]

In scan design, use of the cells specified below is inhibited.

<Cells the use of which is inhibited>

- RS latch cells
- Flip-flops with asynchronous set/reset functions
- Multi-bit flip-flop cells
- Scan-type flip-flops

<Circuits the use of which is inhibited>

- Combinational feedback loops (including those routed via external bi-directional pins)
- Differentiation circuits (pulse generators)
- Self-reset circuits
- Sequentially controlled ATPG mode (Use the ATPG enable input pin for control.)

* Unless these corrective measures are taken, problems such as reduced fault-detection rates or unstable test patterns may occur.

f. When using functional macros or RAM cells [Recommended]

Because in ATPG functional macros and RAM cells are handled as black boxes, it is impossible to observe the stages preceding the macros and control those following the macros. Therefore, the fault-detection rate is reduced considerably. To counteract this, we recommend inserting scanable flip-flops in locations immediately preceding and following the macro cells. This will bring about a significant improvement when the circuit is tested later (Figure 8-20 (a)). If this is impossible from a specification standpoint, add a mode in which the macros are bypassed and configure a circuit by which the output level can be fixed (Figure 8-20 (b)).

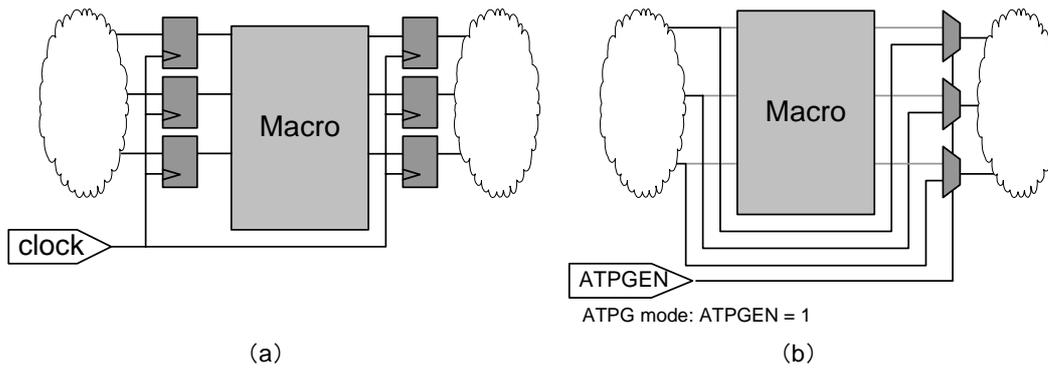


Figure 8-20 Example of Macro Cell Processing

g. Internal bus [Recommended]

Do not use bus circuits comprised of internal 3-state cells. Rather, we recommend that the circuit be designed using selector logic. When using said bus circuits, make sure they are fixed in such a way that the bus lines are not switched over and only one line is activated in ATPG run mode. (If bus circuits are used, the fault-detection rate decreases, as such circuits have fixed values.)

h. External cells with various controls [Essential]

Some types of external input and external bi-directional cells available in the S1K70000 series come equipped with various control pins. These pins must be fixed using the ATPG enable input pin. Follow the procedure described below to process these pins.

- Pull-up/pull-down control pin (PC pin)

Fix this pin to the off state using the ATPG enable input pin (ATPGEN).
(PC = 1 when ATPGEN = active)

- Gating signal (C pin)

Fix this pin to the through state using the ATPG enable input pin (ATPGEN).
(C = 1 when ATPGEN = active)

i. Other

- Approximately 7 days are required for scan work (scan insertion to verification) at Epson after netlists created in accordance with the design rules are received.
- In scan design, optimization by CTS is essential. Please make sure the **Clock Tree Synthesis Checksheet** attached in **Section 7.3, "Clock Tree Synthesis,"** is included with the netlists presented to Epson.

Scan Design Checksheet (1/2)

This checksheet includes the contents we would like you to confirm before using scan or ATPG services from Epson. Fill out this checksheet and present it to Epson. Without this checksheet, scan and ATPG services cannot be used.

Information on scan design and the results of the design check are provided below.

Date filled in: _____ (month) _____ (day) 200____

Company name: _____

Your name: _____

● Design information

➤ Top block name: _____

➤ Desired fault-detection rate: _____%

● Pin information

➤ ATPG-enable pin names and active edges (rise/fall)

Pin name 1: _____ (Rise/Fall)

Pin name 2: _____ (Rise/Fall)

Pin name 3: _____ (Rise/Fall)

➤ Scan-enable pin names and active levels (High/Low)

Pin name 1: _____ (High/Low)

Pin name 2: _____ (High/Low)

Pin name 3: _____ (High/Low)

➤ Scan-clock input-pin names and active levels (High/Low)

Pin name 1: _____ (High/Low)

Pin name 2: _____ (High/Low)

Pin name 3: _____ (High/Low)

➤ Scan-data input-pin name

Pin name: _____

➤ Scan-data output-pin name

Pin name: _____

➤ Asynchronous set/reset pin names and active levels (High/Low)

Pin name 1: _____ (High/Low)

Pin name 2: _____ (High/Low)

Pin name 3: _____ (High/Low)

Scan Design Checksheet (2/2)

● **Check items (Mark the applicable items with a check.)**

- The scan-clock pins have been treated in accordance with the design rules described in Section 8.7.3, paragraph b.
- Asynchronous set/reset signals of registers have been treated in accordance with the design rules described in Section 8.7.3, paragraph c.
- Transparent latches (Select one of the following.)
 - Not used
 - Treated in accordance with Section 8.7.3, paragraph d
 - Not treated in accordance with Section 8.7.3, paragraph d.
A reduction in the fault-detection rate is acknowledged.
 - Other: _____
- Cells or circuits the use of which is inhibited as described in Section 8.7.3, paragraph e, do not exist.
- Functional macros or RAM cells (Select one of the following.)
 - Not used
 - Treated in accordance with Section 8.7.3, paragraph f
 - Not treated in accordance with Section 8.7.3, paragraph f.
A reduction in the fault-detection rate is acknowledged.
 - Other: _____
- Internal 3-state bus (Select one of the following.)
 - Not used
 - Treated in accordance with Section 8.7.3, paragraph g
 - Not treated in accordance with Section 8.7.3, paragraph g.
A reduction in the fault-detection rate is acknowledged.
 - Other: _____
- External cells with various control pins (Select one of the following.)
 - Not used
 - Treated in accordance with Section 8.7.3, paragraph h
 - Not treated in accordance with Section 8.7.3, paragraph h.
A reduction in the fault-detection rate is acknowledged.
 - Other: _____
- Other

8.8 Boundary Scan Design

A boundary scan (JTAG) insertion service is available from Epson. When this service is used, an IEEE1149.1-compliant boundary scan circuit and a control circuit (TAP controller) are inserted in the periphery of the logic circuit. At the same time, BSDL files that contain information on those circuits are presented to customers. Because the inserted boundary-scan-function patterns are created by Epson, it is not necessary for customers to create patterns for the boundary scan circuit.

8.8.1 Boundary-Scan Design Flow

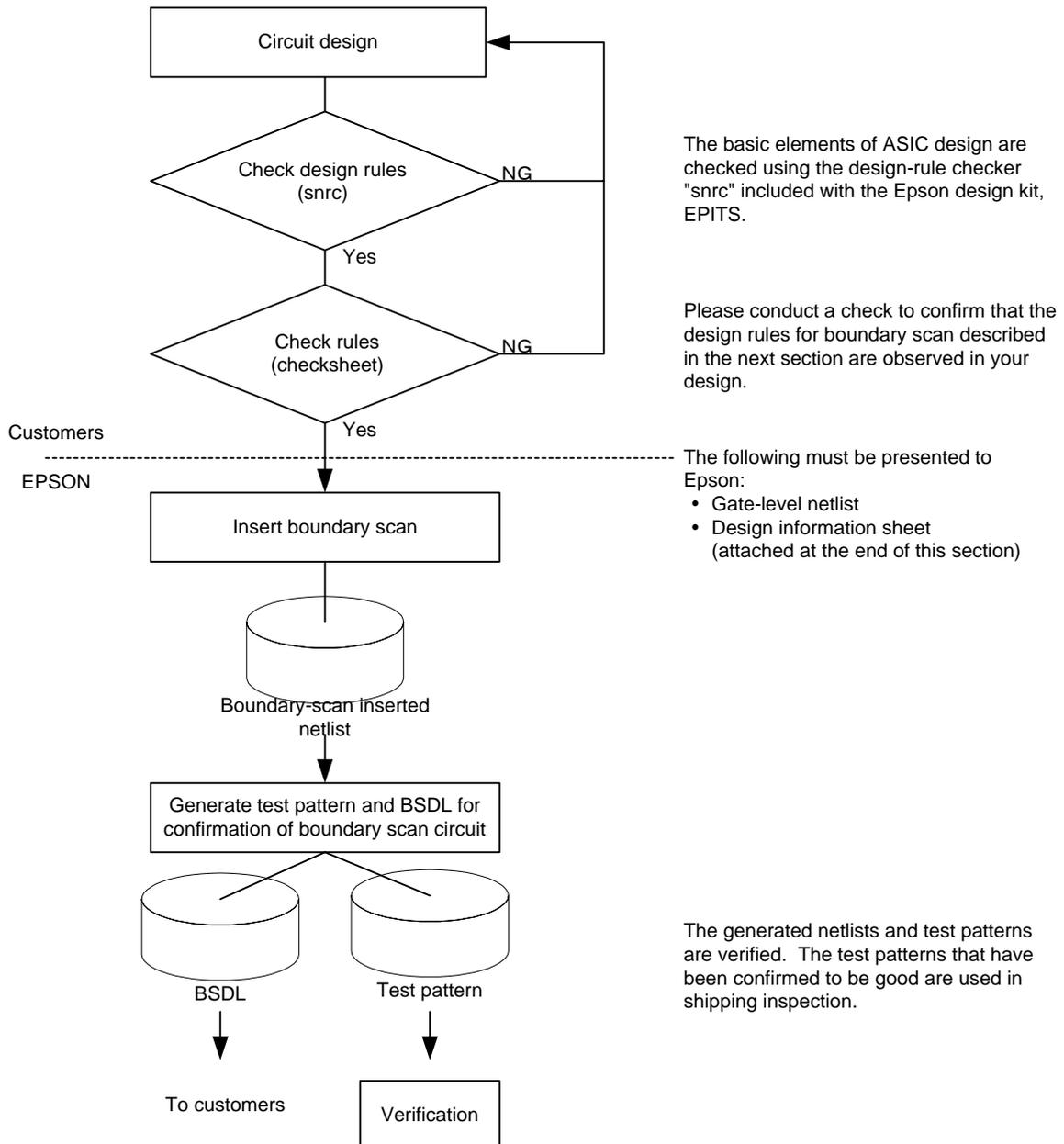


Figure 8-21 Boundary-Scan Design Flow

8.8.2 Instructions

The JTAG instructions specified below are supported.

Table 8-4 Supported Instruction Codes

Instruction	Code
SAMPLE/PRELOAD	0...10
BYPASS	1...11
EXTEST	0...00
CLAMP	Selectable as desired ^(*)
HIGHZ	Selectable as desired ^(*)
IDCODE	0...01

Note *1: Unless explicitly specified, Epson will select the appropriate code. No duplicate codes can be specified.

Instruction bit sizes may be selected in the range of 2 to 32 bits. Unless explicitly specified, Epson will determine the appropriate instruction size.

8.8.3 Estimating the Number of Gates

The extent of the increase in the number of gates as a result of boundary scan insertion depends on the ASIC series used and the instructions and bit sizes supported. Estimate the approximate number of gates using the information given below.

Table 8-5 Gate-Count Estimation (SOG Equivalent)

Boundary Scan Block	Gate Counts
TAP controllers + miscellaneous gates	Approx. 1000 (BCs)
Input pin	When using normal cells: Approx. 30 (BCs/pin) When using dedicated observation cells: Approx. 15 (BCs/pin)
Two-state output pin	Approx. 35 (BCs/pin)
3-state output pin	Approx. 65 (BCs/pin)
Bi-directional pin	Approx. 95 (BCs/pin)

8.8.4 Design Rules

For the boundary scan service to be used, it is necessary that customers' logic circuits be designed in observance of the restrictions described below. Before releasing data to Epson, please be sure to confirm the circuit information using the **Boundary Scan Checklist** attached at the end of this chapter, and to fill out and present the Design Information Sheet to Epson. Please note that if any circuit violating the restrictions exists, this service cannot be used.

a. Coexistence with DC/AC easy-to-test circuits inhibited

Coexistence with the easy-to-test circuits described in **Section 8.3, "Test Circuit Which Simplifies DC and AC Testing,"** is inhibited. To be suitable for the boundary scan service, a design cannot have DC/AC easy-to-test circuits inserted in it.

b. Character strings usable for external pins

Due to the rules for the BSDL file format, external pin names are subject to the following limitations:

- Only alphanumeric characters (a to z, A to Z, 0 to 9) and the underscore (_) can be used.
- The characters are not case-sensitive (for example, CLK and clk are assumed to be the same).
- The first character must always be a letter (for example, 0CLK and _CLK are not accepted).
- The underscore cannot be used in succession (for example, SYS__CLK is not accepted).
- The character string cannot end with an underscore (for example, CLK_ is not accepted).

c. Preparation of dedicated external pins

The boundary scan circuit always requires five dedicated external pins. Insert these external pins in your design in accordance with the rules described below.

- Clock (TCK)

This is a clock pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected.

- Mode select (TMS)

This is a mode select pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use an input cell with pull-up.

- Data input (TDI)

This is a scan-data input pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use one with pull-up.

- Data output (TDO)

This is a scan-data output pin for the boundary scan circuit. Use a 3-state output cell and confirm that its input port is tied low to GND.

- Reset (TRST)

This is an asynchronous reset pin for the boundary scan circuit. Prepare an input cell and confirm that its output port is not connected. For this input cell, use one with pull-up.

```
IBC U1 (.PAD(TCK) );           // IBC:      Normal input cell
IBCP1 U2 (.PAD(TMS) );        // IBCP1:   Input cell with pull-up
IBCP1 U3 (.PAD(TDI) );
IBCP1 U4 (.PAD(TRST) );
TB1 U5 (.PAD(TDO), .A(1'b0), .E(1'b0) ); // TB1:     3-state output cell
```

Figure 8-22 Example of Dedicated-Pin Description (Written in verilog)

d. Regarding hierarchical blocks

Make sure the hierarchical blocks in the netlist are configured as shown below. Note that, following boundary scan insertion, hierarchical blocks such as a TAP controller are added.

- Place I/O cells in the top block.
- Place other logic cells in a sub-block one layer below that as much as possible.

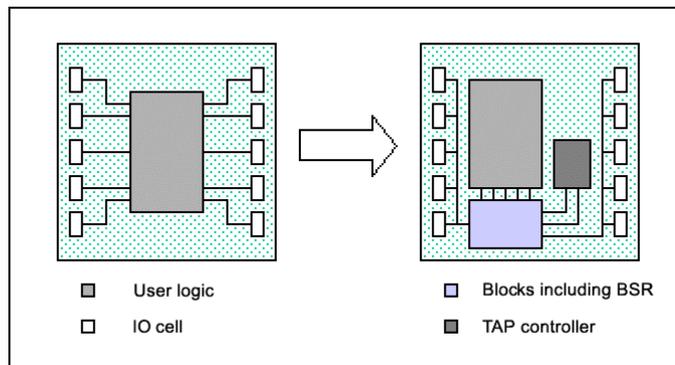


Figure 8-23 Image of a Hierarchical Block Configuration

e. Regarding I/O-cell types

If the design includes one of the following types of I/O cells, the boundary scan service cannot be used:

- I/O cells with test mode
- Gated input cells
- Open-drain output cells
- I/O cells with pull-up/pull-down resistor

f. External pins handling analog signals

Boundary scan cells are not inserted for oscillation-circuit input/output pins or external pins that handle analog signals.

g. Multibonding and multipads

If the design includes multibonding or multipads, the boundary scan service cannot be used.

Boundary Scan Checksheet

Please confirm the check items listed below before interfacing to Epson, and present the Design Information Sheet shown on the next page to Epson. Please note that if any circuit violating these check items exists or any information is omitted, the boundary scan service cannot be used.

Please confirm the following items before presenting netlists to Epson:

- (a) The supported range of instructions complies with Table 8-4.
- (b) The circuits described in Section 8.3, “Test Circuit Which Simplifies DC and AC Testing,” cannot coexist.
- (c) Confirm that the external pin names comply with Section 8.8.4, paragraph b “Character strings usable for external pins.”
- (d) Regarding dedicated pins
 - (i) Conduct a check to confirm that five dedicated pins already exist in the netlist.
 - (ii) For the TMS, TDI, and TRST equivalent pins, use input cells with pull-ups.
 - (iii) For the TDO equivalent pin, use a 3-state output cell.
 - (iv) Conduct a check to confirm that the dedicated pins are not shared with any other functions.
- (e) Place I/O cells in the top layer.
- (f) Do not use the I/O cells listed in Section 8.8.4, paragraph e.
- (g) Boundary scan cells cannot be inserted for oscillation-circuit input/output pins or external pins that handle analog signals.
- (h) Conduct a check to confirm that multibonding and multipads are not used.

Design Information Sheet

(Fill out this sheet and present it to Epson by the time the design is released.)

Information on boundary scan design is provided below.

Date filled in: _____ (month) _____ (day) 200____

Company name: _____

Your name: _____

● Design information

➤ Top block name: _____

- | | |
|---|--|
| 1. Desired instructions
(Select the desired instructions.) | <input checked="" type="checkbox"/> Essential instructions → Codes comply with Table 8-4.
<input type="checkbox"/> CLAMP instructions → Your desired code _____ ^(*1)
<input type="checkbox"/> HIGHZ instructions → Your desired code _____ ^(*1)
<input type="checkbox"/> IDCODE instructions → Codes comply with Table 8-4. |
|---|--|

- | | |
|---|--|
| 2. Instruction bit size
(Select the desired size.) | <input type="checkbox"/> Not specified → Determined by Epson
<input type="checkbox"/> Specified → Bit size _____ bits ^(*2) |
|---|--|

3. Selection of boundary scan cells

To choose the boundary scan cells to be inserted, supply the information specified below. Unless explicitly specified, the following will be applied at Epson:

- Dedicated observation cells may be used, if necessary, for the system clock or asynchronous reset bits.
 - Boundary scan cells will not be inserted for input and output pins handling analog signals.
- ◆ External pin names for which dedicated observation cells are used

- ◆ External pin names for which boundary scan cells are not to be inserted

- ◆ Other

- ◆ Dedicated-pin information (Enter the pin names corresponding to each pin.)

TCK: _____ TMS: _____ TDI: _____ TDO: _____ TRST: _____

- ◆ User circuit information

System clock name: _____

Asynchronous reset signal name: _____

Top block name: _____

Sub-block name^(*3): _____

Notes *1 Do not select duplicate codes for any instruction. Unless explicitly specified, codes will be assigned by Epson. In addition, make sure the bit size matches that in Item 2, "Instruction bit size."

*2 Bit sizes can be specified in the range of 2 to 32 bits.

*3 Enter all sub-blocks that exist immediately below the top block. If any buffers or delay elements inserted for delay adjustment or the like exist in the top block, enter their instance names.

Chapter 9 Test Pattern Generation

Following completion of logic design, generate test patterns. Test patterns are used not only for simulation to confirm circuit operation, but also for the shipping inspection of a product.

To improve the quality of the shipped product, take the following into account in the generation of test patterns.

9.1 Testability Consideration

Because test patterns are used for the shipping inspection of a product, they must be generated so as to enable the entire internal circuit of the LSI to be tested. If the LSI's internal circuit contains any untested part, there is a possibility of a defective product being shipped, as that part of the product cannot be tested during the shipping inspection.

Generally speaking, the entire internal circuit of the LSI cannot be tested easily. Therefore, it is important that the testability of the LSI be taken into consideration from the beginning of circuit design.

By inserting Epson-recommended test circuits in your design, the DC testing and various other conditions required for test patterns can be set easily. For details, refer to Section 8.3, "Test Circuit Which Simplifies DC and AC Testing," in Chapter 8.

9.2 Usable Waveform Modulations

Test patterns are normally comprised of logic 0s and 1s. However, when circuit operation is simulated or the circuit is tested using an LSI tester, the input waveform can have a delay inserted or its waveform changed. The following two types of waveforms can be used in the creation of test patterns.

NRZ (Non-Return-to-Zero)

Normally used for signals other than the clock. This type of waveform can change state once per test period and can be given a delay.

RZ (Return-to-Zero)

Use this for clock signals and the like. Because this type of waveform can generate a positive or negative pulse within a test period, it aids in the efficient creation of clock signals. It can be given a delay, as with NRZ.

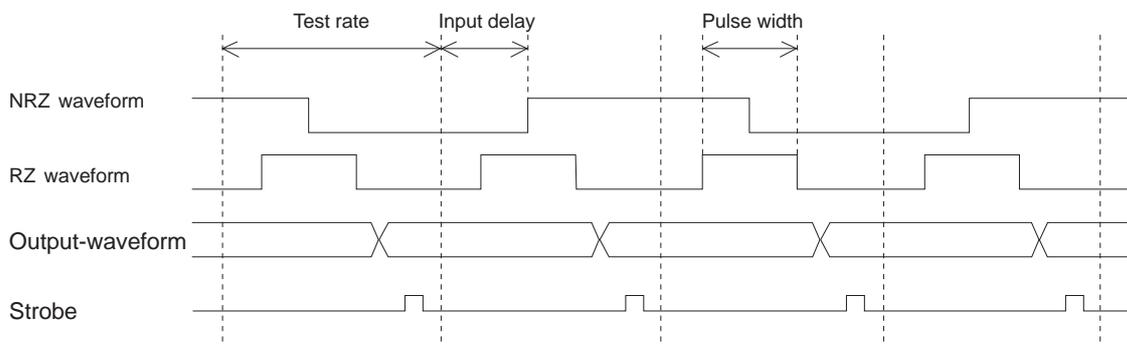


Figure 9-1 Limitations on Timing Settings

9.3 Constraints on Test Patterns

For simulation during timing design, a test pattern is used that has been set to the actual operating frequency. Because this test pattern is also used for the shipping inspection of a product, it must be adapted to the constraints of the LSI tester. Make sure the test pattern is created in conformity with the constraints described below.

9.3.1 Test Rate and Event Counts

The test rate must be 100 ns or more, in 1-ns units (the recommended period is 200 ns). Furthermore, the test period must be defined so as to satisfy the strobe constraints specified in Section 9.3.5. Note that there are constraints on the event counts of LSI testers.

Number of events per test pattern: Up to 256K events
Number of test patterns: Up to 30 patterns
Total number of events in test patterns: Up to 1M events

9.3.2 Input Delay

- (1) Range of input delays

$0 \text{ ns} \leq \text{input-delay value} < \text{strobe point}$

Define the input delay within the above range in 1-ns units. For the constraints on strobe points, refer to Section 9.3.5, "Strobes."

- (b) Phase difference in input delay

3 ns or more

- (c) Types of input delays

There may be up to 8 types of input delays in one test pattern. 0-ns delays are counted as one type. If any delay value in an RZ waveform is the same as that in an NRZ waveform, they are counted as different types. If two RZ waveforms or two NRZ waveforms, respectively, have the same delay value, they are counted as the same type.

9.3.3 Pulse Width

The pulse width in an RZ waveform must be 15 ns or more.

9.3.4 Input Waveform Format

Input waveforms can take on the values 0, 1, P, or N. The values P and N represent pulse inputs in an RZ waveform. Furthermore, the values P and N can only be defined in a combination of (0, P) or (1, N) for the same pin in one test pattern. No other combinations can be used.

For bi-directional pins, an RZ waveform can be applied only when they do not have an output state and are handled in the same way as input pins.

9.3.5 Strobes

The strobe-related constraints are as follows:

- (a) Only one type of strobe can be defined in each test pattern.
(b) The minimum value of the strobe must be such that in all events, at least 30 ns elapses after all output signals have changed state pursuant to the applied input signal.

- (c) The maximum value of the strobe must be smaller than the value of test rate – 15 ns.
- (d) Define the strobe in 1-ns units.

9.4 Notes Regarding DC Testing

Test patterns are used not only for function testing, but also for DC testing in which output voltages and the like are measured. Make sure the following items of DC testing can be performed when creating test patterns.

DC testing is conducted in order to verify the DC parameters of the LSI. Measurements for DC testing are taken at the end of a measurement event. For this reason, the measured pins cannot have their state changed in accordance with the strobe position in the measurement event.

The following items of DC parameters are measured:

- (a) Output-characteristic test (V_{OH} , V_{OL})

The current drive capability of the output buffer is measured. The measured pin is driven to an output level at which measurement can be conducted, and the value of the voltage drop that occurs when the designated current load is applied to the pin is measured.

For the output-characteristic test to be performed, the test pattern must contain all possible states in which the measured pins can operate. Furthermore, those states must be sufficiently stable that they will not change even when the test rate is infinitely extended in the measurement event.

- (b) Quiescent-current test (I_{DDS})

The quiescent current is the leakage current that flows in the power supplies of the LSI when its inputs are in a steady state. Because the amount of this current is generally very small, it must be measured while no currents other than the leakage current are flowing. To meet this requirement, all of the conditions listed below must be satisfied. Note also that the test pattern must contain at least two points of events in which the quiescent current can be measured.

- (1) All of the input pins shall be in a steady state.
- (2) A High- or Low-level signal shall be applied to or output from the bi-directional pins.
- (3) No oscillating or other operating parts shall exist in the circuit.
- (4) The internal 3-state buffer (internal bus) shall not be left floating or have no data or signal contention.
- (5) The RAM, ROM, and megacells shall not be in a current-flowing state.
- (6) A High-level signal shall be applied to the input pins with pull-up resistors.
- (7) A High-level signal shall be applied to or output from the bi-directional pins with pull-up resistors.
- (8) The bi-directional pins with pull-down resistors shall be in input mode or outputting a Low-level signal.

- (c) Input-current test

Measurements are taken of the inputs for the input buffers. The items measured in this test are the input leakage current and the pull-up/pull-down currents.

Measurements in this test are performed by applying V_{DD} - or V_{SS} -level voltage to the measured pin, and then measuring the amount of current flowing in the pin. This means that a High- or Low-level voltage is applied to the measured pin during measurement. For example, if a V_{DD} -level (High-level) voltage is applied to the measured pin while input for it is held Low, the measured pin changes state from Low to High, causing the LSI to perform an unintended operation.

For the input-current test, in an event in which input for the measured pin is held High in the test pattern, measurements must be taken by applying a V_{DD} -level voltage to the measured pin, and in an event in which input for the measured pin is held Low, measurement must be taken by applying a V_{SS} -level voltage to the measured pin. Therefore, an input-current test cannot be conducted unless the test pattern includes these states for the measured pin.

The input-current test is further classified as follows:

(1) Input-leakage-current test (I_{IH} , I_{IL})

Measurements are taken of the input currents for the input buffers without pull-up/pull-down resistors.

The current flowing in the input buffer when a High-level voltage is applied to the buffer is referred to as " I_{IH} ," and is guaranteed by the maximum current value. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held High. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held High.

The current flowing in the input buffer when a Low-level voltage is applied to the buffer is referred to as " I_{IL} ," and is guaranteed by the maximum current value. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held Low. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held Low.

(2) Pull-up current test (I_{PU})

The current flowing in the input buffer is measured using a pull-up resistor when a Low-level voltage is applied to the buffer. For this test to be conducted, the test pattern must include an event in which the input for the measured pin is held Low. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held Low.

(3) Pull-down current test (I_{PD})

The current flowing in the input buffer is measured using a pull-down resistor when a High-level voltage is applied to the buffer. For this test to be conducted, the test pattern must include an event in which input for the measured pin is held High. If the measured pin is a bi-directional pin, it must be in input mode and its input must be held High.

(4) Off-state leakage current (I_{OZ})

Measurements are taken of the leakage current flowing in the open-drain or 3-state output buffer when its output enters a high-impedance state. In this test, the measured pin is placed in a high-impedance state and measurements are taken of current values by applying a V_{DD} -level and V_{SS} -level voltage to the measured pin, respectively. Therefore, the test pattern must include an event in which the measured pin enters a high-impedance state.

9.5 Notes Regarding the Use of Oscillation Circuits

The diagrams below show examples of oscillation circuits (steady and intermittent oscillations).

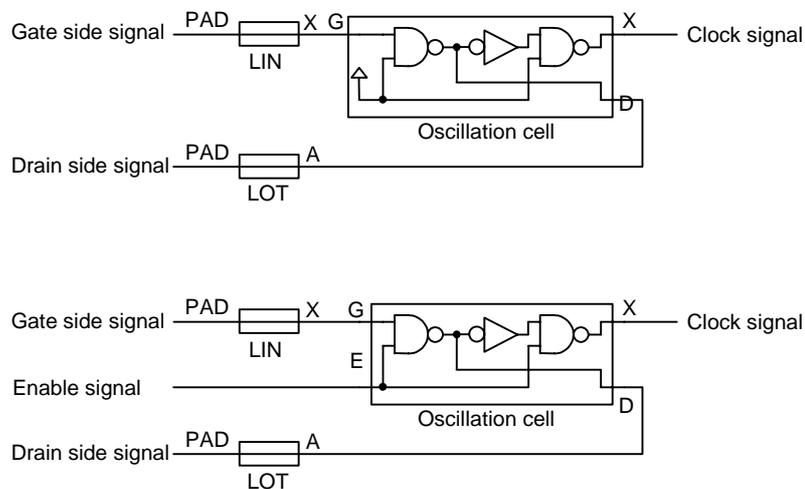


Figure 9-2 Examples of Oscillation Circuits

For systems using oscillation circuits, in general, because the oscillation inverter's drive capability is small and the oscillation circuit's output waveform is affected by the load in the measurement environment, the waveform does not precisely propagate to the gates in the stages following the oscillation circuit.

To reproduce the simulation state using a tester, therefore, a corrective measure is taken in which reverse drive is applied (i.e., by supplying a waveform to the drain pin that is in phase with the signal output to the drain).

If the oscillation inverter is comprised of an inverter, the reverse-drive signal, i.e., the signal to be entered from the drain, can be produced simply by entering a signal 180 degrees out of phase with the signal being applied to the gate. If comprised of a NAND gate (known as an "intermittent oscillator" or "Gated OSC"), however, the signal to be entered cannot easily be determined from the gate signal alone. Therefore, the reverse-drive waveform is determined based on the expected value of the drain pin.

In this method, if the input waveform is an NRZ waveform and has a strobe at the end of a test period, the expected value of the drain pin can be used directly for the input waveform to produce a reverse-drive waveform. In the case of an RZ waveform, however, the expected value of the drain pin remains High or Low regardless of whether the pin is oscillating or turned off, and a reverse-drive waveform cannot be determined by referring to the expected value of the drain pin.

For systems using intermittent oscillators, therefore, take the following into consideration:

1. Use of an RZ waveform for the input signal is inhibited.
2. The clock signal cannot have its state changed by changing the enable signal.

9.6 Regarding AC Testing

In AC testing, the elapsed time from when the state of any input pin changes until the change propagates to the output pin is measured. The measurement paths chosen by customers are used for AC testing.

9.6.1 Constraints Regarding Measurement Events

AC testing is normally conducted using a test method known as the binary research method. For the measured pin (i.e., an output pin the state of which has changed), there can be only one location within the measurement event at which the measured pin changes state. (No measurements can be taken at the pins from which RZ waveforms are output. Nor can measurements be taken in cases in which hazards are output in the measurement event.) Furthermore, the state changes of the signal that can be measured must be High to Low or Low to High (changes in which Z is involved cannot be measured).

It should also be noted that caution must be used in the selection of a measurement event in which no multiple output pins change state at the same time, or in which there is no signal contention between the bi-directional pins and the LSI tester. This is due to the fact that a simultaneous change in state or signal contention causes the LSI's power supply to fluctuate greatly, which affects the output waveform at the measured pin, making precise measurement impossible.

9.6.2 Constraints on the Measurement Location for AC Testing

Limit the measurement locations in AC testing to four.

9.6.3 Constraints Regarding the Path Delay Which is Tested

In the AC measurement path, the larger the delay, the greater the measurement accuracy. Make sure the delay time in the measured path is set to 30 ns or more, but does not exceed the strobe point under Max conditions of test simulation.

9.6.4 Other Constraints

- (1) Do not specify paths from the oscillation circuit.
- (2) Specify paths that do not pass through the internal 3-state circuit (internal bus).
- (3) Do not specify paths in which there is any bi-directional cell between the input buffer and the output buffer of the measured path.
- (4) If power supplies with two or more voltage ranges are used, limit the measured voltage in AC testing to one of those voltage ranges.

9.7 Test Patterns Constraints for Bi-directional Pins

Due to constraints on tester performance, the bi-directional pins cannot be switched between input and output modes more than twice per event. Therefore, make sure the test patterns created do not use RZ waveforms to control the switching of input/output modes for the bi-directional cells.

However, RZ waveforms may be used only if the bi-directional pins do not have an output state and are handled in the same way as the input pins.

9.8 Notes on Device in a High-Impedance State

At Epson, CMOS devices are subject to the limitation that, when the input pins are in a high-impedance state, the device operation cannot be guaranteed and the high-impedance state is inhibited during simulation.

To solve such high-impedance-related problems, I/O cells with pull-up/pull-down resistors are available from Epson. However, the propagation delays in the pull-up/pull-down resistors of these cells are not taken into consideration in simulation for the reasons specified below. Therefore, because operation cannot be precisely simulated, the non-input state for the bi-directional pins with pull-up/pull-down resistors in input mode is also inhibited during simulation.

<Reasons that the propagation delays in pull-up/pull-down resistors are not considered>

Because the delay fluctuates significantly depending on the external load capacitance

Because the pull-up/pull-down resistors are used only to avoid floating gates due to the high-impedance state

At Epson, test patterns are checked for the above contents prior to simulation through the use of an appropriate tool. If state Z representing a high-impedance state is detected, customers are requested to correct the test pattern.

In such a case, for the aforementioned reasons, customers are also cautioned about the “Z” state on the bi-directional pins with pull-up/pull-down resistors, as well as for open-drain bi-directional pins.

<Corrective measures>

When test patterns are checked, all occurrences of the Z state in the bi-directional pins are indicated by an error (not including the Z state appearing on the 3-state and open-drain output pins).

As a means of correcting the input pattern, a utility program is available from Epson that replaces the Z state on the aforementioned bi-directional pins with logic 1 when they come equipped with a pull-up resistor, or logic 0 when they come equipped with a pull-down resistor.

If bi-directional pins in the X state are placed in input mode, the X state is propagated in simulation regardless of whether they have a pull-up or pull-down resistor, and is represented by “?” in the simulation result. Customers are requested to correct occurrences of “?” before conducting resimulation.

Table 9-1 Handling the Signal at the Bi-directional Pins in Simulation

Input Pattern	Input/Output Mode	Simulation	Simulation Result (Output Pattern)
"X"	Input Mode	"X"	"?"
"1", "H"	Input Mode	"1"	"1"
"0", "L"	Input Mode	"0"	"0"

AMERICA

EPSON ELECTRONICS AMERICA, INC.**- HEADQUARTERS -**

150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

- SALES OFFICES -**West**

1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

Central

101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast

301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast

3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

- DESIGN SUPPORT CENTERS -**San Jose Asic Design Center**

150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH**- HEADQUARTERS -**

Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

DÜSSELDORF BRANCH OFFICE

Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

UK & IRELAND BRANCH OFFICE

Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE

1 Avenue de l'Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE**Barcelona Design Center**

Edificio Testa
Adva. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 Fax: +34-93-544-2491

Scotland Design Center

Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 Fax: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.

23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH

7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: 86-21-5423-5577 Fax: 86-21-5423-4677

EPSON HONG KONG LTD.

20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

14F, No. 7, Song Ren Road,
Taipei 110
Phone: 02-8786-6688 Fax: 02-8786-6660

HSINCHU OFFICE

13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900 Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.

No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-6337-7911 Fax: +65-6334-2716

SEIKO EPSON CORPORATION**KOREA OFFICE**

50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

GUMI OFFICE

6F, Good Morning Securities Bldg.
56 Songjeong-Dong, Gumi-City, 730-090, KOREA
Phone: 054-454-6027 Fax: 054-454-6093

SEIKO EPSON CORPORATION**ELECTRONIC DEVICES MARKETING DIVISION****IC Marketing Department****IC Marketing & Engineering Group**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5117

S1K70000 / S1X70000 Series

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SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ EPSON Electronic Devices Website

<http://www.epsondevice.com>



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