

STAND-OFF VOLTAGE - 5.0 Volts
POWER DISSIPATION - 120 WATTS

● GENERAL DESCRIPTION

The L12ESDL5V0C6-4X is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

● FEATURES

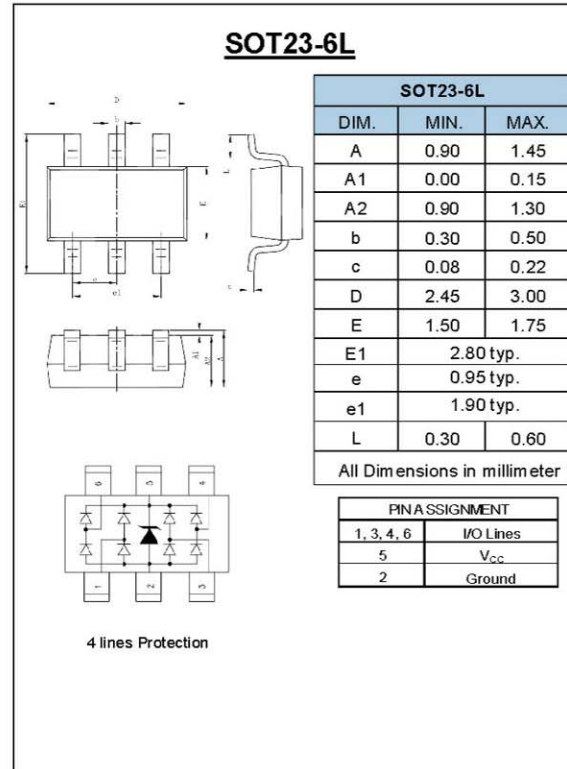
- Protects up to four I/O lines (Data lines) & power line (Vcc pin5)
- Low capacitance: 0.3pF typical (I/O to I/O)
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air); > ±8KV (contact).

● APPLICATION

- High Definition Multimedia Interface (HDMI)
- Digital Visual Interface (DVI)
- Monitors and Flat Panel Displays
- USB 2.0
- USB OTG
- IEEE 1394 Firewire Port

● MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br,Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E



● MAXIMUM RATINGS (T_J= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P _{pk}	120	W
Peak Pulse Current (tp = 8/20us)	I _{pp}	5	A
Operating Junction Temperature Range	T _J	-55 to + 125	°C
Storage Temperature Range	T _{stg}	-55 to + 150	°C
Soldering Temperature, t max = 10s	T _L	260	°C

● ELECTRICAL CHARACTERISTICS (T_J= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V _{RVM}	Any pin to ground	---	---	5.0	V
Breakdown voltage	V _{BR}	I _R = 1 mA	6.0	---	---	V
Reverse leakage current	I _{RM}	V _{DRM} = 5V	---	---	1	uA
Clamping Voltage	V _C	I _{PP} = 1A, tp = 8/20μs, Any I/O pin to ground	---	---	15	V
Clamping Voltage	V _C	I _{PP} = 5A, tp = 8/20μs, Any I/O pin to ground	---	---	24	V
Junction capacitance	C _J	V _R = 2.5V, f = 1MHz, Any I/O pin to ground	---	---	0.8	pF
Junction capacitance	C _J	V _R = 2.5V, f = 1MHz, Between I/O pins	---	---	0.4	pF

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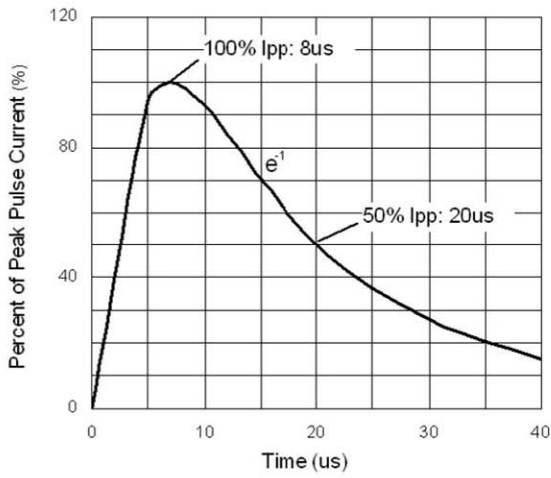


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

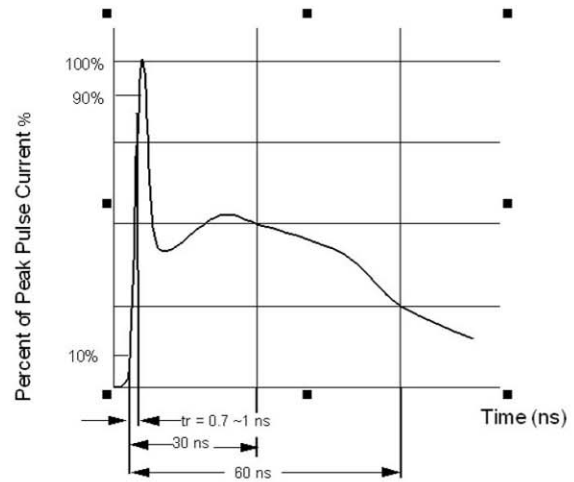


Figure 2. ESD pulse waveform according to IEC 61000-4-2

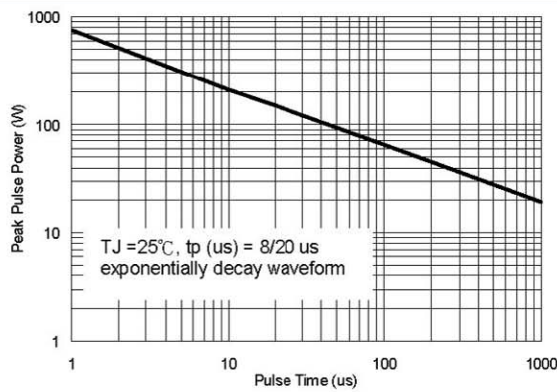


Figure 3. Power Dissipation versus Pulse Time

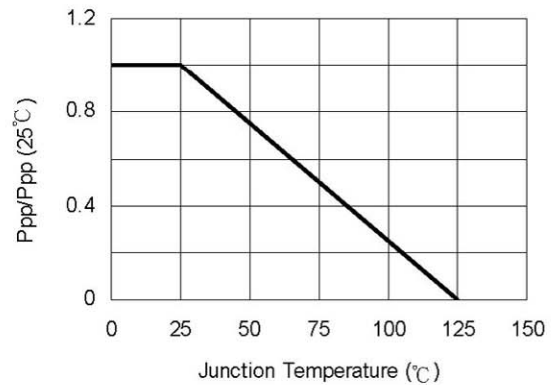


Figure 4. Peak pulse power versus TJ

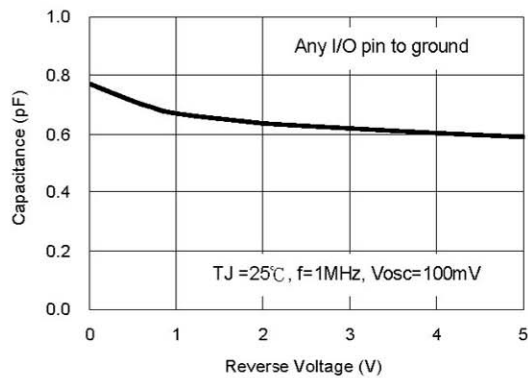


Figure 5. Typical Junction Capacitance

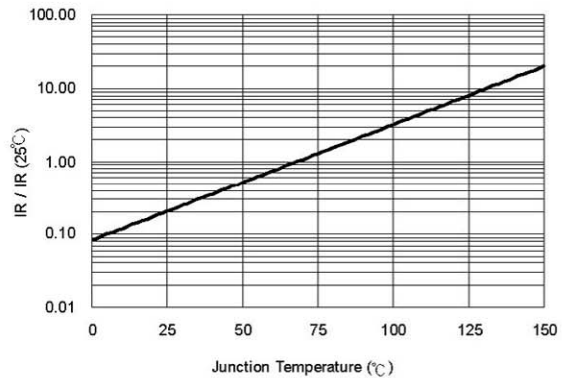


Figure 6. Reverse Leakage Current versus TJ

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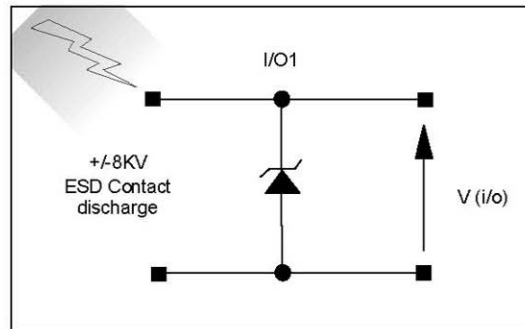


Figure 7. ESD Test Configuration

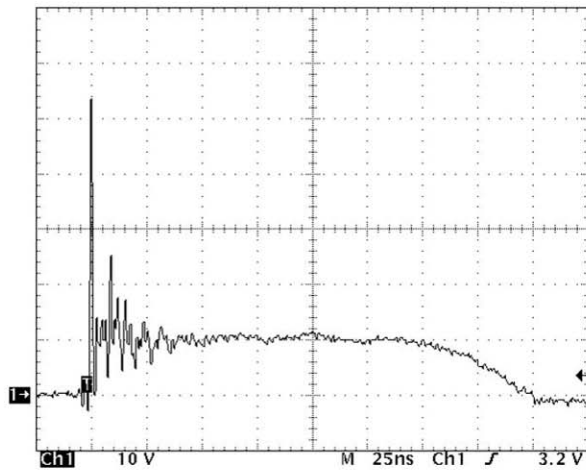


Figure 8. Clamped +8 kV ESD voltage waveform

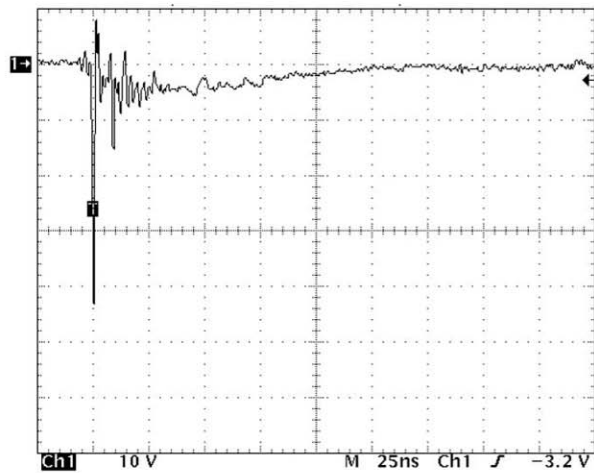


Figure 9. Clamped -8 kV ESD voltage waveform

