

UT54ACS132E

Quadruple 2-Input NAND Schmitt Triggers

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FEATURES

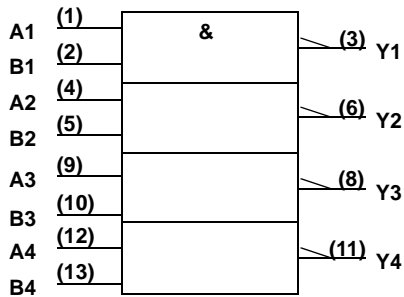
- 0.6μm CRH CMOS Process
 - Latchup immune
- High speed
- Low power consumption
- Wide operating power supply from 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack

DESCRIPTION

The UT54ACS132 is a quadruple 2-input NAND gate with Schmitt Trigger input levels. A high applied on both the inputs forces the output to a low state.

The devices are characterized over full HiRel temperature range of -55°C to +125°C.

LOGIC SYMBOL



Note:

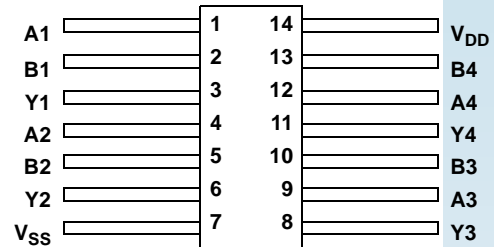
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

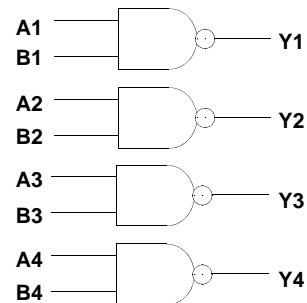
INPUTS		OUTPUT
An	Bn	Yn
L	L	H
L	H	H
H	L	H
H	H	L

PINOUT

**14-Lead Flatpack
Top View**



LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} + .3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	3.0 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to +125	°C

DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS132E⁷

($V_{DD} = 3.0V$ to $5.5V$; $V_{SS} = 0V^6$; $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	Description	CONDITION	VDD	MIN	MAX	UNIT
V_{T+}	Schmitt trigger positive-going threshold ¹		3.0V		2.1	V
			5.5V		3.85	
V_{T-}	Schmitt trigger negative-going threshold ¹		3.0V	0.9		V
			5.5V	1.65		
V_H	Hysteresis ² ($V_{T+} - V_{T-}$)		3.0V	0.3	1.2	V
			4.5V	.6	1.5	
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}	5.5V	-1	1	μA
V_{OL}	Low-level output voltage ³	$I_{OL} = 100\mu A$	3.0V		0.25	V
			4.5V		0.25	
V_{OH}	High-level output voltage ³	$I_{OH} = -100\mu A$	3.0V	2.75		V
			4.5V	4.25		
I_{OS}	Short-circuit output current ^{2,4}	$V_O = V_{DD}$ and V_{SS}	3.0V	-100	100	mA
			5.5V	-200	200	
I_{OL}	Low level output current ⁹	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	3.0V	6		mA
			5.5V	8		
I_{OH}	High level output current ⁹	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4V$	3.0V		-6	mA
			5.5V		-8	
P_{total}	Power dissipation ^{2,8}	$C_L = 50pF$	5.5V		1.9	mW/ MHz
			3.0V		0.76	
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	5.5V		10	μA
C_{IN}	Input capacitance ⁵	$f = 1MHz$	0V		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz$	0V		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\min) + 20\%$, -0% ; $V_{IL} = V_{IL}(\max) + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\min)$ and $V_{IL}(\max)$.
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose $\leq 1E6$ rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.
- Power dissipation specified per switching output.
- This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS132E²

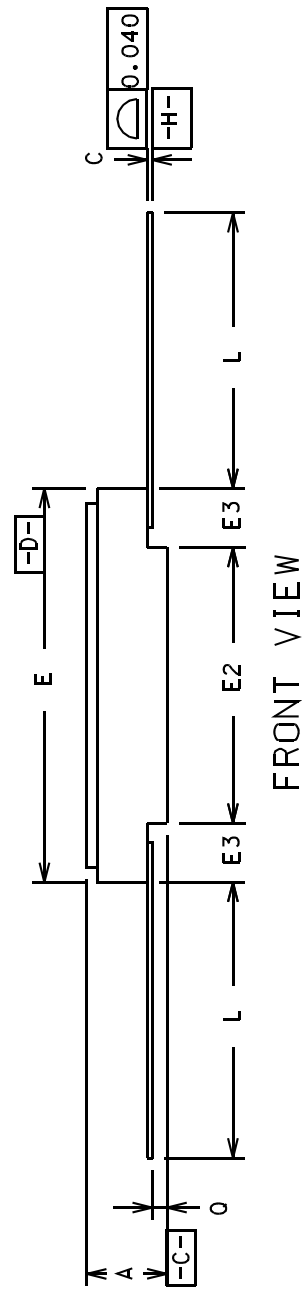
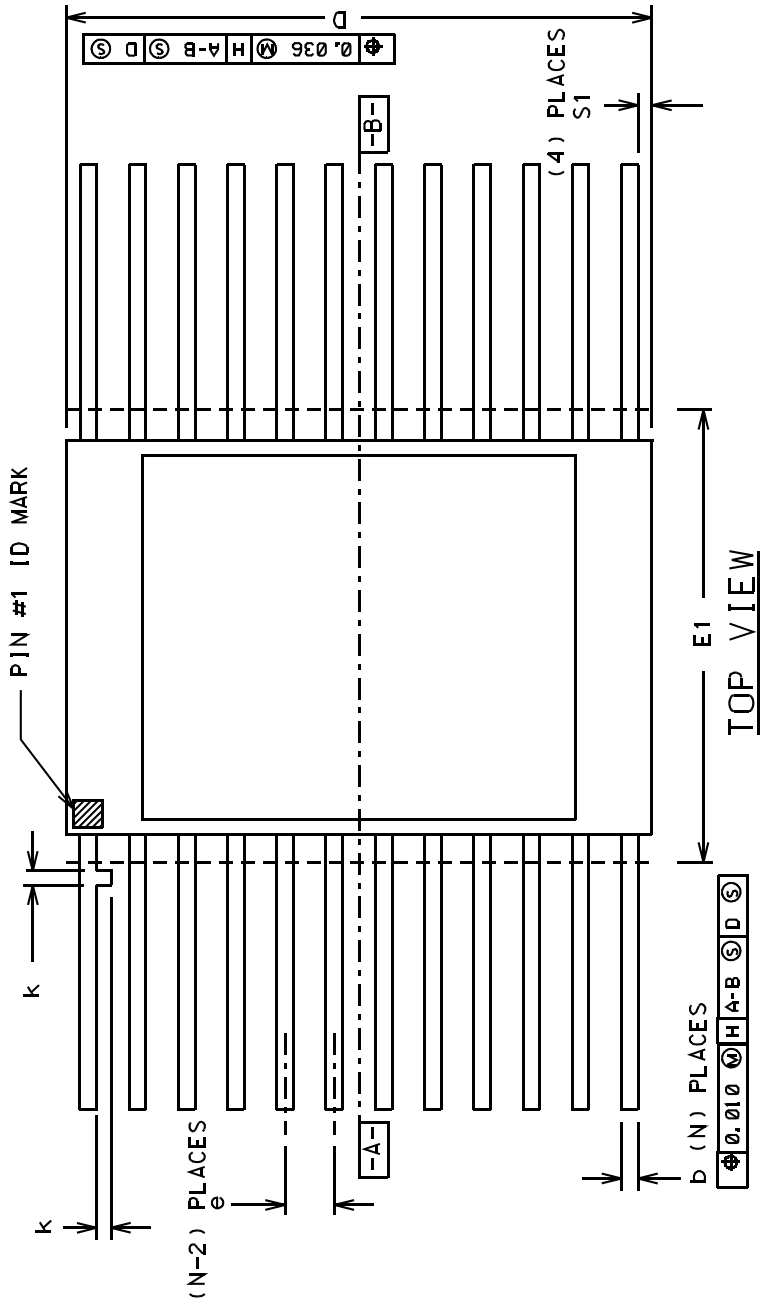
($V_{DD} = 3.0V$ to $5.5V$; $V_{SS} = 0V$ ¹, $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	PARAMETER		V_{DD}	MINIMUM	MAXIMUM	UNIT
t_{PHL}	Input to Yn	$C_L = 30pF$	3.0V & 3.6V	2	12	ns
			4.5V & 5.5V	2	8	
		$C_L = 50pF$	3.0V & 3.6V	2	16	ns
			4.5V & 5.5V	2	12	
t_{PLH}	Input to Yn	$C_L = 30pF$	3.0V & 3.6V	2	15	ns
			4.5V & 5.5V	2	11	
		$C_L = 50pF$	3.0V & 3.6V	2	19	ns
			4.5V & 5.5V	2	15	

Notes:

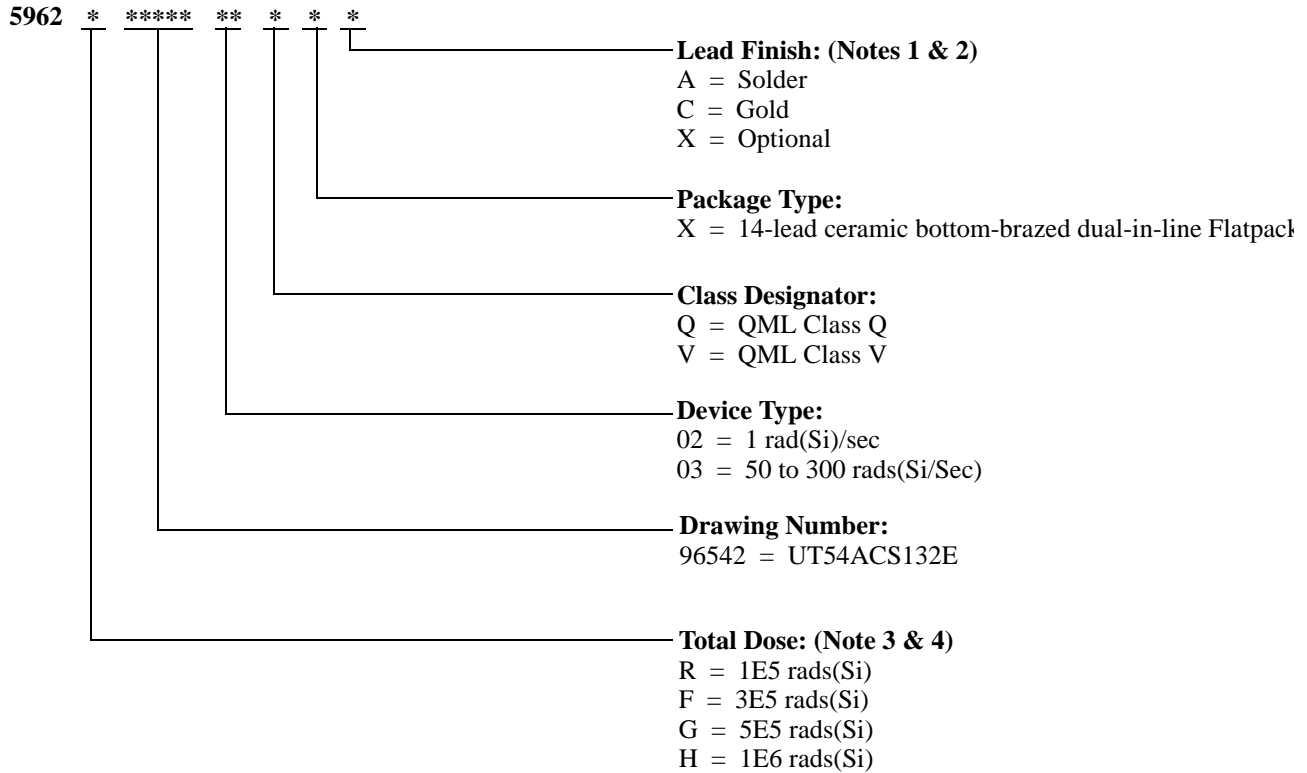
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose $\leq 1E6$ rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.

Packaging



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.235	---	0.130	BSC	0.008	0.270	0.026	0.005	
-04	16	F-5A	0.115	0.022	0.009	0.440	0.285	0.315	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	0.130	BSC	0.008	0.250	0.026	0.005	
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	0.130	BSC	0.008	0.250	0.026	0.005	

Ordering Information: UT54ACS132E: SMD



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

COLORADO

Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL

Tel: 805-778-9229
Fax: 805-778-1980

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Tel: 603-888-3975
Fax: 603-888-4585

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Fax: 321-951-4254

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Tel: 949-362-2260
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Tel: 719-594-8017
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www.aeroflex.com info-ams@aeroflex.com

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