EMI6183

Common Mode Filter with ESD Protection

ON Semiconductor®

http://onsemi.com

Product Description

The EMI6183 is an Integrated Common Mode Filter in a 3x2, 6−bump, 0.4 mm pitch, CSP form factor for the elimination of common mode noise in high speed data line applications such as USB2.0 and other LVDS type applications. ESD protection is integrated into the Common mode filter for superior protection and significant part count reduction.

Features

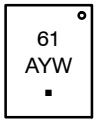
- Single Integrated Package for Common Mode Filter (CMF) and ESD Protection for High Speed Data Lines
- High Differential Mode Bandwidth Cutoff Frequency for Best Signal Integrity
- 3 x 2, 6−bump, 0.4 mm pitch CSP
- Provides ESD protection to IEC61000−4−2 Level 4, ±8 kV Contact Discharge at External Pins and Stand−Alone C2 Pin
- Provides ESD protection to IEC61000−4−2 Level 1, ±2 kV Contact Discharge at Internal Pins
- Low Channel Input Capacitance
- Coated for Improved Reliability at Assembly
- These Devices are Pb−Free and are RoHS Compliant II Packaging

Applications

- High Speed Differential Data Lines
- USB2.0
- LVDS

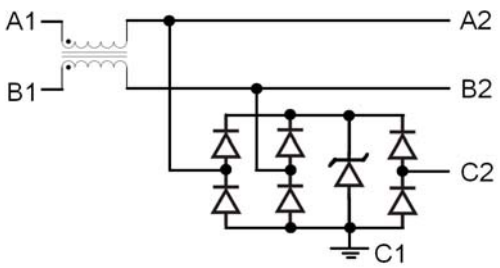
MARKING DIAGRAM

WLCSP6
CASE 567GA

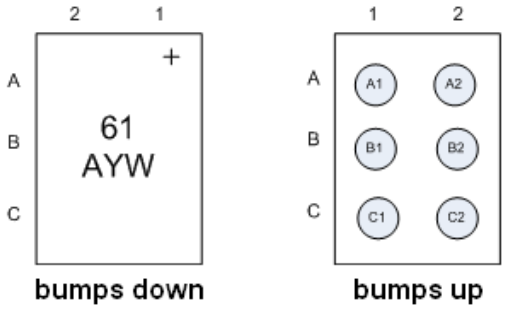


61 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ORDERING INFORMATION

Device	Package	Part Marking	Shipping†
EMI6183FCTBG	3 x 2, 6−bump CSP	61	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN DESCRIPTION

Pin Name	Type	Parameter
A1	I/O	CMF Channel 1+ to ASIC (Internal Pin)
A2	I/O	CMF Channel 1+ to Connector (External Pin)
B1	I/O	CMF Channel 1− to ASIC (Internal Pin)
B2	I/O	CMF Channel 1− to Connector (External Pin)
C1	GND	Ground
C2	ID	ID Pin for ESD Protection (External Pin)

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Parameter	Symbol	Rating	Unit
ESD Discharge IEC61000−4−2 Contact Discharge	V_{PP}	±8.0	kV
Operating Temperature Range	T_{OP}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C
Maximum Lead Temperature for Soldering Purposes (1/8” from Case for 10 seconds)	T_L	260	°C
DC Current per Line	I_{LINE}	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Reverse Working Voltage	V_{RWM}				5.5	V
Breakdown Voltage	V_B	I_R = 1 mA	6.0			V
Leakage Current	I_{LEAK}	V_{RWM} = 3 V		10	300	nA
ESD Protection Peak Discharge Voltage at A2, B2 & C2 a) Contact discharge per IEC61000−4−2 Standard b) Air discharge per IEC61000−4−2 Standard	V_{ESD}	(Notes 2 and 3)	 ±8.0 ±15			 kV kV
ESD Protection Peak Discharge Voltage at A1 & B1 a) Contact discharge per IEC61000−4−2 Standard b) Air discharge per IEC61000−4−2 Standard	V_{ESD}	(Notes 2 and 3)	 ±2.0 ±2.0			 kV kV
TLP Clamping Voltage (See Figure 6)	V_{CL}	Forward I_{PP} = 8 A Forward I_{PP} = 16 A Reverse I_{PP} = −8 A Reverse I_{PP} = −16 A		11.58 15 −4.5 −8.8		V V V V
Resistance A1 to A2; B1 to B2	R_{CH}			8.0		Ω
Capacitance B2 to C1	C_{L1}	At 1 MHz, V_{IN} = 0 V (Note 2)		2.8		pF
Capacitance A2 to C1	C_{L2}	At 1 MHz, V_{IN} = 0 V (Note 2)		3.1		pF
Capacitance C2 to C1	C_{ID}	At 1 MHz, V_{IN} = 0 V (Note 2)			1.5	pF
Differential Mode Cut−Off Frequency	f_{3dB}	(Note 4)		2.0		GHz
Common Mode Stop Band Attenuation	F_{atten}	@ 800 MHz		21		dB

1. All parameters specified at T_A = 25°C unless otherwise specified.
2. These parameters guaranteed by design and characterization.
3. Standard IEC61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 300 Ω.
4. Above this frequency, appreciable Common Mode Attenuation occurs at 50 Ω Source and 50 Ω load termination.

TYPICAL CHARACTERISTICS

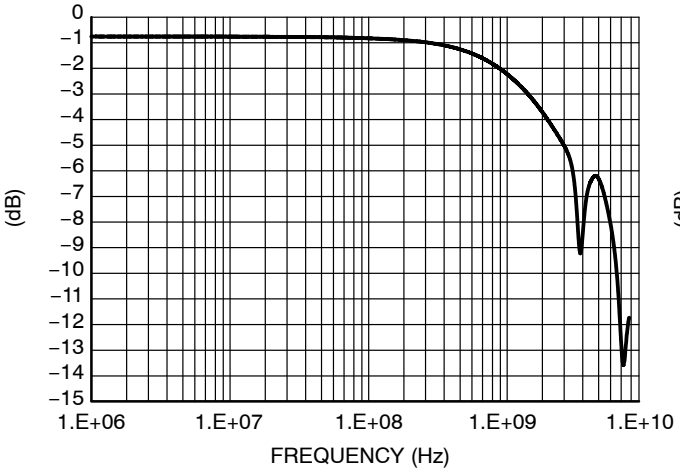


Figure 1. Differential Mode Attenuation vs. Frequency

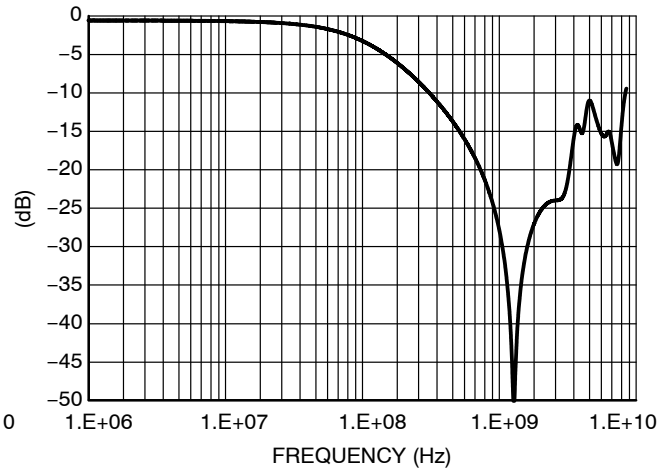
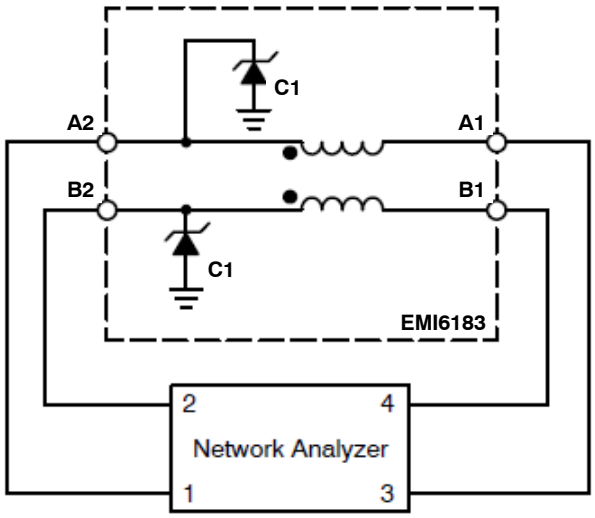


Figure 2. Common Mode Attenuation vs. Frequency

TEST CONFIGURATION



Normal (Differential) Mode

Figure 3. Normal (Differential) Mode Test Configuration

APPLICATION SCHEMATIC

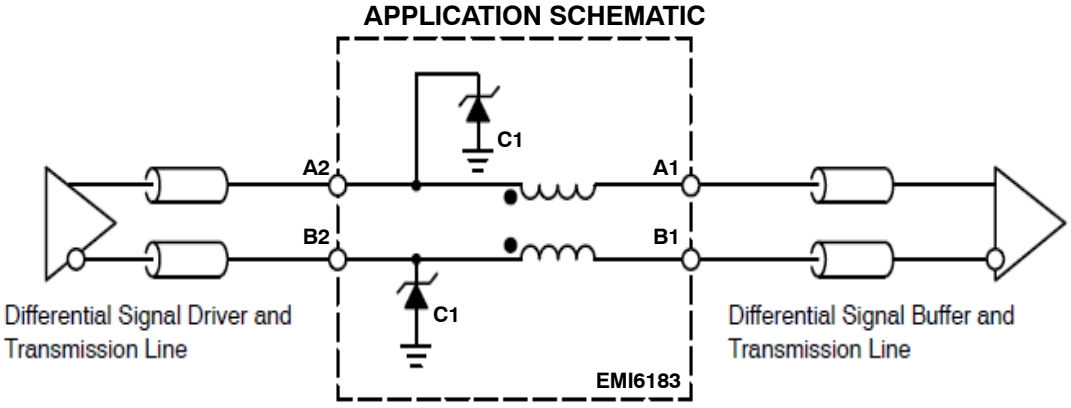


Figure 4. Application Circuit

Transmission Line Pulse (TLP) Measurements

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 5. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 6 where an 8 kV IEC61000−4−2 current waveform is compared with TLP current pulses at 8 and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I−V curves for the EMI6183 are shown in Figure 7.

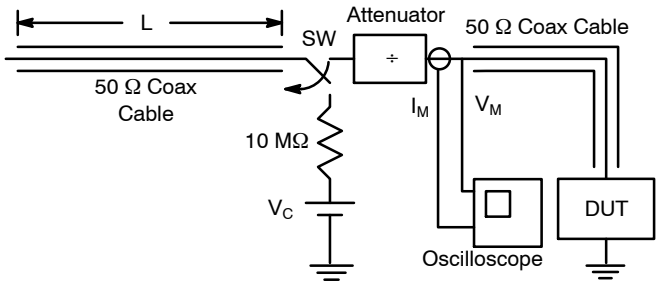


Figure 5. Simplified Schematic of a Typical TLP System

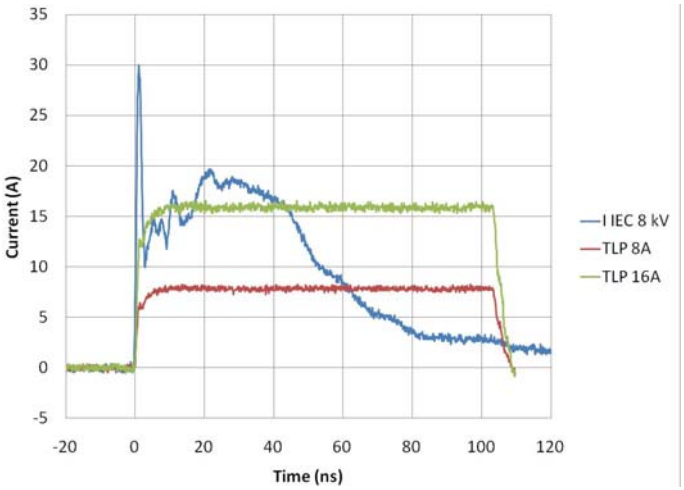


Figure 6. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms

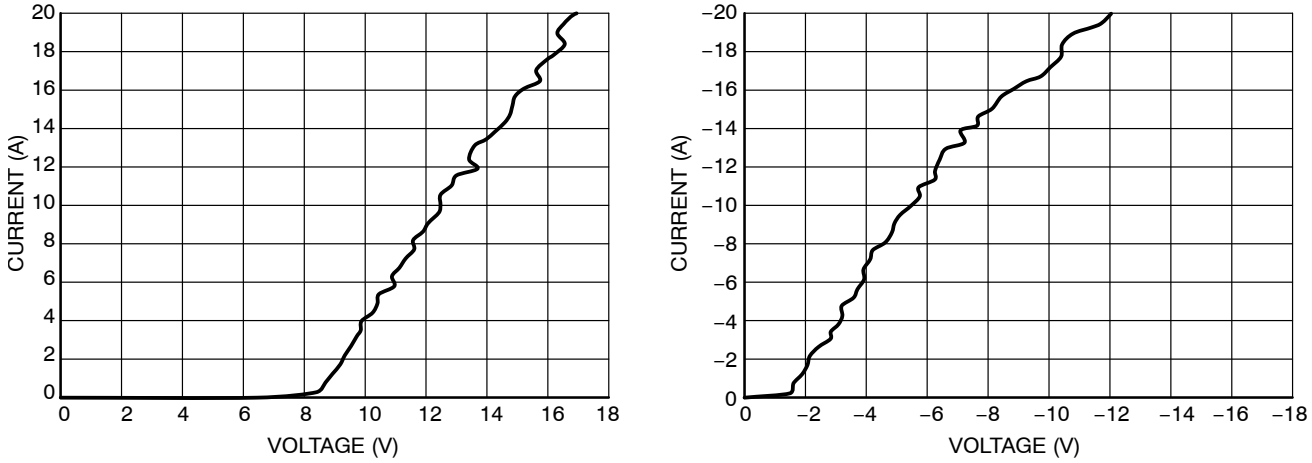


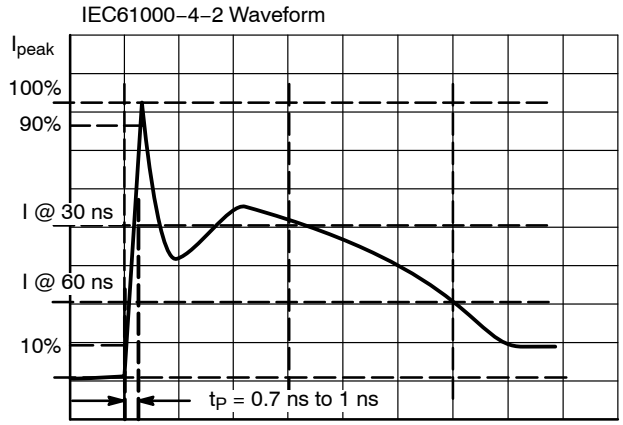
Figure 7. Positive and Negative TLP Waveforms

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



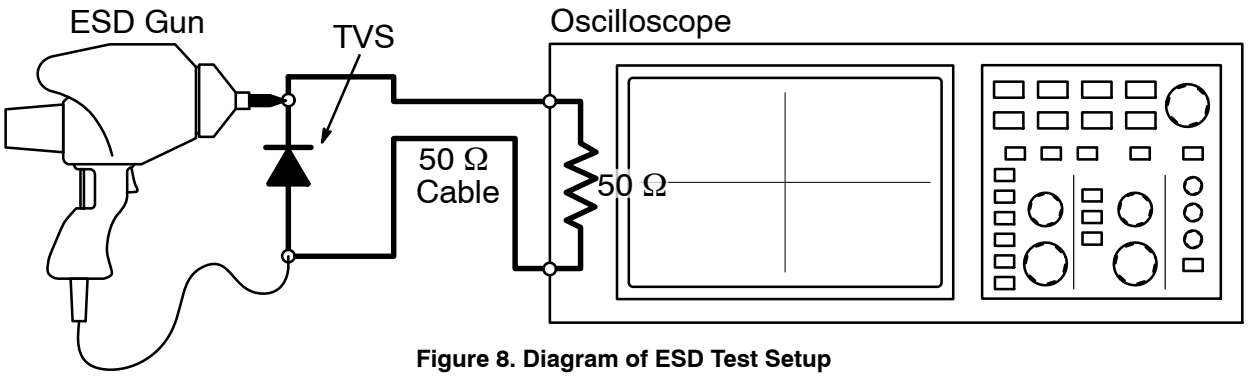


Figure 8. Diagram of ESD Test Setup

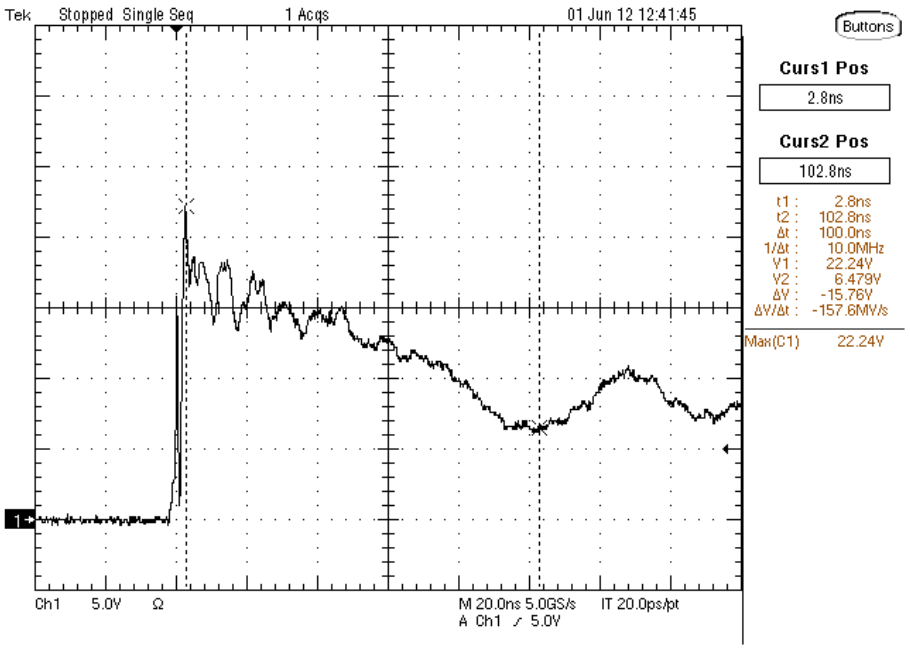


Figure 9. ESD Clamping Voltage +8 kV per IEC6100−4−2 (external to internal pin)

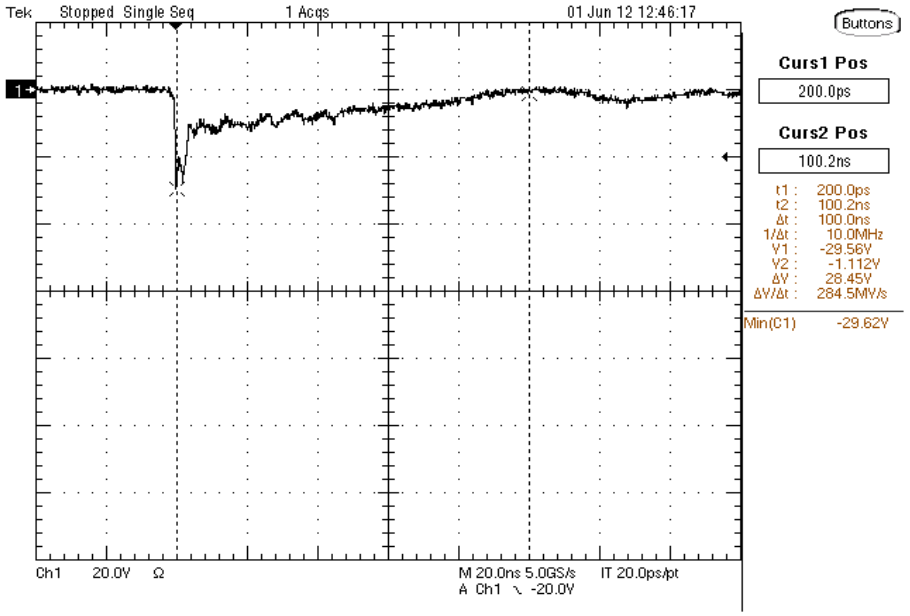
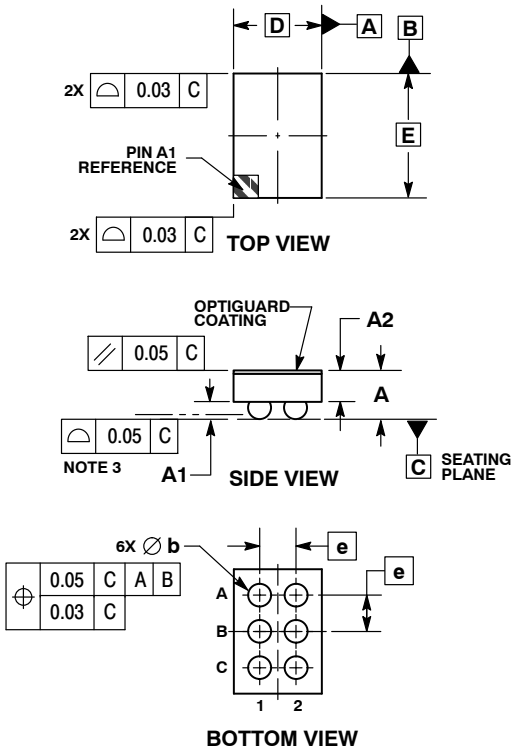


Figure 10. ESD Clamping Voltage −8 kV per IEC6100−4−2 (external to internal pin)

PACKAGE DIMENSIONS

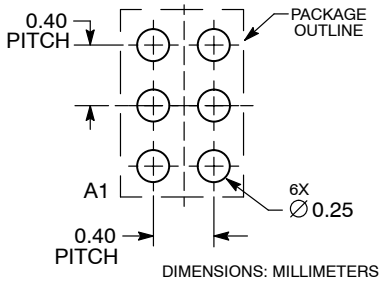
WLCSP6, 0.97x1.37
CASE 567GA
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.58
A1	0.17	0.24
A2	0.35 REF	
b	0.24	0.29
D	0.97 BSC	
E	1.37 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative