

High-Voltage NPN Silicon Transistor

... designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

• High Voltage —

 $V_{CEX} = 400 \text{ Vdc}$

- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V _{CEX}	400	Vdc
Collector-Base Voltage	V _{CB}	400	Vdc
Emitter–Base Voltage	V _{EB}	5.0	Vdc
Collector Current — Continuous	I _C	10	Adc
Base Current	Ι _Β	2.0	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	125 1.0	Watts W/°C
Operating Junction Temperature Range	TJ	-65 to +150	°C
Storage Temperature Range	T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θJC	1.0	°C/W

MJ423

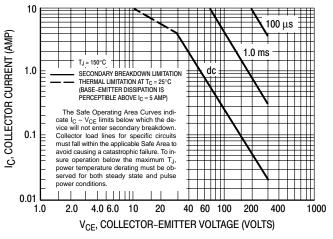
10 AMPERE
POWER TRANSISTOR
NPN SILICON
400 VOLTS
125 WATTS



ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage* (1) (I _C = 100 mAdc, I _B = 0)	V _(BR) CEO(sus)	325	_	Vdc
Collector Cutoff Current $(V_{CE} = 400 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc})$ $(V_{CE} = 400 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125 ^{\circ}C)$	I _{CEX}	_ _	0.25 0.5	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	_	5.0	mAdc
ON CHARACTERISTICS	·			•
DC Current Gain(1) ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc) ($I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc)	h _{FE}	30 10	90 —	_
Collector–Emitter Saturation Voltage (1) $(I_C = 1.0 \text{ Adc}, I_B - 0.10 \text{ Adc})$	V _{CE(sat)}	_	0.8	Vdc
Base–Emitter Saturation Voltage $(I_C = 1.0 \text{ Adc}, I_B = 0.1 \text{ Adc})$	V _{BE(sat)}	_	1.25	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I _C = 200 mAdc, V _{CE} = 10 Vdc, f = 1.0 MHz)	f⊤	2.5	_	MHz

⁽¹⁾ PW \leq 300 μ s Duty Cycle \leq 2.0%.



125 PD, POWER DISSIPATION (WATTS) 100 75 50 25 0 20 100 160 180 0 40 80 120 140 T_C, CASE TEMPERATURE (°C)

Figure 1. Active-Region Safe-Operating Area

Figure 2. Power-Temperature Derating Curve

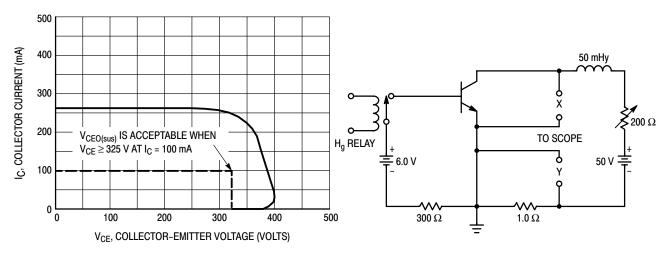


Figure 3. Sustaining Voltage Test Load Line

Figure 4. Sustaining Voltage Test Circuit

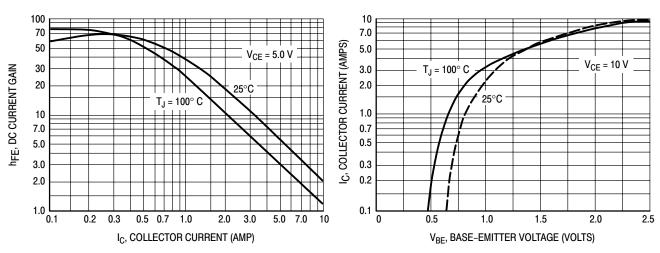
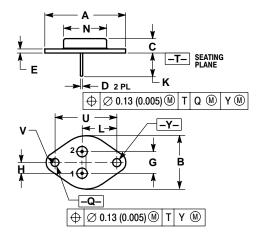


Figure 5. Current Gain

Figure 6. Transconductance

PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTRIOLLING DIMENSION: INCH.

 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.550 REF		39.37 REF		
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
E	0.055	0.070	1.40	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46 BSC		
K	0.440	0.480	11.18	12.19	
L	0.665 BSC		16.89 BSC		
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187 BSC		30.15 BSC		
٧	0.131	0.188	3.33	4.77	

STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR

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