PNP Silicon Epitaxial Transistor

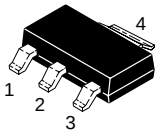
BCP69T1

ON Semiconductor Preferred Device

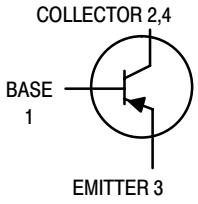
MEDIUM POWER PNP SILICON HIGH CURRENT TRANSISTOR SURFACE MOUNT

This PNP Silicon Epitaxial Transistor is designed for use in low voltage, high current applications. The device is housed in the SOT-223 package, which is designed for medium power surface mount applications.

- High Current: I_C = –1.0 Amp
- The SOT-223 Package can be soldered using wave or reflow.
- SOT-223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.
- Available in 12 mm Tape and Reel
  Use BCP69T1 to order the 7 inch/1000 unit reel.
  Use BCP69T3 to order the 13 inch/4000 unit reel.
- NPN Complement is BCP68



CASE 318E-04, STYLE 1
TO-261AA



Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	–25	Vdc
Collector-Base Voltage	V_{CBO}	–20	Vdc
Emitter-Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current	I_C	–1.0	Adc
Total Power Dissipation @ T_A = 25°C(1) Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

DEVICE MARKING

CE

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction-to-Ambient (surface mounted)	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625″ from case Time in Solder Bath	T_L	260 10	°C Sec

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = –100 μAdc, I_E = 0)	$V_{(BR)CES}$	–25	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = –1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	–20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = –10 μAdc, I_C = 0)	$V_{(BR)EBO}$	–5.0	—	—	Vdc

November, 2001 – Rev. 4

Publication Order Number:
BCP69T1/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = –25 Vdc, I_E = 0)	I_{CBO}	—	—	–10	μAdc
Emitter-Base Cutoff Current (V_{EB} = –5.0 Vdc, I_C = 0)	I_{EBO}	—	—	–10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = –5.0 mAdc, V_{CE} = –10 Vdc) (I_C = –500 mAdc, V_{CE} = –1.0 Vdc) (I_C = –1.0 Adc, V_{CE} = –1.0 Vdc)	h_{FE}	 50 85 60	 — — —	 — 375 —	—
Collector-Emitter Saturation Voltage (I_C = –1.0 Adc, I_B = –100 mAdc)	$V_{CE(sat)}$	—	—	–0.5	Vdc
Base-Emitter On Voltage (I_C = –1.0 Adc, V_{CE} = –1.0 Vdc)	$V_{BE(on)}$	—	—	–1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = –10 mAdc, V_{CE} = –5.0 Vdc)	f_T	—	60	—	MHz

TYPICAL ELECTRICAL CHARACTERISTICS

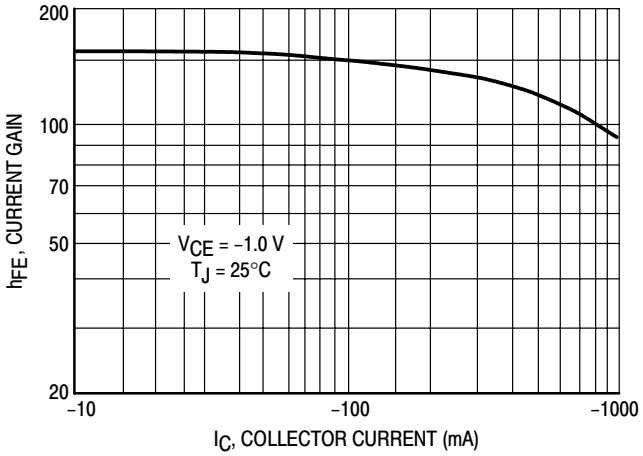


Figure 1. DC Current Gain

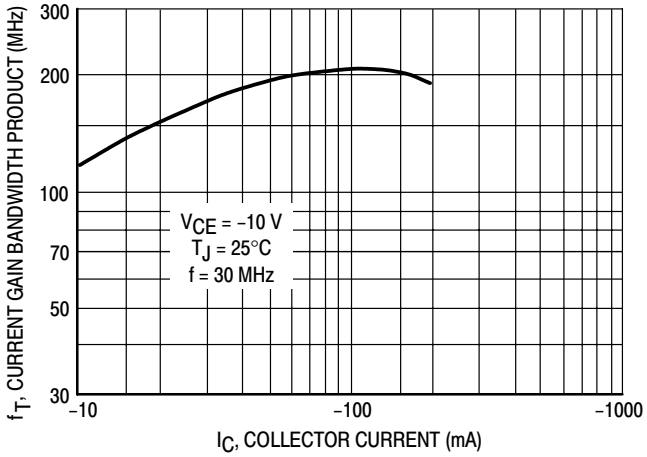


Figure 2. Current Gain Bandwidth Product

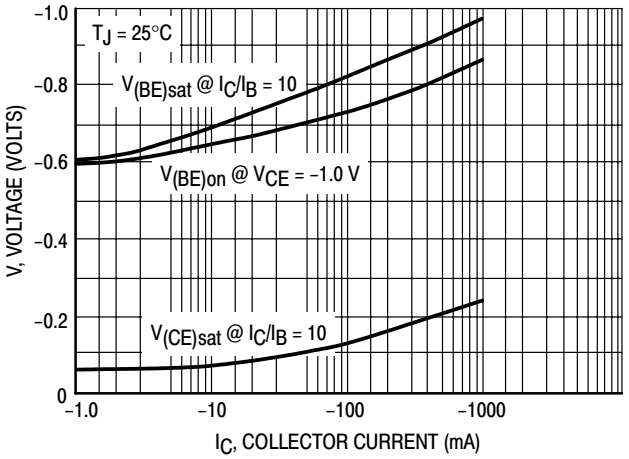


Figure 3. Saturation and "ON" Voltages

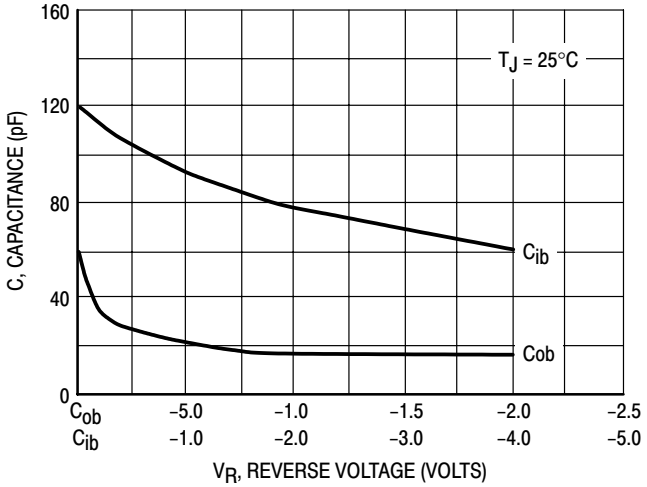
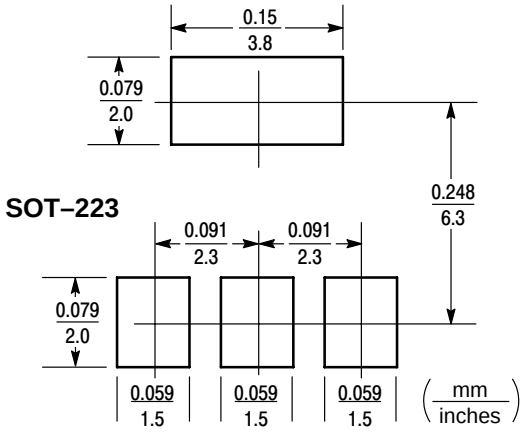


Figure 4. Capacitances

INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R\theta_{JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–223 package, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150°C - 25°C}{83.3°C/W} = 1.50 \text{ watts}$$

The 83.3°C/W assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, a higher power dissipation of 1.6 watts can be achieved using the same footprint.

SOLDERING PRECAUTIONS

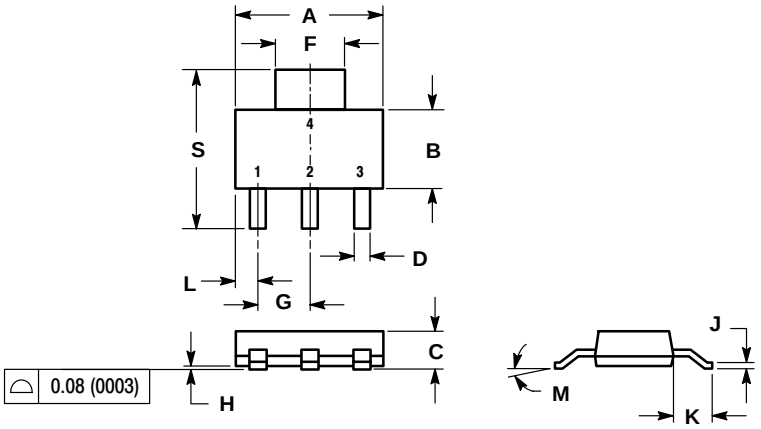
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT–223 (TO–261)
CASE 318E–04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Thermal Clad is a trademark of the Bergquist Company.

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