FAIRCHILD SEMICONDUCTOR®

April 2013

# FDD6N50/ FDU6N50

## N-Channel UniFET™ MOSFET

### 500 V, 6 A, 900 mΩ

## Features

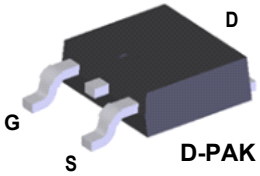
- $R_{DS(on)}$ = 900 mΩ (Max.) @ $V_{GS}$ = 10 V, $I_D$ = 3 A
- Low Gate Charge (Typ.12.8 nC)
- Low $C_{rss}$ (Typ. 9 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability

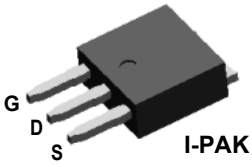
## Applications

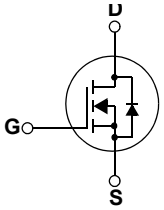
- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

## Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.




## Absolute Maximum Ratings

| Symbol | Parameter | | FDD6N50/ FDU6N50 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 500 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C)<br>- Continuous ($T_C$ = 100°C) | 6<br>3.8 | A<br>A |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 24 | A |
| $V_{GSS}$ | Gate-Source voltage | | ±30 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy (Note 2) | | 270 | mJ |
| $I_{AR}$ | Avalanche Current (Note 1) | | 6 | A |
| $E_{AR}$ | Repetitive Avalanche Energy (Note 1) | | 8.9 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | | 4.5 | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C)<br>- Derate above 25°C | 89<br>0.71 | W<br>W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | FDD6N50/ FDU6N50 | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case, Max. | 1.4 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient, Max. | 83 | |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDD6N50 | FDD6N50TM | D-PAK | 380mm | 16mm | 2500 |
| FDD6N50S | FDD6N50TM_WS | D-PAK | 380mm | 16mm | 2500 |
| FDU6N50 | FDU6N50TU | I-PAK | - | - | 70 |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 500 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, Referenced to 25°C | -- | 0.5 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 500V, $V_{GS}$ = 0V<br>$V_{DS}$ = 400V, $T_C$ = 125°C | --<br>-- | --<br>-- | 1<br>10 | μA<br>μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30V, $V_{DS}$ = 0V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30V, $V_{DS}$ = 0V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10V, $I_D$ = 3A | -- | 0.76 | 0.9 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40V, $I_D$ = 3A | -- | 2.5 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1.0MHz | -- | 720 | 940 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 95 | 190 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 9 | 13.5 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 250V, $I_D$ = 6A<br>$R_G$ = 25Ω | -- | 6 | 20 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 55 | 120 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 25 | 60 | ns |
| $t_f$ | Turn-Off Fall Time | (Note 4) | -- | 35 | 80 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 400V, $I_D$ = 6A<br>$V_{GS}$ = 10V | -- | 12.8 | 16.6 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 3.7 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | (Note 4) | -- | 5.8 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 6 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 24 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 6A | -- | -- | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_S$ = 6A<br>$dI_F/dt$ =100A/μs | -- | 275 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 1.7 | -- | μC |

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS}$ = 6A, $V_{DD}$ = 50V, L=13.5mH, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 6A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

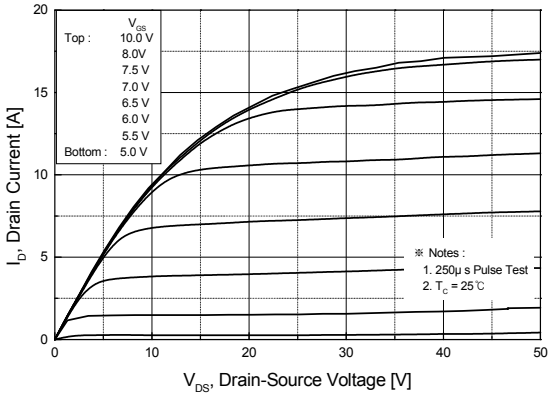



**Figure 2. Transfer Characteristics**

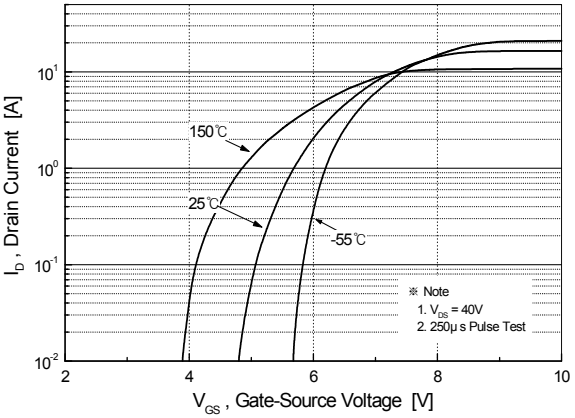



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

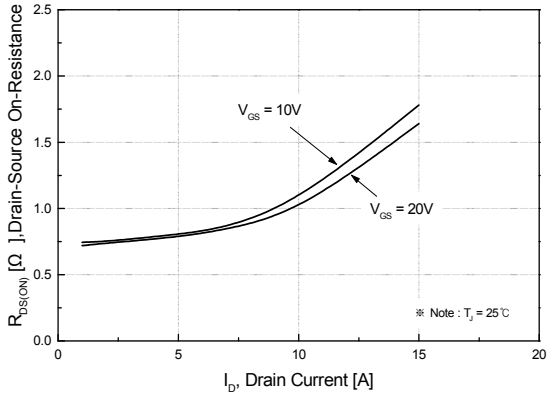



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

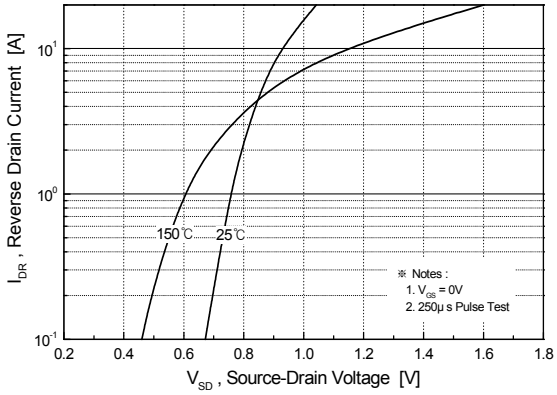



**Figure 5. Capacitance Characteristics**

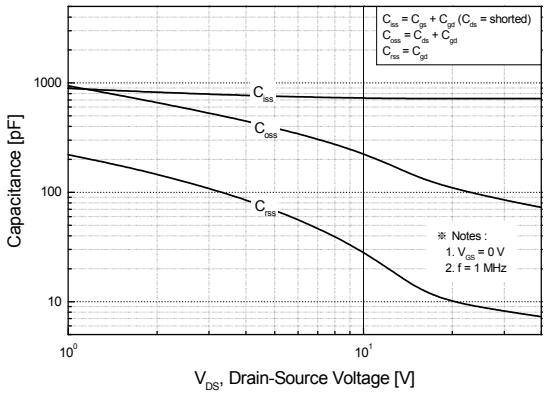
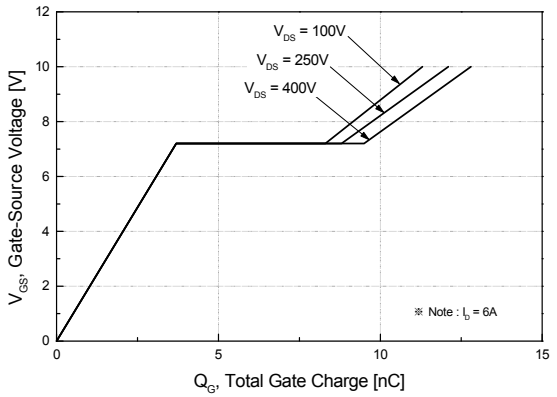



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

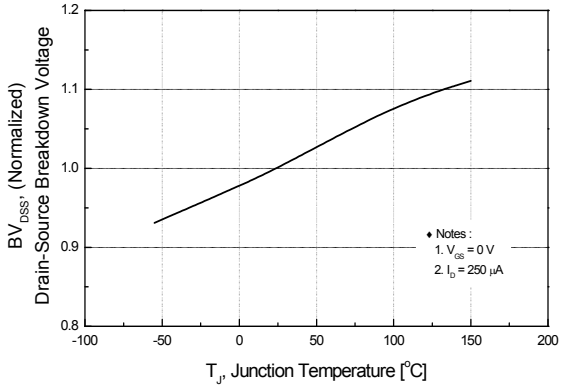



**Figure 8. On-Resistance Variation vs. Temperature**

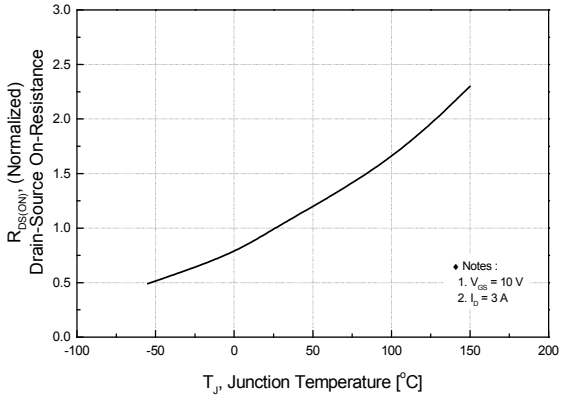



**Figure 9. Maximum Safe Operating Area**

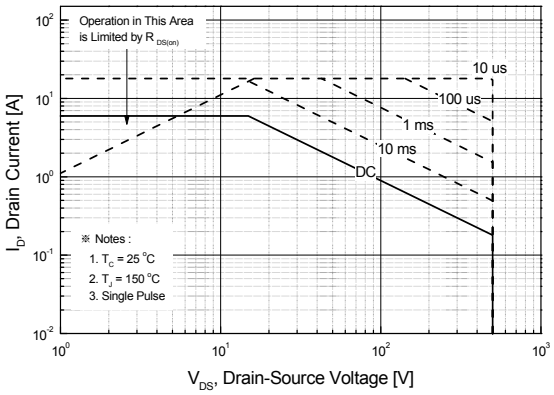



**Figure 10. Maximum Drain Current vs. Case Temperature**

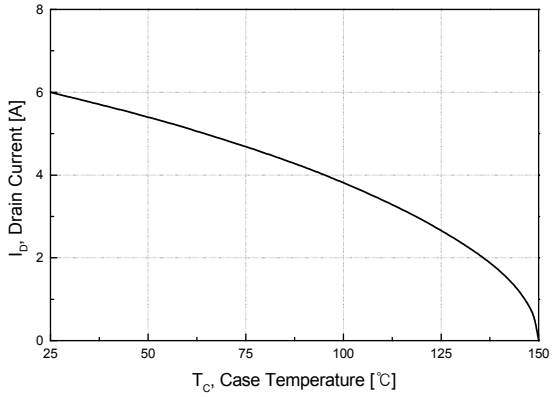
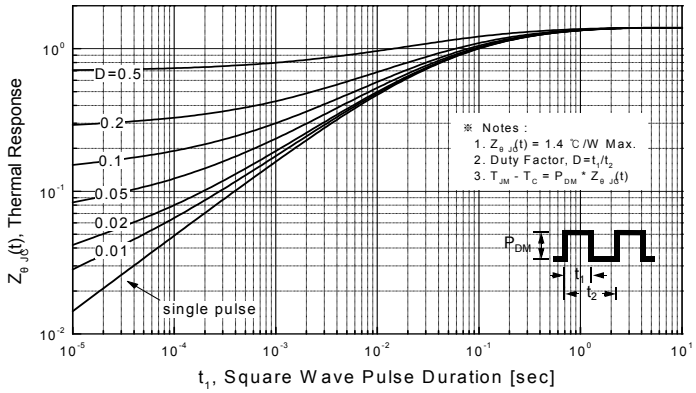
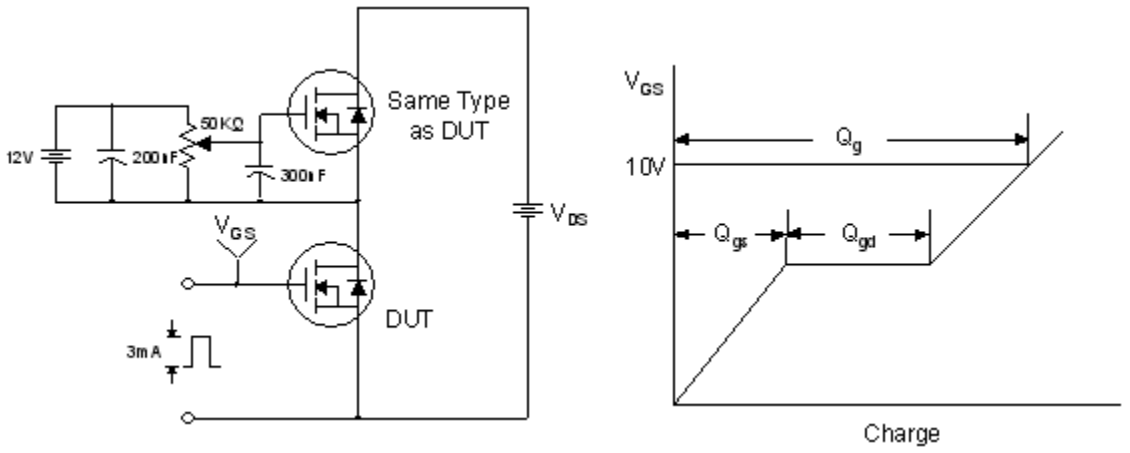


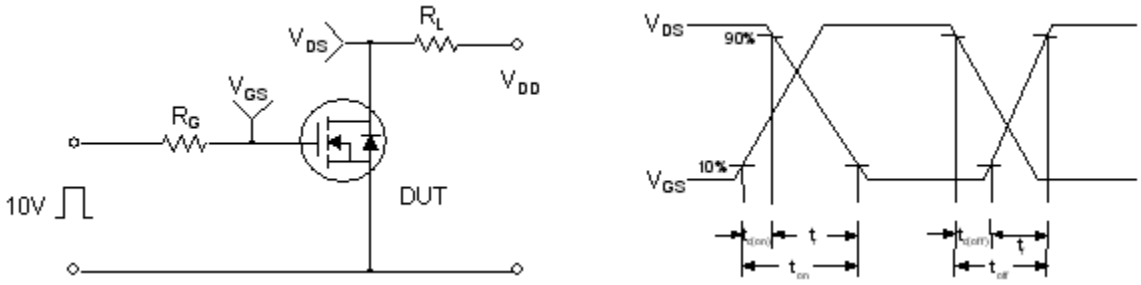

**Figure 11. Transient Thermal Response Curve**



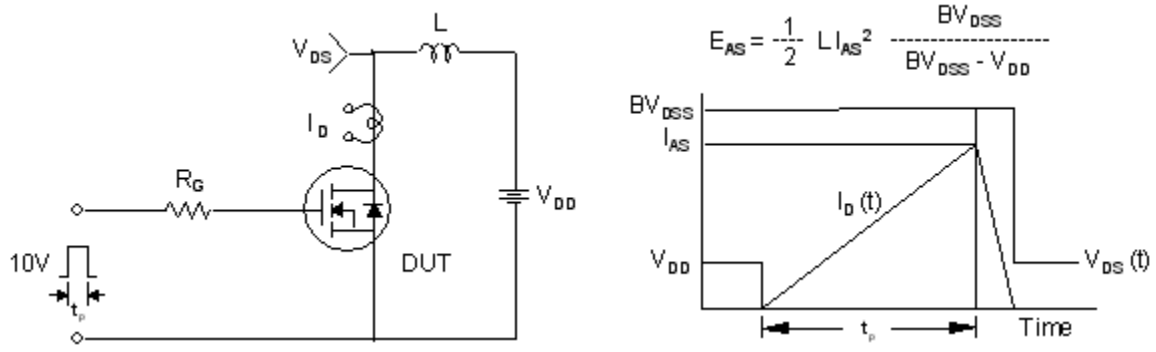
**Gate Charge Test Circuit & Waveform**



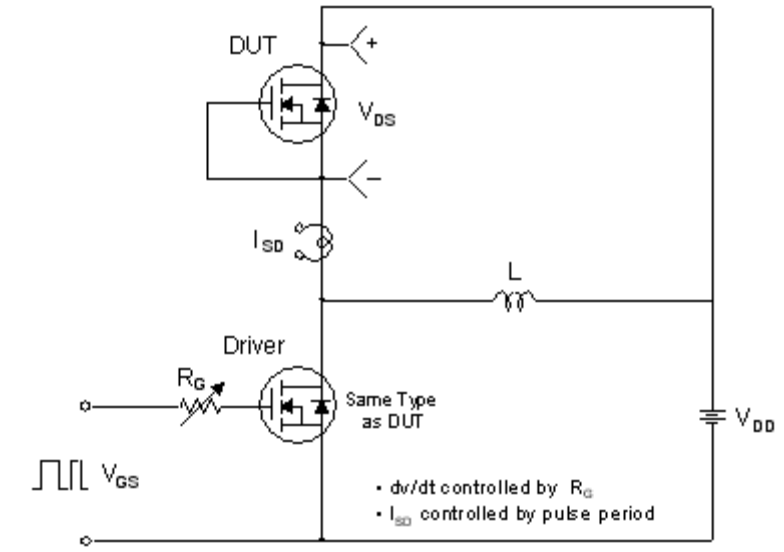

**Resistive Switching Test Circuit & Waveforms**

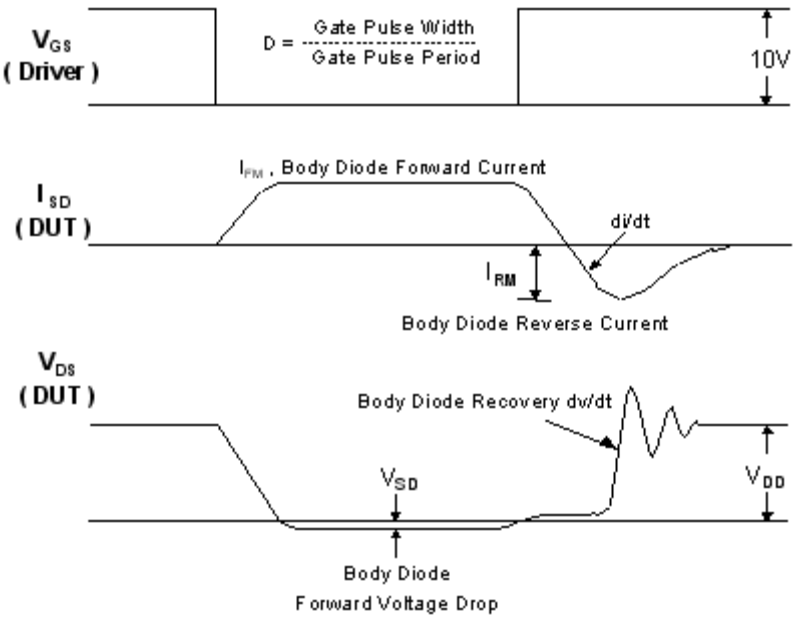



**Unclamped Inductive Switching Test Circuit & Waveforms**



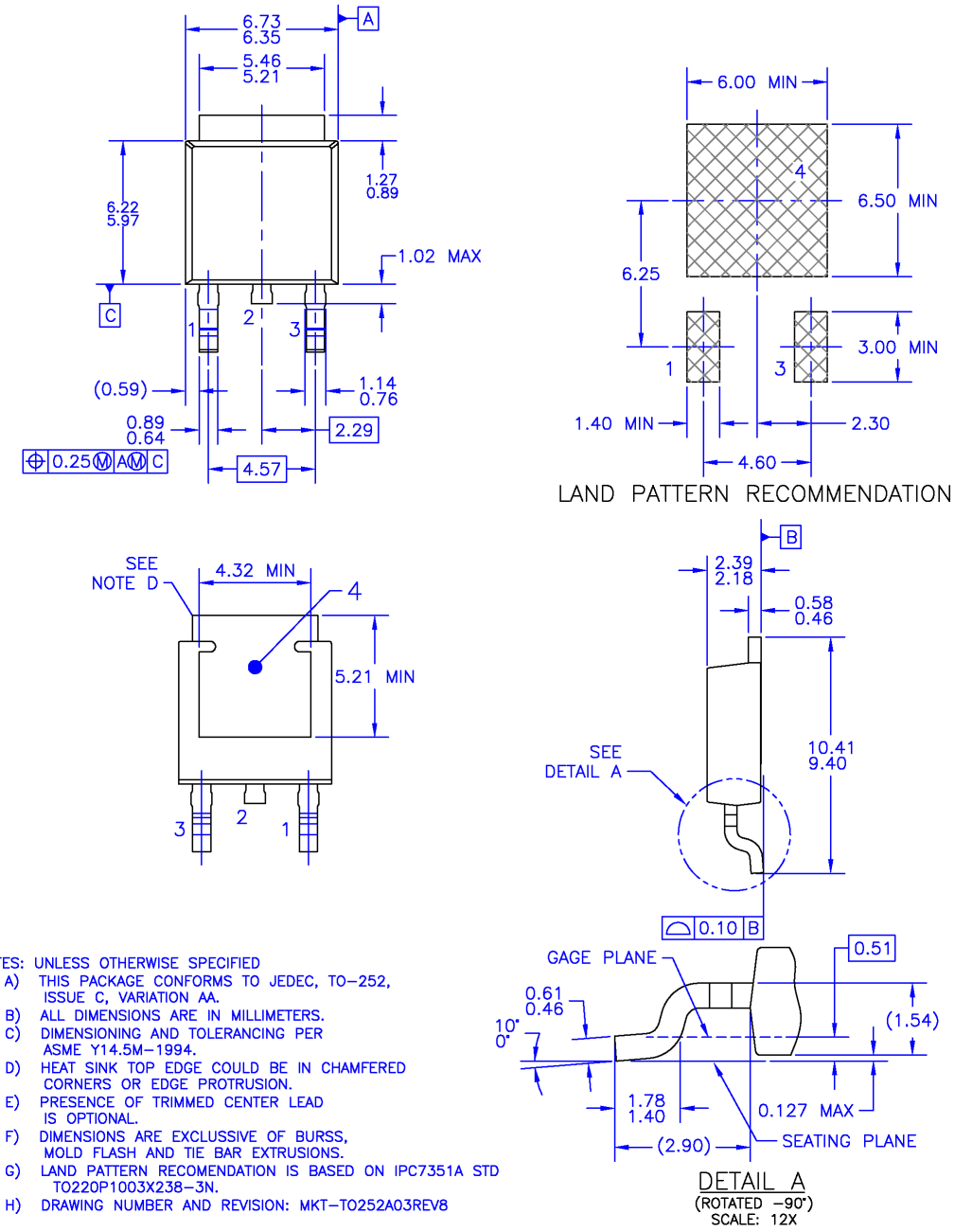
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Mechanical Dimensions

# D-PAK

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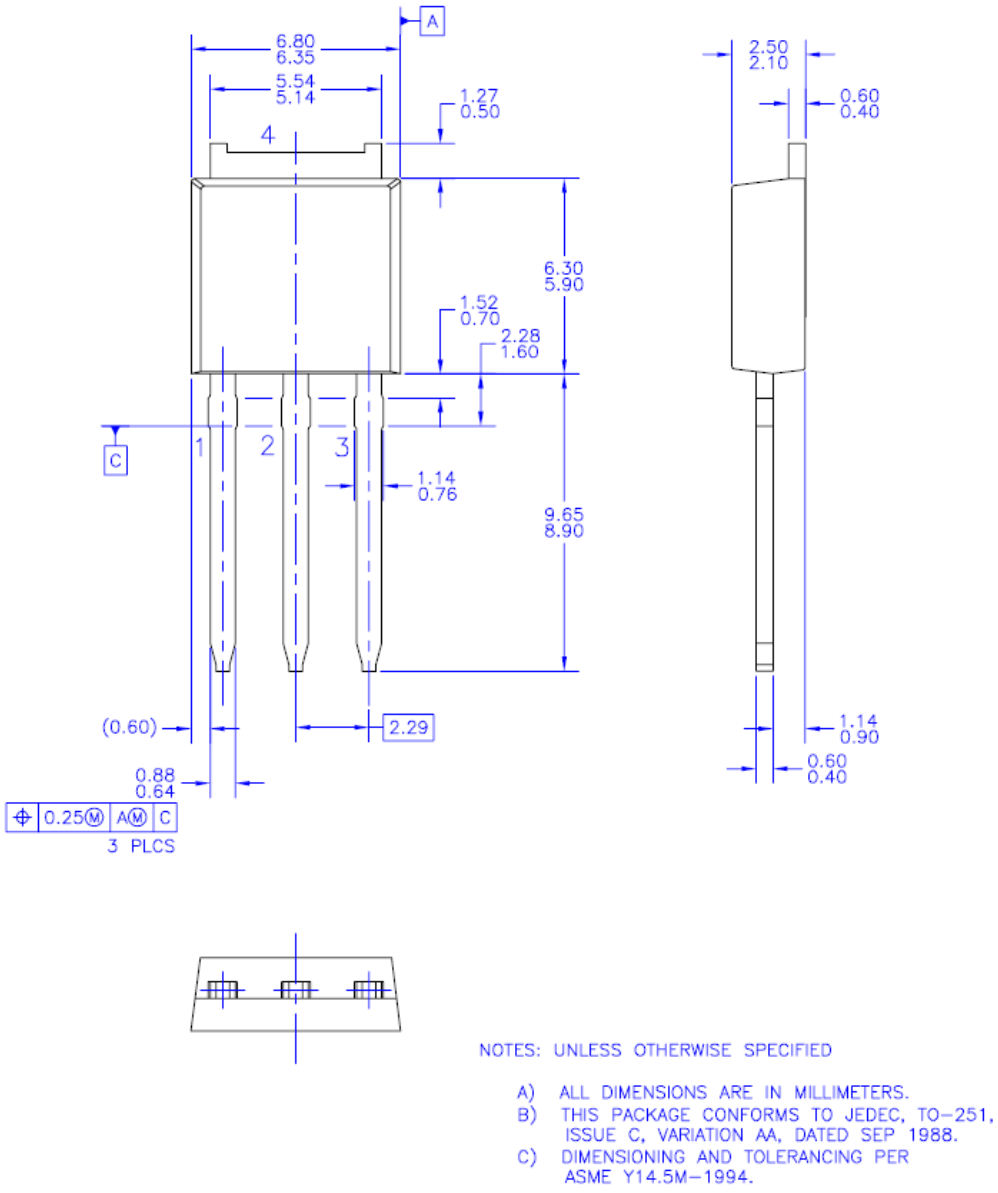
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Dimensions in Millimeters

## Mechanical Dimensions

# I-PAK

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Dimensions in Millimeters

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