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April 1st, 2010
Renesas Electronics Corporation

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HA16163T

Synchronous Phase Shift Full-Bridge Control IC

REJ03F0001-0600
Rev.6.00
Jul 01, 2008

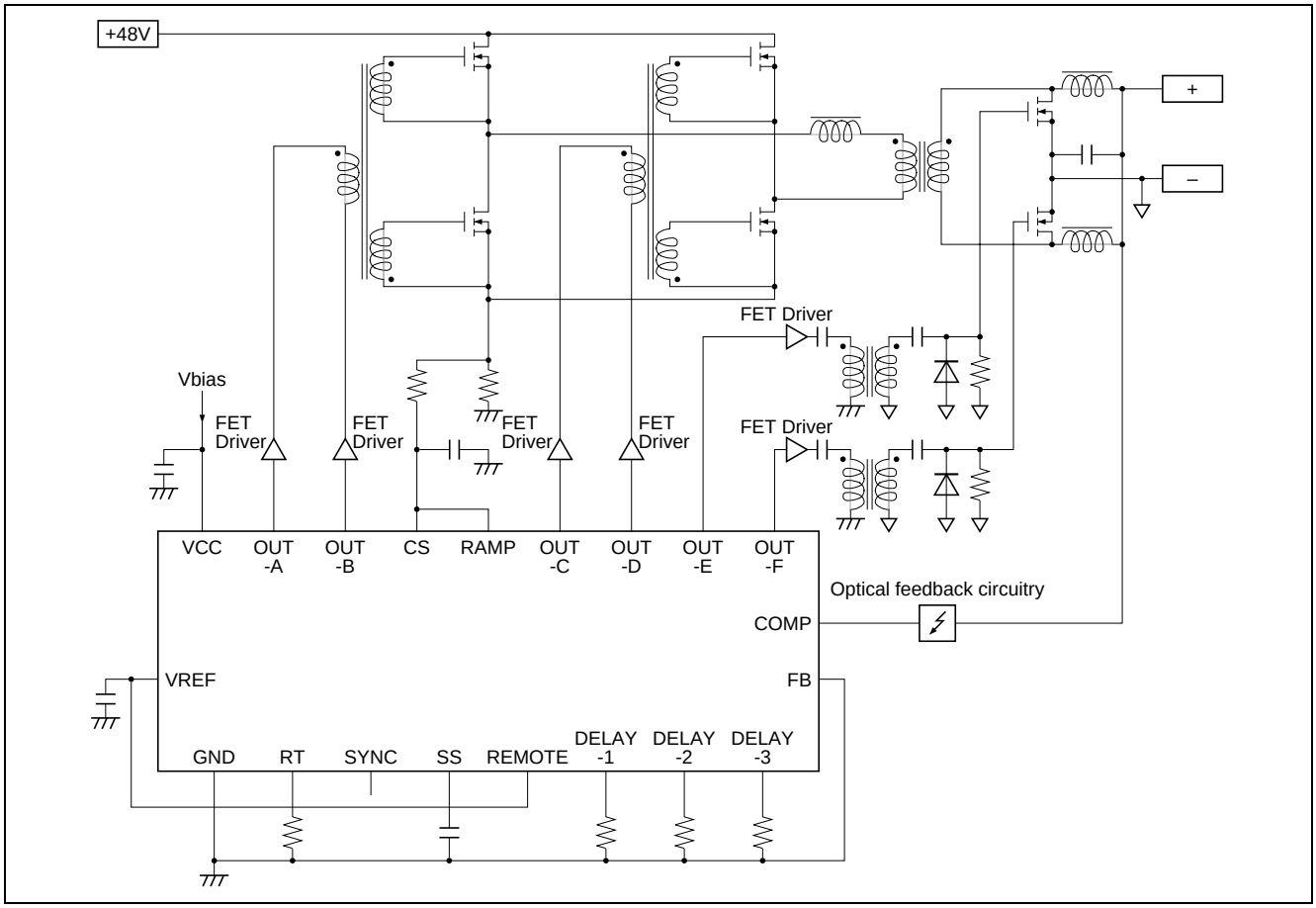
Features

- High frequency operation; oscillator frequency = 2 MHz max.
- Full-bridge phase-shift switching circuit with adjustable delay times
- Integrated secondary synchronous rectification control with adjustable delay times
- Three-level over current protection; pulse by pulse, timer Latch, one shot OCP
- Package: TSSOP-20

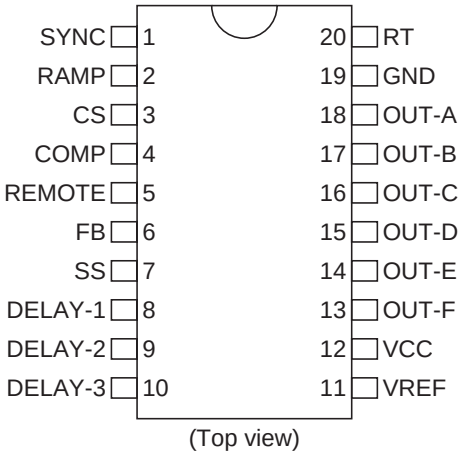
Application

- 48 V input isolated DC/DC converter
- Primary; Full-bridge circuit topology
- Secondary; current doubler or center-tapped rectification

Illustrative Circuit



Pin Arrangement

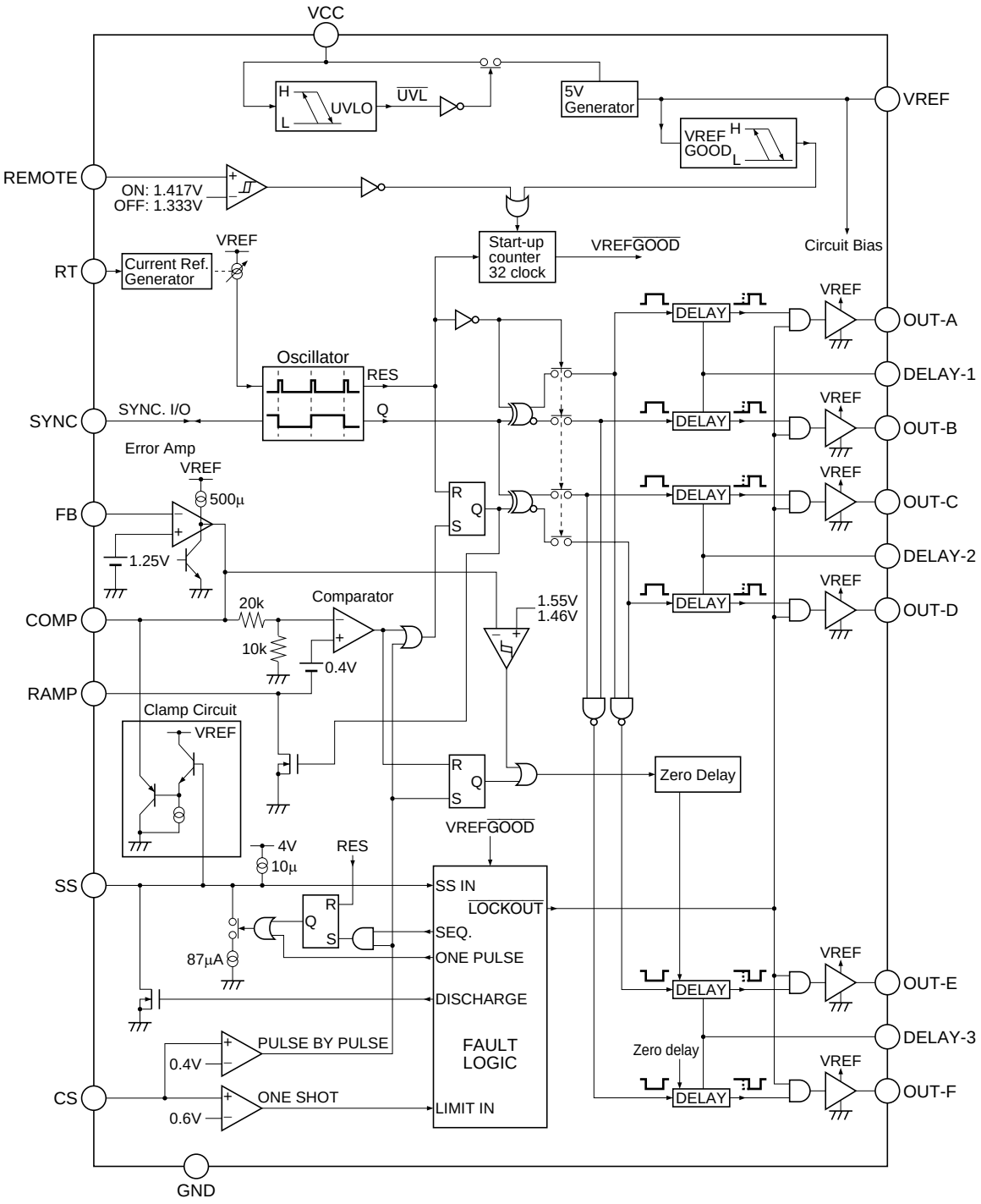


(Top view)

Pin Functions

Pin No.	Pin Name	Pin Function
1	SYNC	Synchronization I/O for the oscillator
2	RAMP	Current sense signal input for the full-bridge control loop
3	CS	Current sense signal input for OCP
4	COMP	Error amplifier output
5	REMOTE	Remote on/off control
6	FB	Voltage feedback input
7	SS	Timing capacitor for both soft start and timer latch
8	DELAY-1	Delay time adjustor for the full-bridge control signal (OUT-A and B)
9	DELAY-2	Delay time adjustor for the full-bridge control signal (OUT-C and D)
10	DELAY-3	Delay time adjustor for the secondary control signal (OUT-E and F)
11	VREF	5 V/20 mA Output
12	VCC	IC power supply input
13	OUT-F	Secondary control signal
14	OUT-E	Secondary control signal
15	OUT-D	Full-bridge control signal
16	OUT-C	Full-bridge control signal
17	OUT-B	Full-bridge control signal
18	OUT-A	Full-bridge control signal
19	GND	Ground level for the IC
20	RT	Timing resistor for the oscillator

Block Diagram



Note that all switches in the block diagram are turned on when control signal is high.

Absolute Maximum Ratings

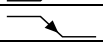
(Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Power supply voltage	Vcc	20	V	1
Peak output current	Ipk-out	±50	mA	2, 3
DC output current	Idc-out	±5	mA	3
VREF output current	Iref-out	–20	mA	3
COMP sink current	Isink-comp	2	mA	3
DELAY set current	Iset-delay	0.3	mA	3
RT set current	Iset-rt	0.3	mA	3
VREF terminal voltage	Vter-ref	–0.3 to 6	V	1, 4
Terminal group 1 voltage	Vter-1	–0.3 to (Vref +0.3)	V	1, 5
Operating junction temperature	Tj-opr	–40 to +125	°C	6
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are with reference to the GND pin.
2. Shows the transient current when driving a capacitive load.
3. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
4. VREF pin voltage must not exceed VCC pin voltage.
5. Terminal group 1 is defined the pins;
REMOTE, CS, RAMP, COMP, FB, SS, RT, SYNC, DELAY-1 to 3, OUT-A to F
6. θja
228°C/W Board condition; Glass epoxy 55 mm × 45 mm × 1.6 mm, 10% wiring density.

Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, RT = 33 kΩ, Rdelay = 51 kΩ, unless otherwise specified.)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	9.0	9.8	10.6	V	
	Shutdown threshold	VL	7.3	7.9	8.5	V	
	UVLO hysteresis	dV_{UVL}	1.7	1.9	2.1	V	
	Start-up current	Is	—	90	150	μA	Vcc = 8.5V
	Operating current	Icc	—	7	10	mA	No load on VREF pin
VREF	Output voltage	Vref	4.9	5.0	5.1	V	
	Line regulation	Vref-line	—	0	10	mV	Vcc = 10V to 16V
	Load regulation	Vref-load	—	6	20	mV	Iref = –1mA to –20mA
	Temperature stability	dVref/dTa	—	±80 *1	—	ppm/°C	Ta = –40 to 105°C
Oscillator	Oscillator frequency	fosc	—	960 *1	—	kHz	
	Switching frequency	fsw	412	480	547	kHz	Measured on OUT-A, -B
	Line stability	fsw-line	–1.5	0	1.5	%	Vcc = 10V to 16V
	Temperature stability	dfsw/dTa	—	±0.1 *1	—	%/°C	Ta = –40 to 105°C
	RT voltage	V_{RT}	2.5	2.7	2.9	V	
SYNC	Input threshold	$V_{TH\text{-}SYNC}$	2.5	2.85	3.2	V	
	Output high	$V_{OH\text{-}SYNC}$	3.5	4.0	—	V	R_{SYNC} = 33kΩ to GND
	Output low	$V_{OL\text{-}SYNC}$	—	0.05	0.15	V	R_{SYNC} = 33kΩ to VREF
	Minimum input pulse	$T_{I\text{-}MIN}$	50	—	—	ns	
	Output pulse width	$T_{O\text{-}SYNC}$	—	500	—	ns	
Remote	On threshold voltage	V_{ON}	1.374	1.417	1.460	V	
	Off threshold voltage	V_{OFF}	1.293	1.333	1.373	V	
	Input bias current	I_{REMOTE}	0	0.4	2	μA	REMOTE = 2V
Error amplifier	FB input voltage	V_{FB}	1.225	1.250	1.275	V	FB and COMP are shorted
	FB input current	I_{FB}	–1.0	0	1.0	μA	FB = 1.25V
	Open-loop DC gain	Av	—	80 *1	—	dB	
	Unity gain bandwidth	BW	—	2 *1	—	MHz	
	Output source current	I_{SOURCE}	–610	–430	–350	μA	FB = 0.75V, COMP = 2V
	Output sink current	I_{SINK}	2.0	6.5	—	mA	FB = 1.75V, COMP = 2V
	Output high voltage	$V_{OH\text{-}EO}$	3.7	3.9	—	V	FB = 0.75V, COMP; open
	Output low voltage	$V_{OL\text{-}EO}$	—	0.1	0.4	V	FB = 1.75V, COMP; open
	Output clamp voltage *2	$V_{CLAMP\text{-}EO}$	–0.16	–0.07	0.0	V	FB = 0.75V, COMP; open SS = 1V

Notes: 1. Reference values for design. Not 100% tested in production.

2. $V_{CLAMP\text{-}EO} = V_{COMP}$ – SS voltage (1V)

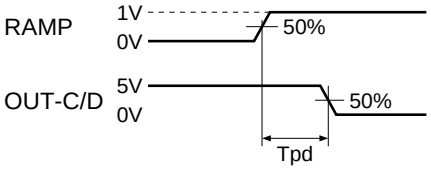
Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 33 kΩ, Rdelay = 51 kΩ, unless otherwise specified.)

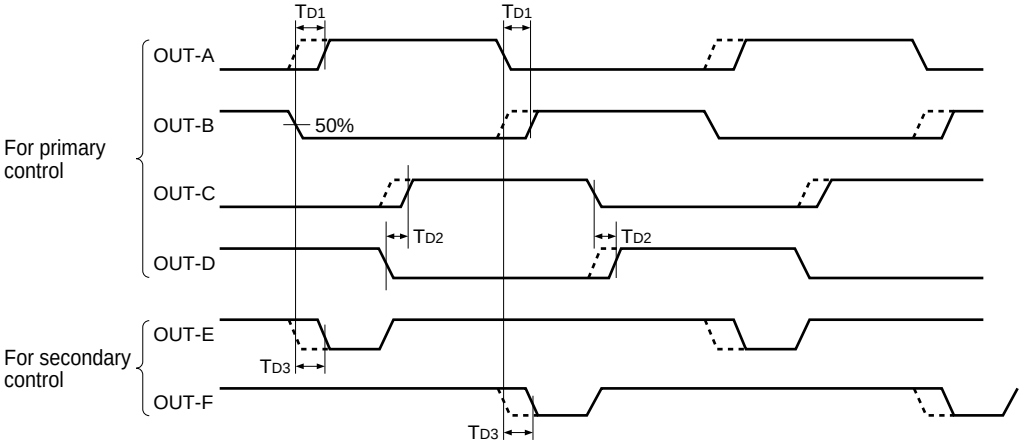
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Phase modulator	RAMP offset voltage	V_{RAMP}	—	0.4 *1	—	V	
	RAMP bias current	I_{RAMP}	–5	–0.8	5	µA	RAMP = 0.3V
	RAMP sink current	$I_{SINK-RAMP}$	8	26	—	mA	RAMP = 1V, COMP = 0V
	Minimum phase shift	Dmin	—	0 *1 *4	—	%	RAMP = 1V, COMP = 0V
	Maximum phase shift	Dmax	—	97.0 *1 *4	—	%	RAMP = 0V, COMP = 2.1V
	Delay to OUT-C, -D *2	Tpd	—	30	60	ns	COMP = 2.1V
Delay	DELAY-1, -2, -3 *3	$T_{D1, 2, 3}$	22	33.5	45	ns	Delay set R = 51k
	Terminal voltage	$V_{D1, 2, 3}$	1.9	2.0	2.1	V	Delay set R = 51k
Soft start	Source current	I_{SS}	–14	–10	–6	µA	SS = 1V
	Discharge current	I_{RES-SS}	5	10	—	mA	SS = 1V, REMOTE = 0V
	Soft-start reset voltage	V_{RES-SS}	0.25	0.40	0.55	V	Measured on SS
	SS high voltage	V_{OH-SS}	3.9	4.0	4.1	V	

Notes: 1. Reference values for design. Not 100% tested in production.

2. Tpd is defined as;

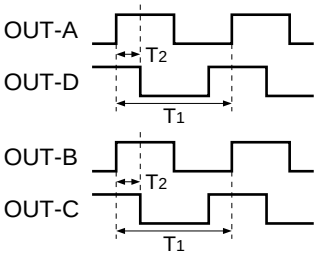


3. $T_{D1, 2, 3}$ are defined as;



4. Maximum/Minimum phase shift is defined as;

$$D = \frac{T_2}{T_1} \times 2 \times 100 \ (\%)$$

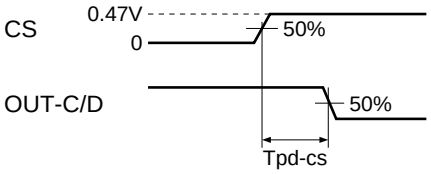


Electrical Characteristics (cont.)

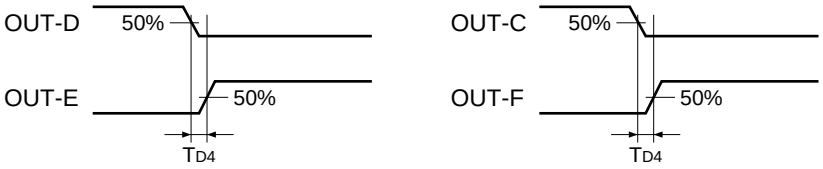
(Ta = 25°C, Vcc = 12 V, RT = 33 kΩ, Rdelay = 51 kΩ, unless otherwise specified.)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Over current protection	Pulse-by-pulse current limit threshold	V_{CS-PP}	0.36	0.40	0.44	V	
	One-shot OCP threshold	V_{CS-SD}	0.54	0.60	0.66	V	
	Delay to OUT pins *1	Tpd-cs	—	40	80	ns	CS = 0V to 0.47V
	Timer latch integration time	T_{TL}	44	63	82	µs	CS = 0.47V step function, SS = 0.022µF
Output	High voltage	V_{OH-OUT}	4.3	4.8	—	V	IOUT = –5mA
	Low voltage	V_{OL-OUT}	—	0.1	0.4	V	IOUT = 5mA
	Rise time	tr	—	5	15	ns	C_{OUT} = 33pF
	Fall time	tf	—	5	15	ns	C_{OUT} = 33pF
	Timing offset *2	T_{D4}	—	3 *3	—	ns	

Notes: 1. Tpd-cs is defined as;



2. T_{D4} is defined as;

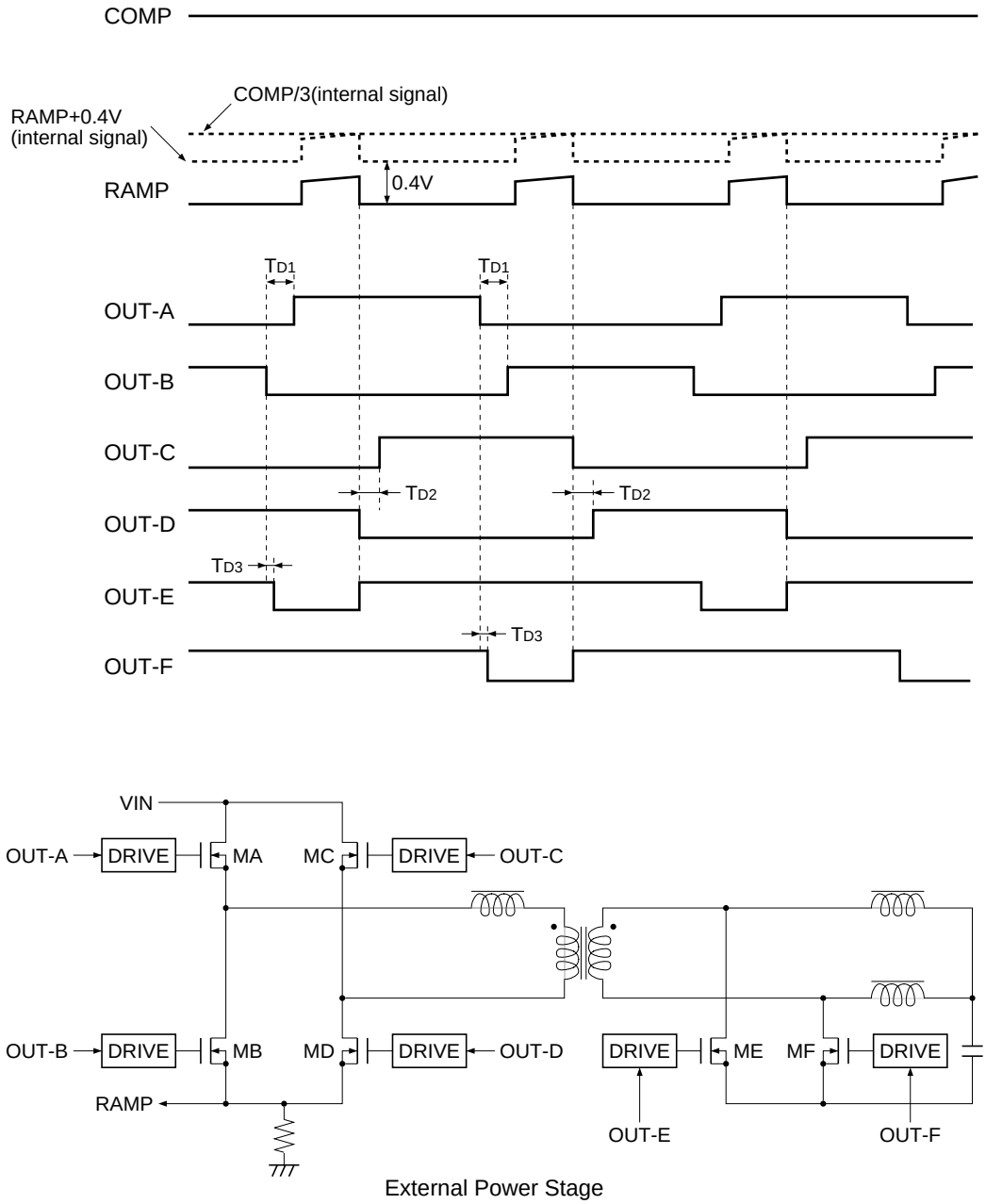


3. Reference values for design. Not 100% tested in production.

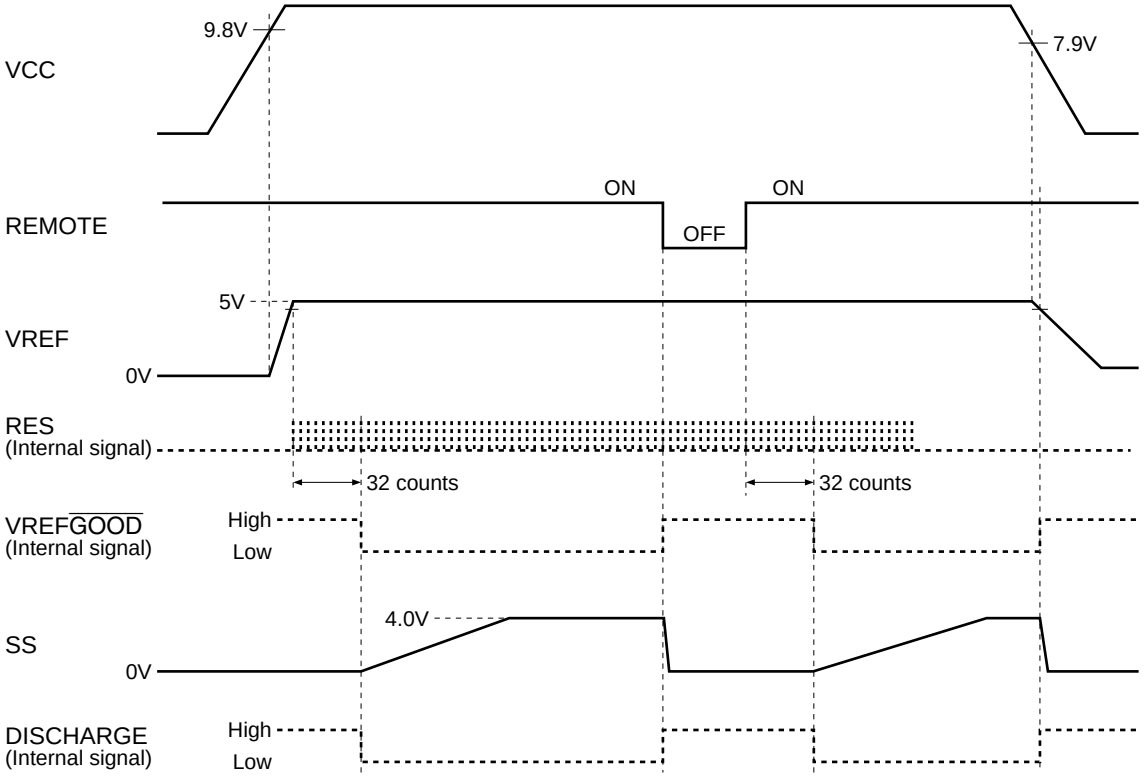
Timing Diagram

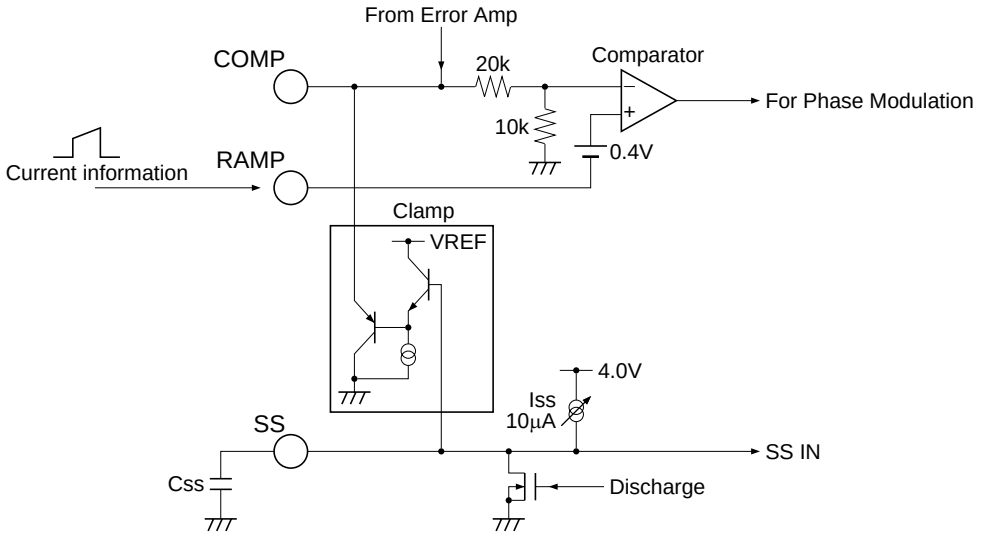
Note: All voltage, current, time shown in the diagram is typical value.

Full Bridge and Secondary Control



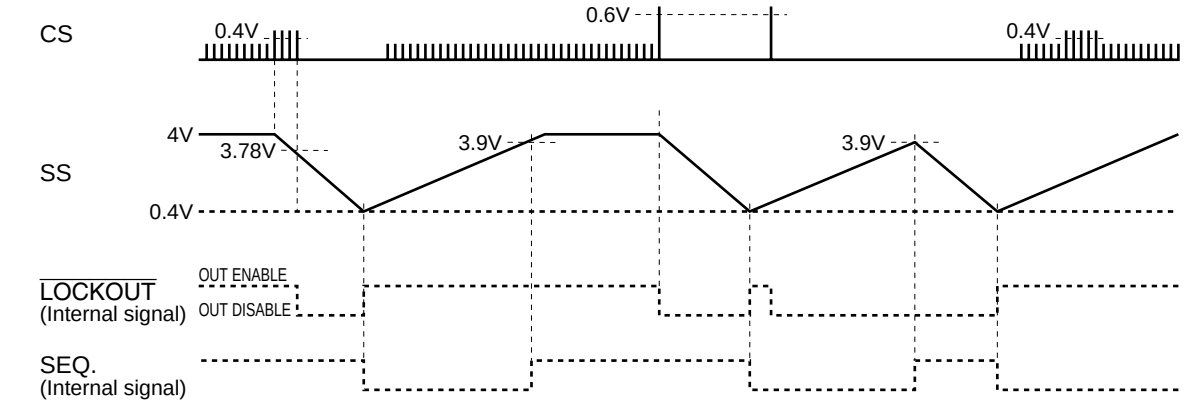
Start-up and Shutdown

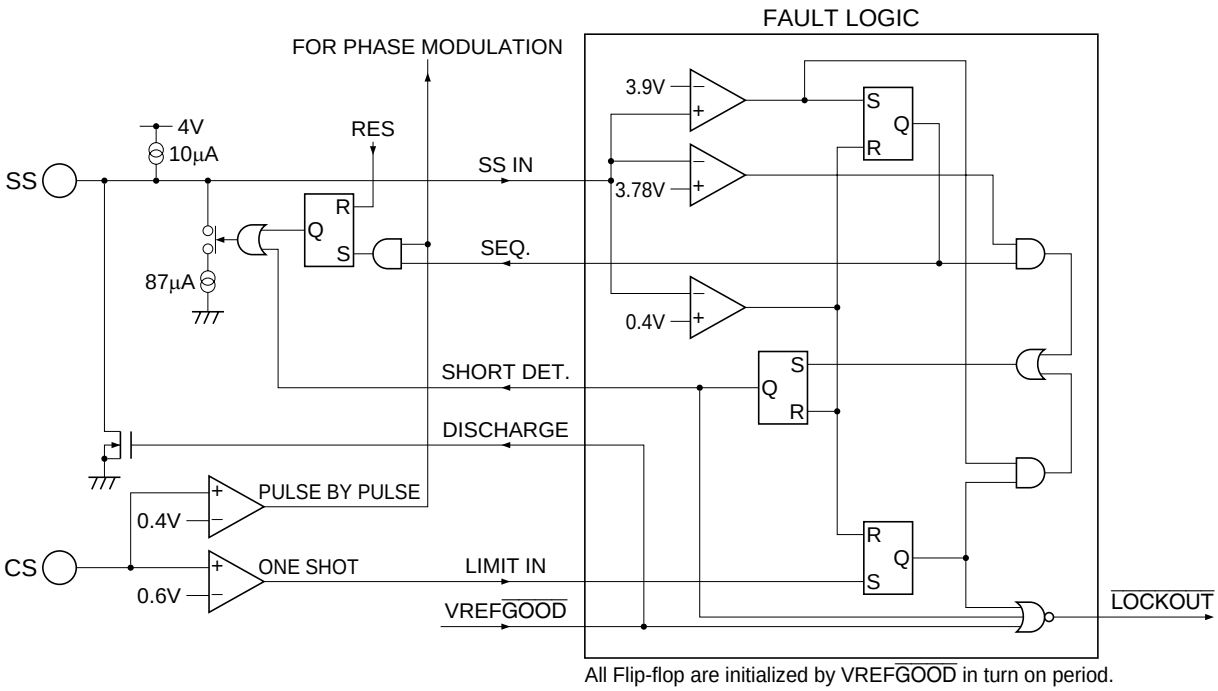




Soft-start Block

Timer Latch and One Shot OCP





OCP Block

SS IN : Voltage detector input of SS pin.
SEQ. : Timer Latch function is not activated when SEQ. signal is Low.
SHORT DET. : Once ONE SHOT comparator detect short current in the power supply, SHORT DET. is High until SS voltage reaches down to 0.4V.
DISCHARGE : Gate control for SS capasitor reset.
LIMIT IN : One shot OCP input.
LOCKOUT : Lock-out signal for OUT-A to F.
VREFGOOD : System reset signal. VREFGOOD is High when either VREF<4.6V or Remote off mode.

Functional Description

Note: All voltage, current, time shown in the diagram is typical value unless otherwise noted.

UVLO

UVLO (Under Voltage Lockout Operation) is a function that halts operation of the IC in the event of a low IC power supply voltage.

When IC operation is halted, the 5 V internal voltage generation circuit (VREF) halts, and therefore operation of circuitry using VREF as the operating power supply halts. Circuit blocks other than UVLO use VREF as their operating power supply. Therefore, the power supply current of the IC becomes equal to the current dissipated by the UVLO circuit. The following graphs show the relationship between the VCC input current and VCC input voltage, and between VREF and the VCC input voltage.

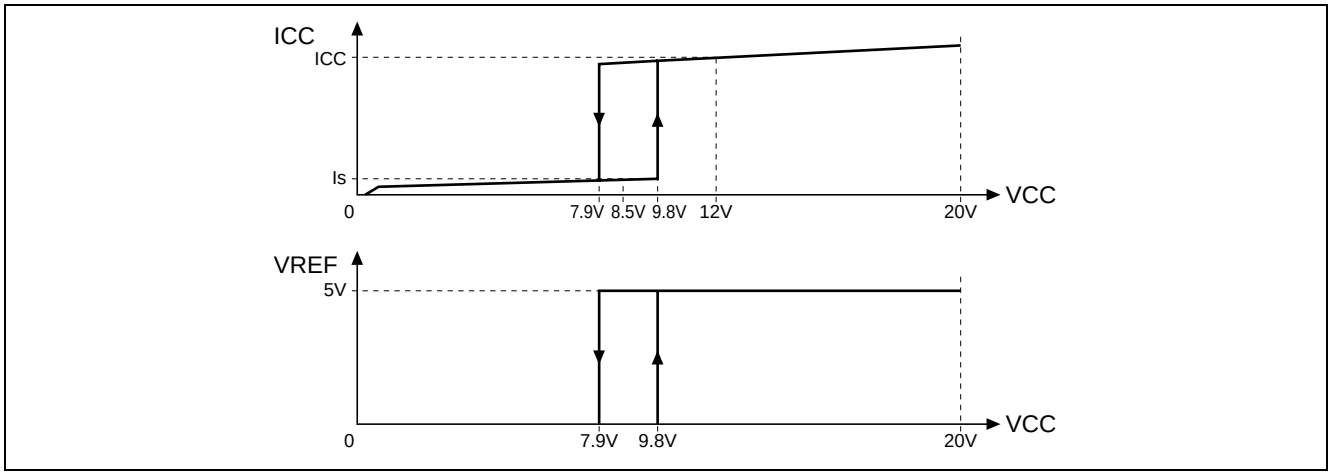


Figure 1

REMOTE

IC outputs (OUT-A through OUT-F) can be halted by means of the REMOTE pin. In this case, the IC output logic level is low.

In the remote off state, VREF output is not halted, and therefore the current dissipation of the IC does not decrease to the start-up level. Also, control by means of the REMOTE pin is not possible when the IC has been halted by UVLO.

The soft start capacitance is discharged in the remote off state. Therefore, operation begins from soft start mode when the next remote on operation is performed. The relationship between the REMOTE pin and the operating mode of the IC is shown in the following figure.

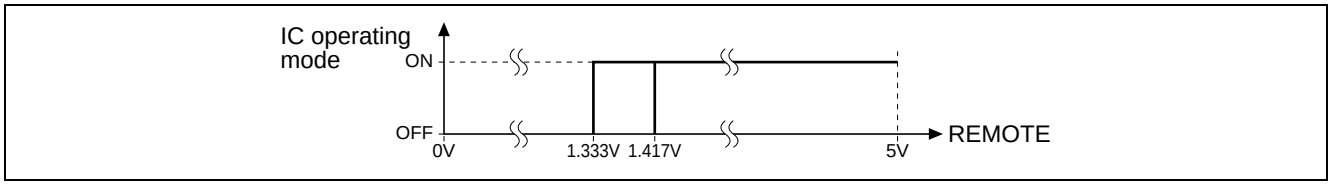


Figure 2

The remote on and off threshold voltages are provided with hysteresis of 84 mV (typ). Remote control can be performed by means of analog input as shown in the diagram below as well as by means of logic control. The following diagram shows an example in which the power supply set input voltage is sensed by means of the REMOTE pin, and the power supply set start-up voltage is set to 34 V, and the shutdown voltage to 32 V.

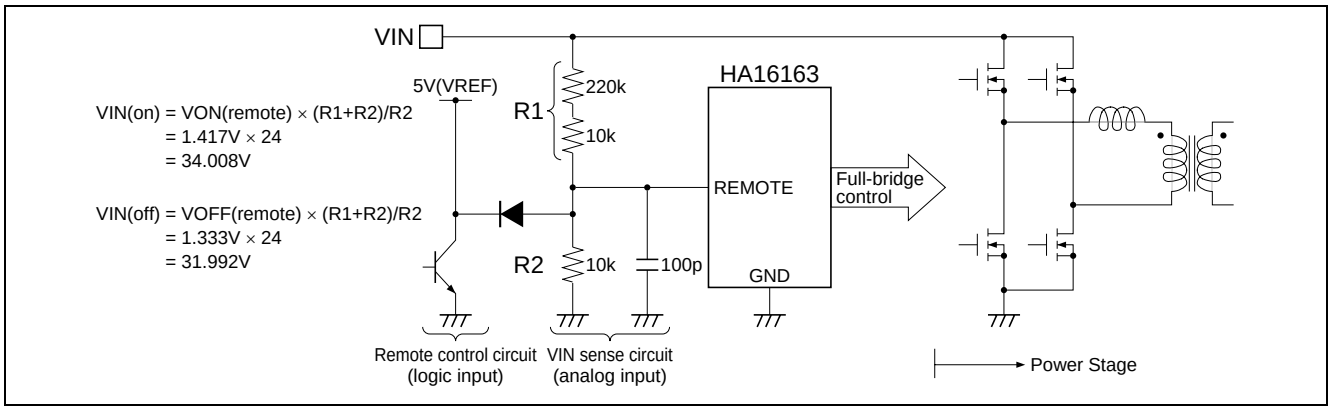


Figure 3

Start-up Counter

When the VREF$\overline{\text{GOOD}}$ signal (internal signal) goes to the logic low level, the HA16163 starts operating as a controller. The VREF$\overline{\text{GOOD}}$ signal is created from the REMOTE comparator and VREFGOOD circuit output via a 32-clock start-up counter.

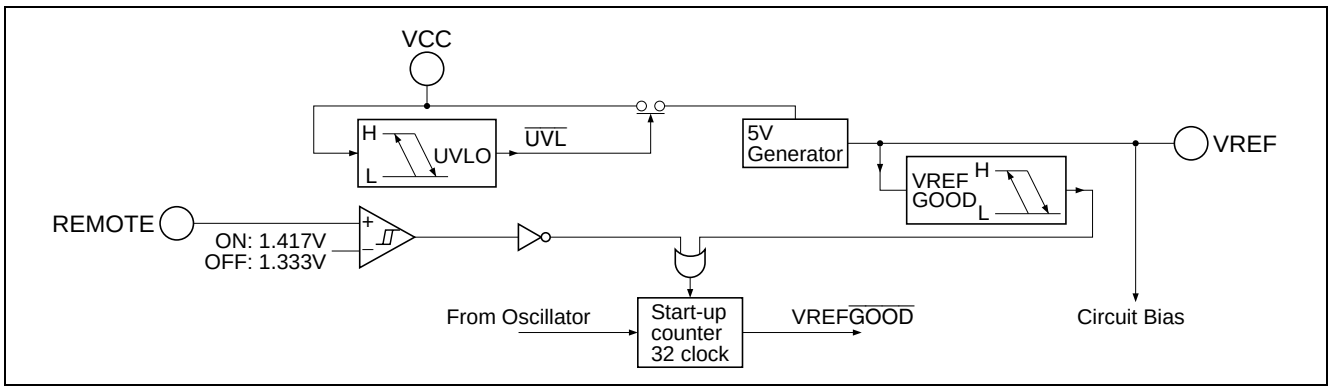


Figure 4

Therefore, the start of IC operation is a 32-count later than UVLO release or the remote on trigger. When the oscillator frequency is set to 1 MHz, this represents a delay of 32 μs. This delay enables operation to be halted until VREF (5 V) stabilizes when UVLO is released. Note that the start-up counter operates when VREF rises or when a remote on operation is performed, but does not operate when VREF falls or when a remote off operation is performed (there is no logic delay due to the start-up counter).

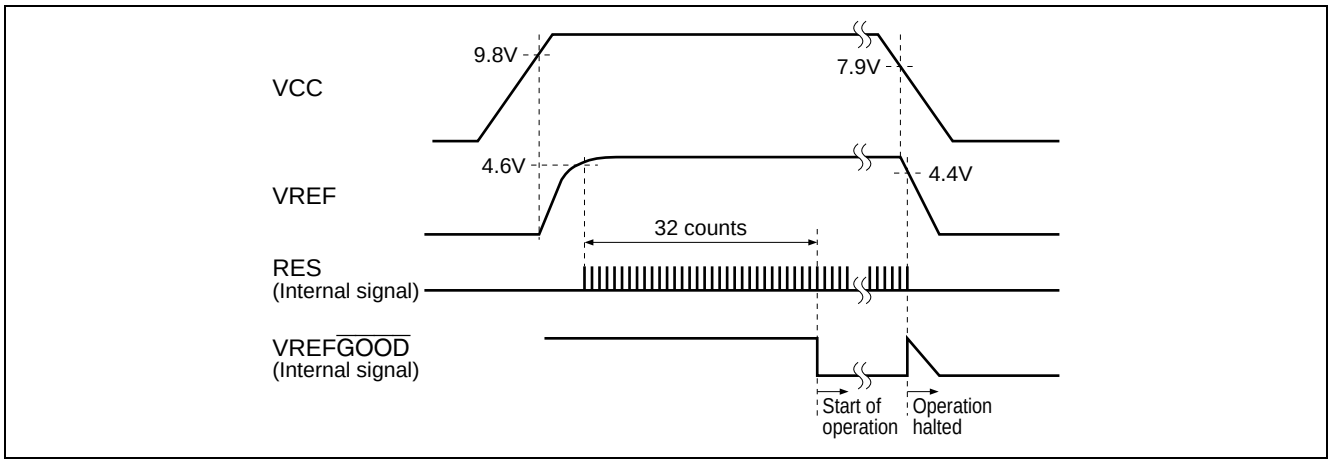


Figure 5

Oscillator

The oscillation frequency of the oscillator is set by means of a resistance connected between the RT pin and GND. The following graph shows the relationship between the external resistance and the oscillation frequency. The typical value of the oscillation frequency is given by the following equation.

$$fosc = \frac{1}{25\ [pF] \times RT\ [\Omega] + 150\ [ns]} \quad [Hz]$$

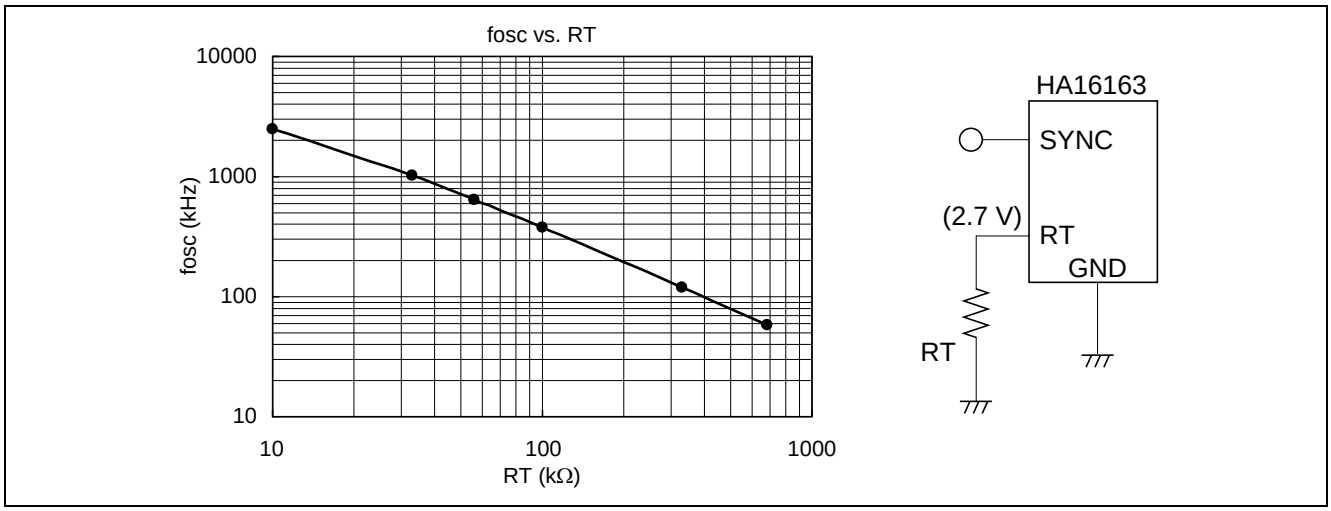


Figure 6

Place the resistor for connection to the RT pin as close to the pin as is possible. Please design the pattern so that the level of cross-talk from other signals is minimized.

Synchronized Operation

Parallel synchronized operation is possible by connecting the SYNC pins of HA16163s. In this case, up to four slave ICs can be connected to one master IC. A value of at least twice the master RT value should be set for the slave IC RT values.

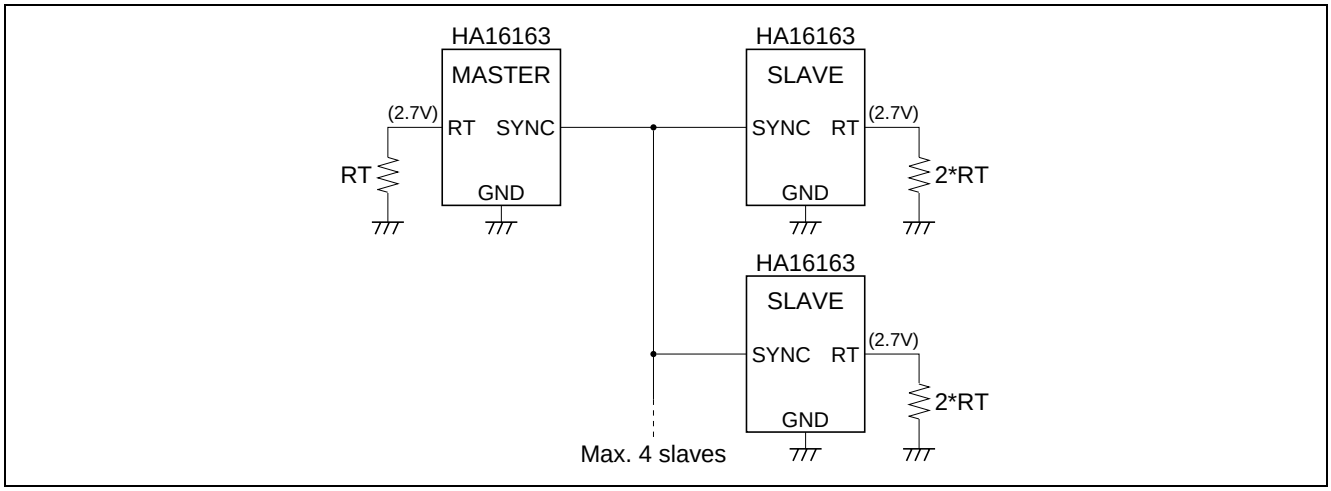


Figure 7 Parallel Synchronized Operation

External synchronized operation is possible by supplying a synchronization signal to the SYNC pins of HA16163s. In this case, a frequency not exceeding 1/2 that of the master clock should be set for the HA16163s.

A maximum master clock frequency of 4 MHz should be used. See the figure below for the input waveform conditions.

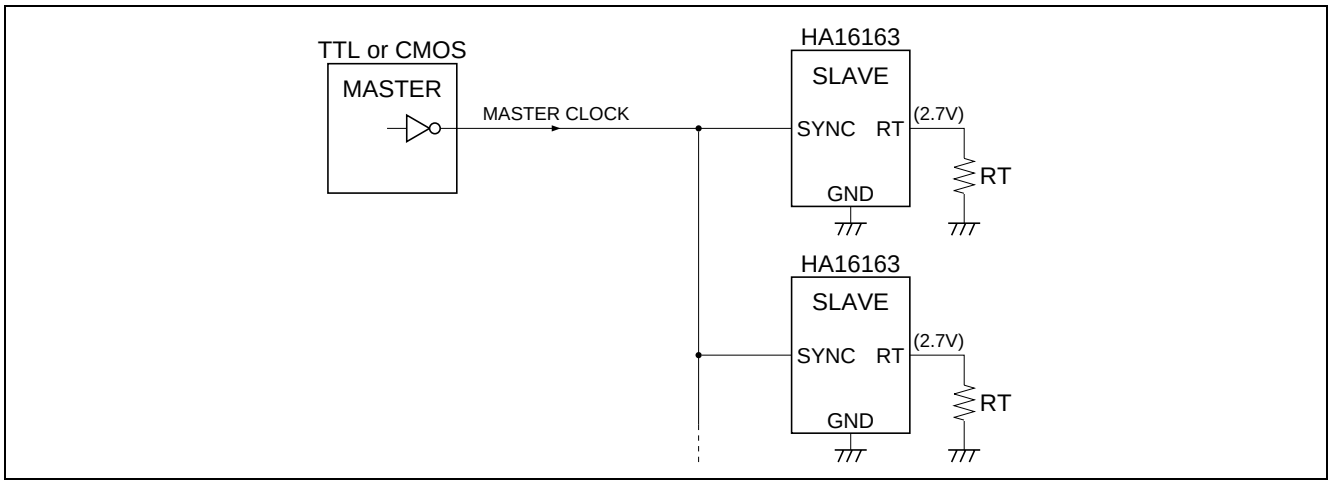
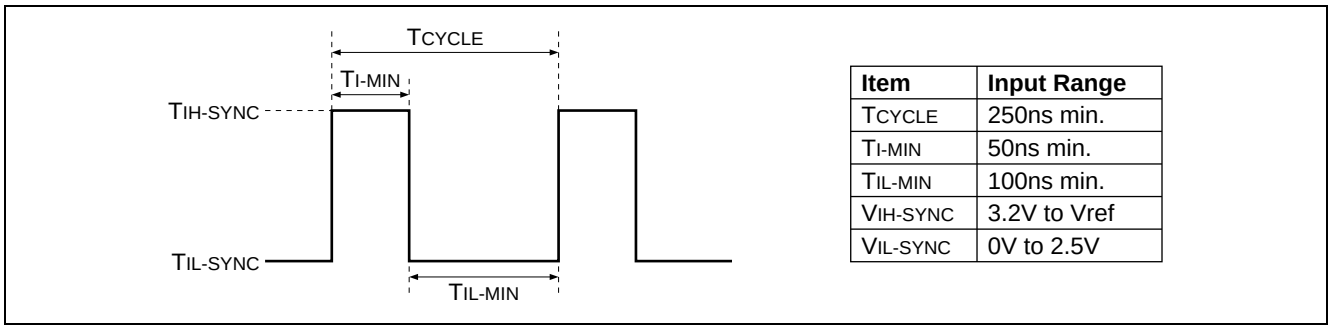


Figure 8 External Synchronized Operation



Item	Input Range
T_{CYCLE}	250ns min.
T_{I-MIN}	50ns min.
T_{IL-MIN}	100ns min.
$V_{IH-SYNC}$	3.2V to Vref
$V_{IL-SYNC}$	0V to 2.5V

Figure 9 SYNC Pin Input Conditions

Synchronous Phase Shift Full-Bridge Control

The HA16163 is provided with full-bridge control outputs OUT-A through OUT-D, and secondary-side synchronous rectification control outputs OUT-E and OUT-F. ZVS (Zero Voltage Switching) can be performed by adjusting timing delays T_{D1} and T_{D2} between the OUT-A through OUT-D outputs by means of an external resistance. OUT-E and OUT-F have an output timing suitable for secondary-side full-wave rectification, and so can be used in either current doubler or center tap applications. The following figure shows full-bridge ZVS + current doubler operation using an ideal model.

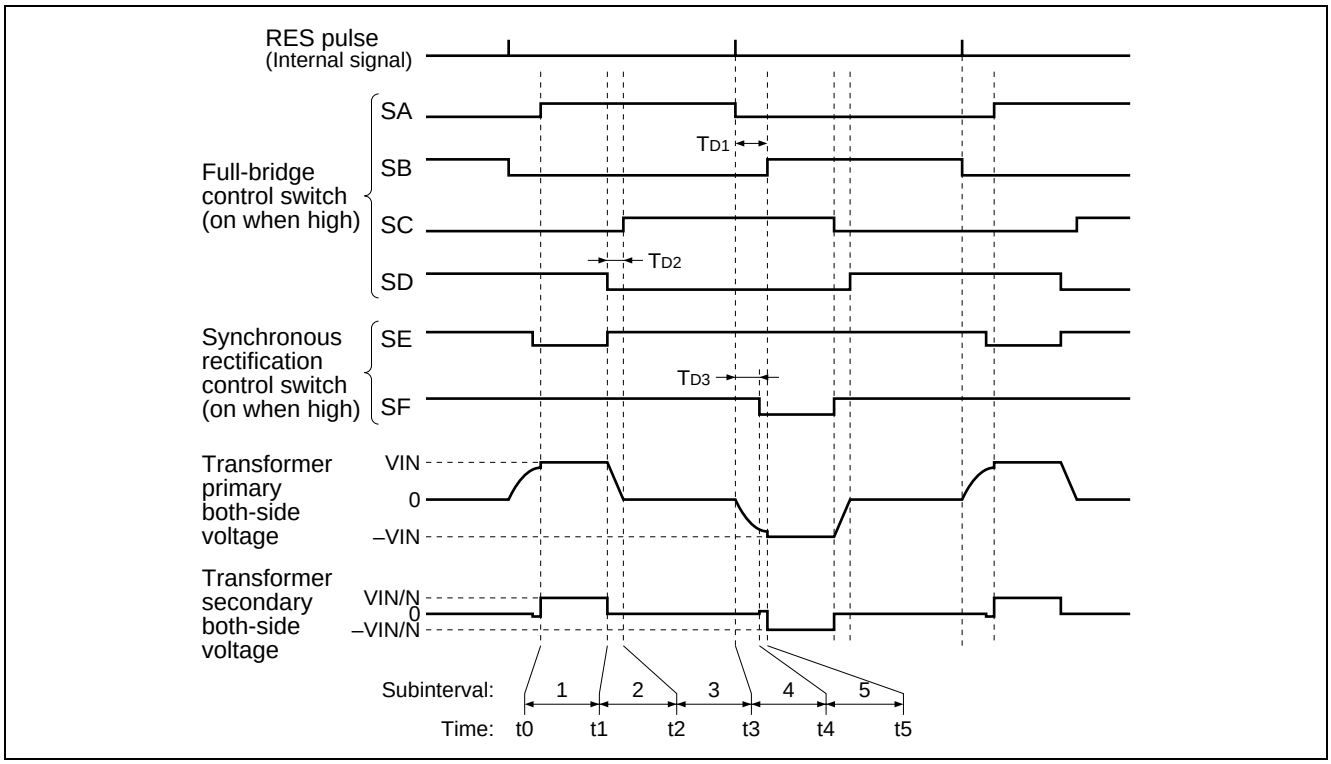
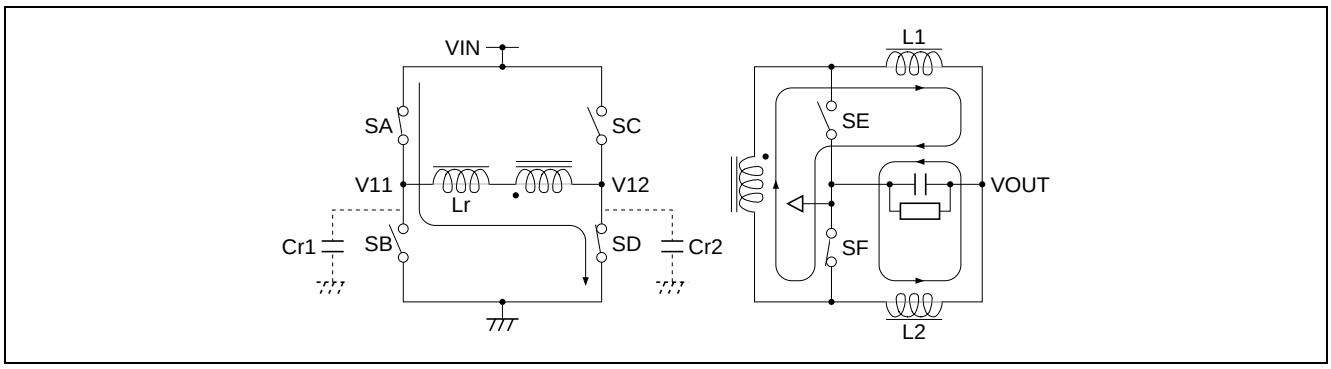


Figure 10

- Subinterval: 1
  In interval 1, SA and SD are turned on, and VIN is generated on the transformer primary side. On the transformer secondary side, a value proportional to the winding ratio is generated, and the primary-side power is transmitted to the load side.
  At this time, secondary-side switch SE is off and SF is on.



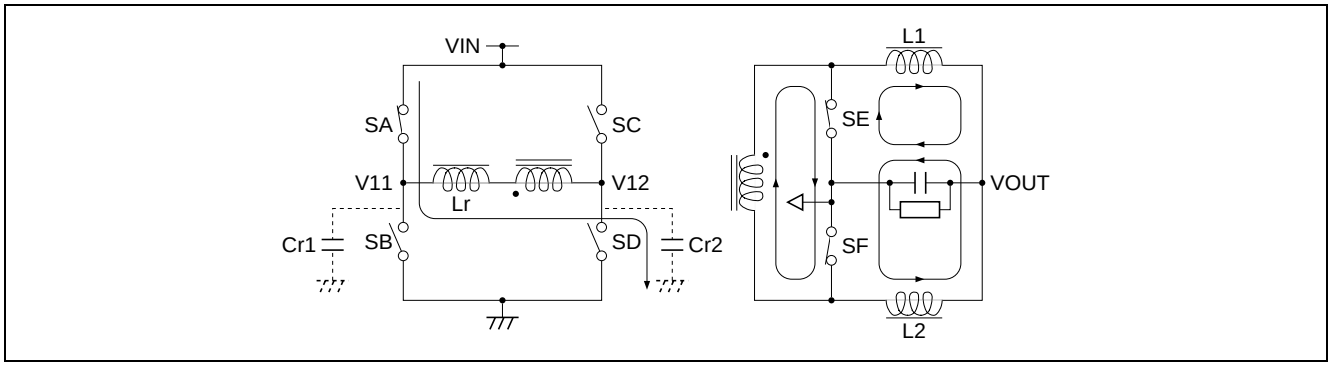
Subinterval: 1

- Subinterval: 2

  As SD is turned off at point t1, the primary-side current flows into resonant capacitance Cr2. At this time Cr2 is charged, and therefore the potential of V12 rises. Considering that the exciting current and the L1 and L2 ripple currents are considerable smaller than Io, the following is an approximate equation for the slope of V12.

$$\frac{dV12}{dt} = \frac{0.5\ Io}{N} \cdot \frac{1}{Cr2} \quad [V/s] \qquad \cdots\cdots(1)$$

  Here, N is the ratio of the primary coil to the secondary coil (N = N1/N2), and Io is the output current.
  As SE and SF are on, the transformer secondary side is in the shorted state, and the value of the current flowing up to that time is retained.



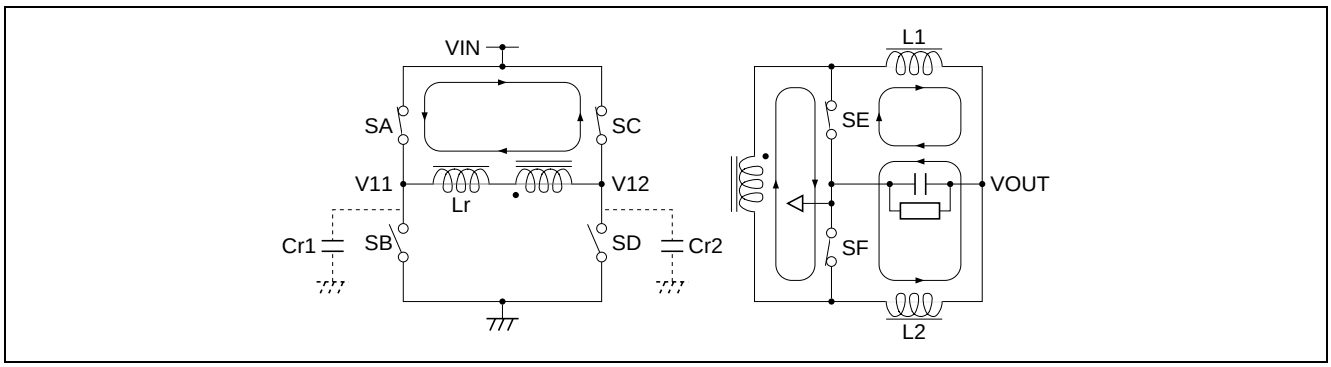
Subinterval: 2

- Subinterval: 3

  SC is turned on at point t2. ZVS operation can be attained by setting the SD off (t2) → SC on (t3) delay to the optimal value. This delay time can be expressed by equation (2).

$$TD2 = \frac{N}{0.5\ Io} \cdot Cr2 \cdot VIN \quad [s] \qquad \cdots\cdots(2)$$

  After SC is turned on, the transformer primary side is in the shorted state, and therefore the current value immediately after SC was turned on is retained.

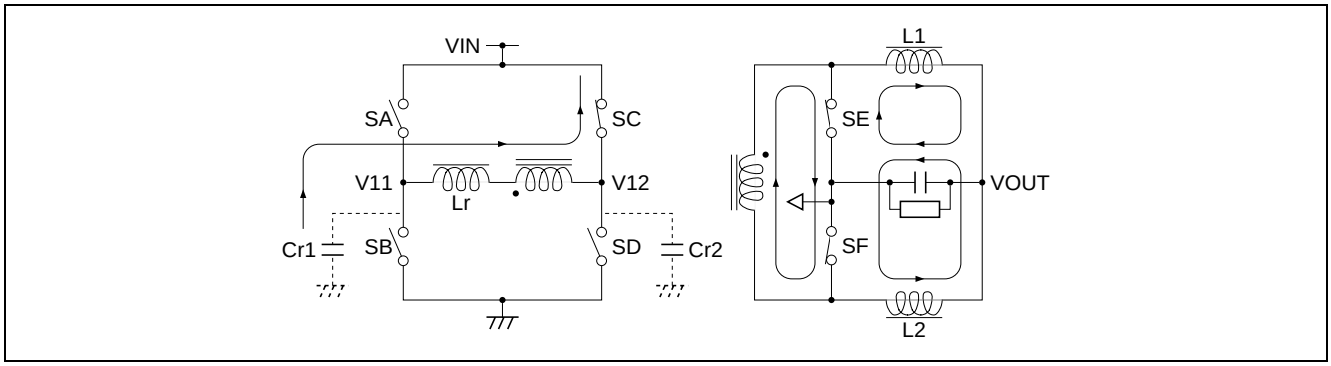


Subinterval: 3

- Subinterval: 4

  As SA is turned off at point t3, the primary-side current discharges resonant capacitance Cr1, and the potential of V11 falls. A negative potential is applied to resonant inductor Lr, and a flux reset starts. At this time, since the series resonance circuit is composed of Cr1 and Lr, the V11 waveform changes to a sine wave. The resonance frequency is given by equation (3).

$$fr = \frac{1}{2\pi\sqrt{(Cr1 \cdot Lr)}} \quad [Hz] \qquad \cdots\cdots(3)$$



Subinterval: 4

- Subinterval: 5

  When synchronous switch SF is turned off at point t4, the current flowing in SF up to that time continues to flow through the SF body diode. SF turn-off must be performed before completion of the resonant inductor Lr flux reset. If SF is not off on completion of the Lr flux reset, power transmission will be performed with the transformer secondary-side shorted, and therefore an excessive current will flow in the transformer primary and secondary sides, and parts may be damaged.

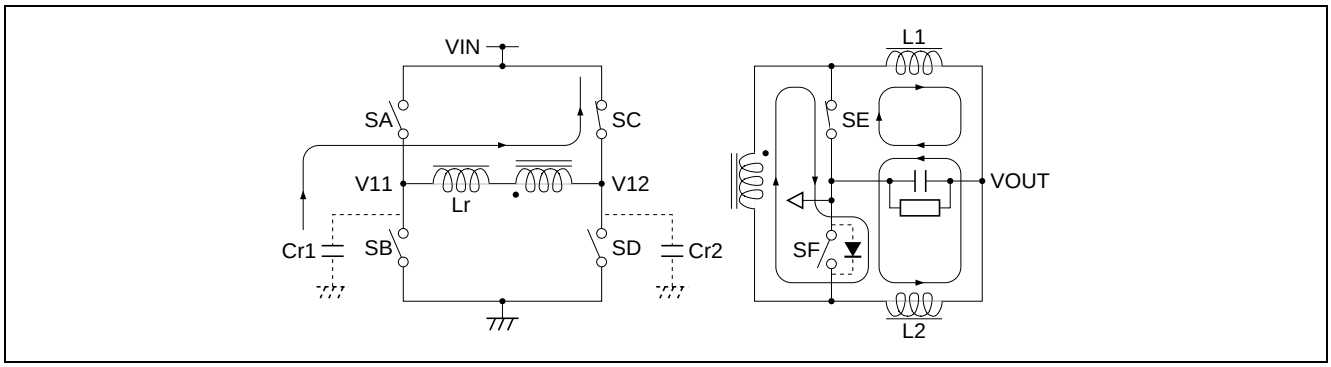
  Also, if the SF body diode is on for a long period, loss will be high. Therefore, optimal timing should be set by means of the HA16163's delay adjustment pin, DELAY-3.

  Lr reset time tr is given by equation (4) when the resonance voltage peak value is within the input voltage.

$$treset(Lr)|_{vpp \le VIN} = \frac{1}{4} \cdot \frac{1}{fr}$$
$$= 0.5\pi\sqrt{(Cr1 \cdot Lr)} \quad [s] \cdots\cdots(4)$$

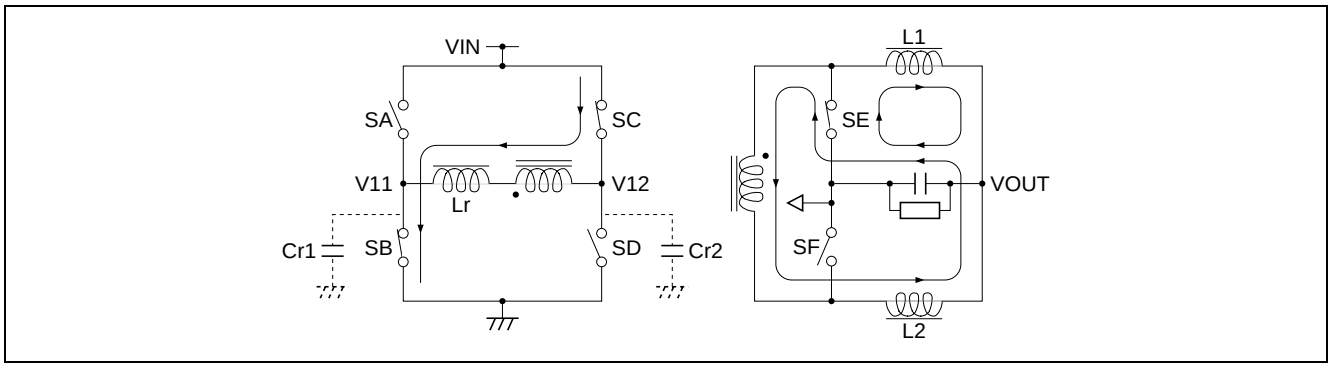
  Here, vpp is the resonance voltage peak value.

$$vpp = \frac{Io}{2} \cdot \frac{1}{N} \cdot \sqrt{(Lr/Cr1)} \quad [V] \qquad \cdots\cdots(5)$$



Subinterval: 5

- Time: t5
  SB is turned on at point t5. The SB switching loss can be minimized by turning on SB when the SB both-side voltages are at a minimum (when the resonance voltage is at a peak). The SB turn-on timing can be set with TD1 of the HA16163. The time when the resonance voltage is at a peak is given by equation (4).
  From t5 onward, operation is on the same principle as in Subinterval 1 through Subinterval 5.



Time: t5

Delay Setting

Inter-output delays (TD1, TD2, TD3) are set by means of a resistance connected between the DELAY-1 (-2, -3) pin and GND. The following graph shows the relationship between the external resistance and delay. The typical value of the delay set time is given by the following equation.

$$TD = 0.5\ [pF] \times RD\ [\Omega] + 8\ [ns] \quad [s]$$

When the RD value is small, the set time will be larger than the above calculated value due to the effect of internal delay, etc., and therefore a constant setting should be made with reference to the following graph.

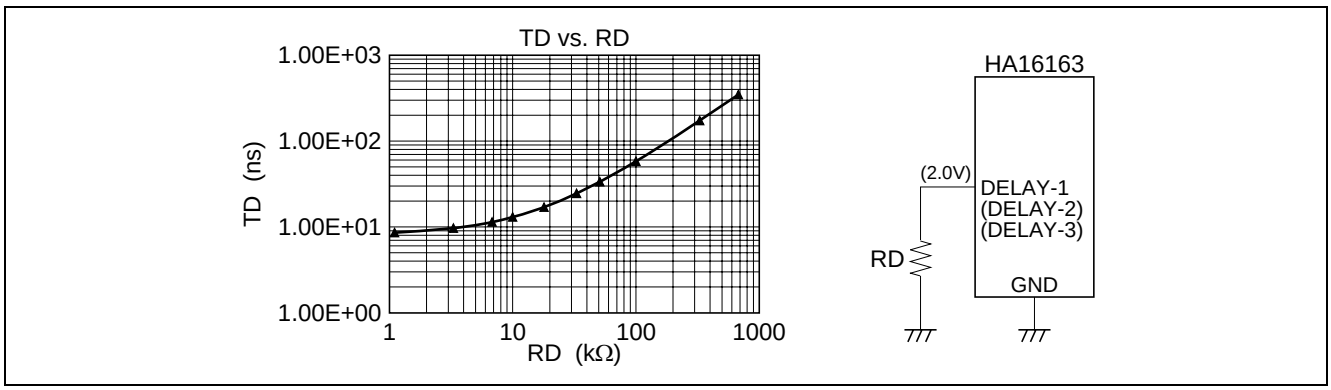


Figure 11

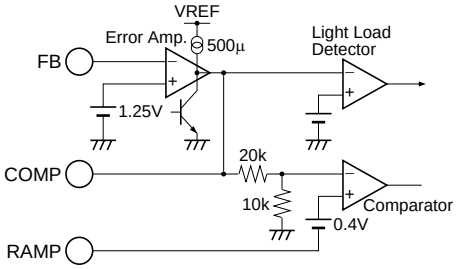
Place the resistor for connection to the DELAY-1,2,3 pin as close to the pin as is possible. Please design the pattern so that the level of cross-talk from other signals is minimized.

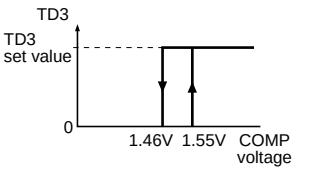
DELAY-3 (TD3)

There is a condition that secondary-side control output OUT-E and OUT-F delay TD3 is 0 s (typical) in order to prevent shorting of the transformer secondary side. The relationship between TD3 and the IC operating state is shown in the following table.

Mode	Definition	Operation of OUT-E, OUT-F	Note
Light load	COMP < 1.65V	TD3 = 0	1
Pulse by pulse OCL	CS ≥ 0.4V	TD3 = 0	2
One shot OCL	CS ≥ 0.6V	Fixed low (operation halted)	

Notes: 1. Light-load detection is performed by means of the error amplifier output voltage. Light-load detection characteristics are as shown in the following diagram.





Light Load Detector Characteristics

2. TD3 of the next OUT-E or OUT-F after the pulse-by-pulse current limiter (PBP OCL) operates is 0 s (typical). When OUT-C and OUT-D are subsequently inverted by the Phase Shift Comparator, not the PBP OCL, TD3 is restored to the value set by means of the DELAY-3 pin.

Application

Note: All voltage, current, time shown in the diagram are typical value.
Sample application circuits are given here. Confirmatory experiments should be carried out when applying these examples to products.

Slope Compensation

In order to improve the unstable operation characteristic of current mode, voltage slopes in a current sense signal can be superimposed. The following is a possible slope compensation method.

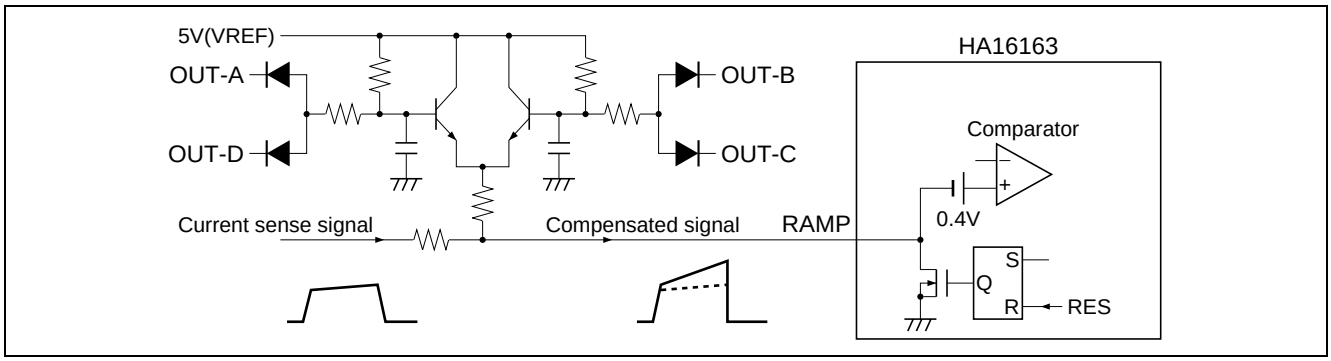
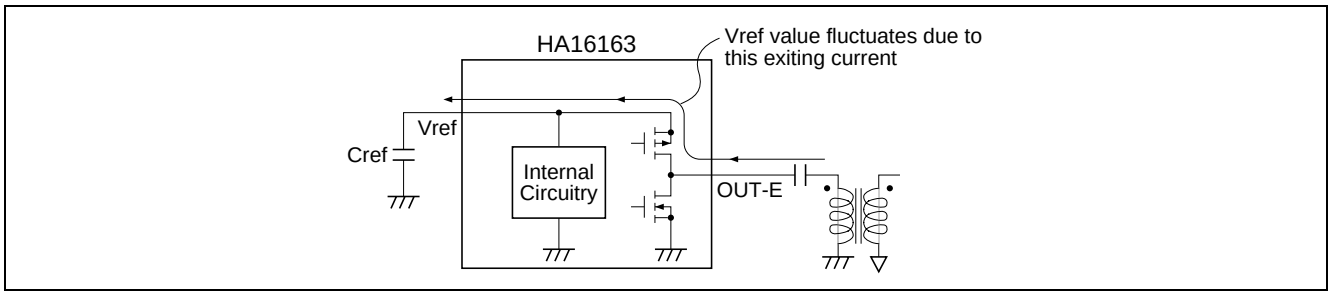


Figure 12

Driving a Pulse Transformer

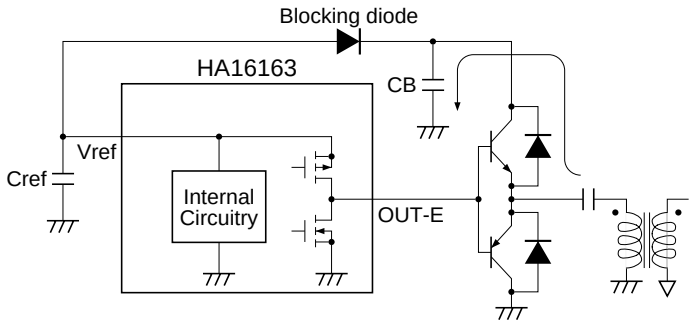
OUT-A through OUT-F of this IC are CMOS outputs that use Vref as their power supply. When directly driving a pulse transformer, the Vref voltage fluctuates according to the exciting current. As Vref fluctuation may make internal circuit operation unstable, direct drive of a pulse transformer should be avoided.

- Case 1 (NG)
  The figure below shows a case where a pulse transformer is driven directly. Vref voltage fluctuation occurs due to the exciting current.



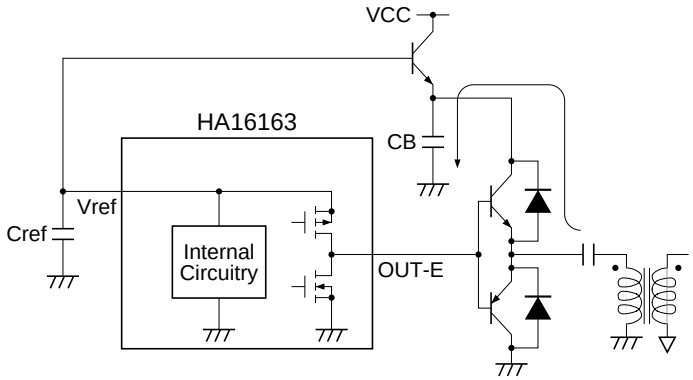
Case 1 (NG)

- Case 2
  The figure below shows an example in which a current amplifier is added by means of transistors. A reverse current due to the exciting current is prevented by a blocking diode, and therefore capacitance CB is charged. In this way, fluctuation of the Cref potential is suppressed and stable operation can be achieved.
  As well as a buffer implemented by means of a transistor, standard logic IC or buffer IC connection is also possible. The buffer circuit power supply method should be implemented in the same way.



Case 2

- Case 3
  The figure below shows an example of a drive power supply method using emitter following. For the same reason as described above, fluctuation of the Cref potential is suppressed and stable operation can be achieved.



Case 3

Supplying Power from an External Power Supply

It is also possible to use an external source as the power supply for the HA16163T as shown in figure 13. The VREF$\overline{\text{GOOD}}$ circuit controls whether the IC is operating or stopped. The threshold voltage of the VREFGOOD circuit is 4.6 V (typ.) on the rising edge and 4.4 V on the falling edge. Since the IC's characteristics vary with the value of the external voltage, this voltage must be provided by a high-precision 5-V source.

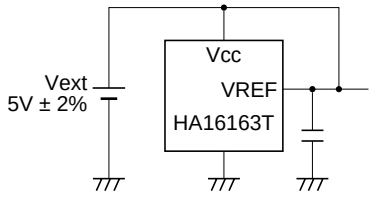
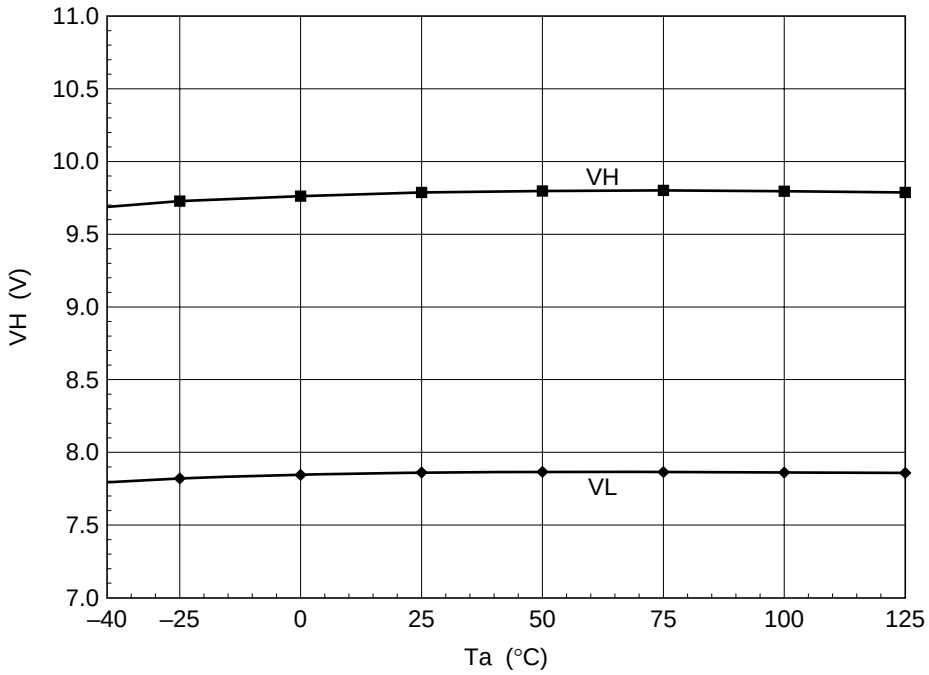


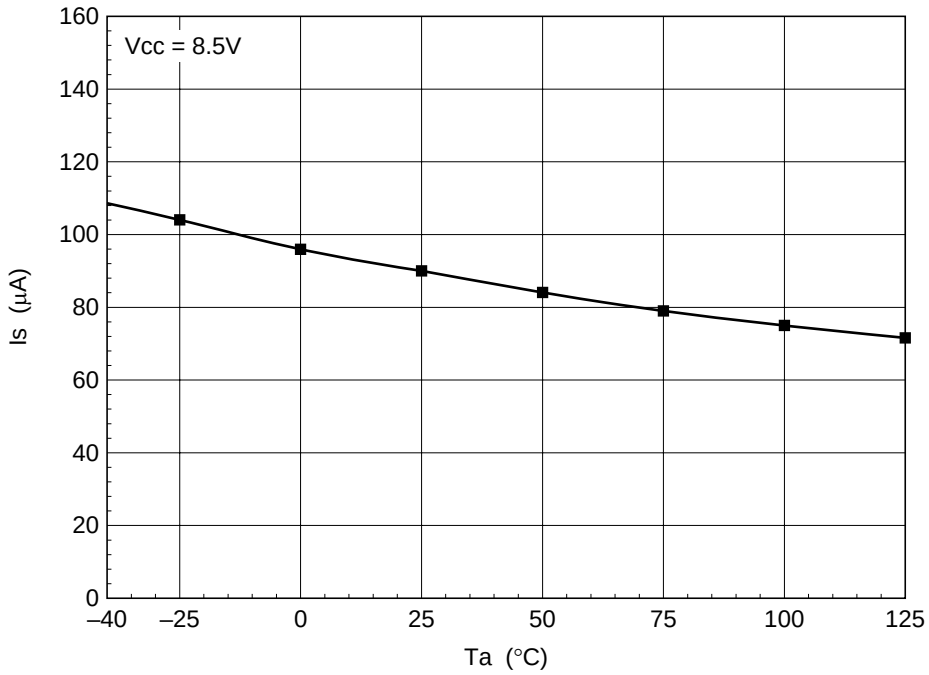
Figure 13

Characteristic Curves

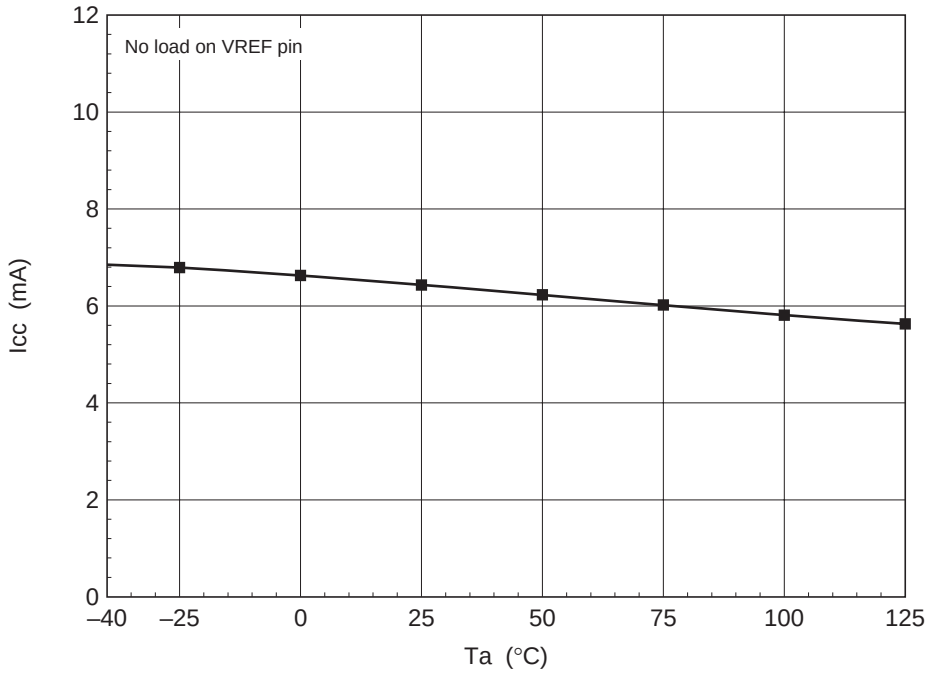
UVL Voltage vs. Ambient Temperature Characteristics



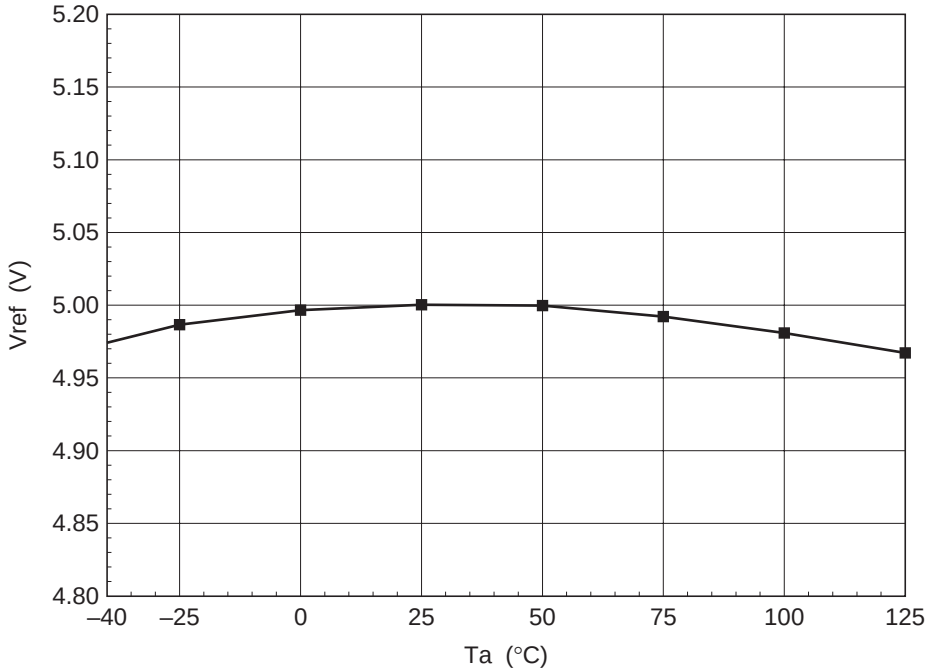
Standby Current vs. Ambient Temperature Characteristics



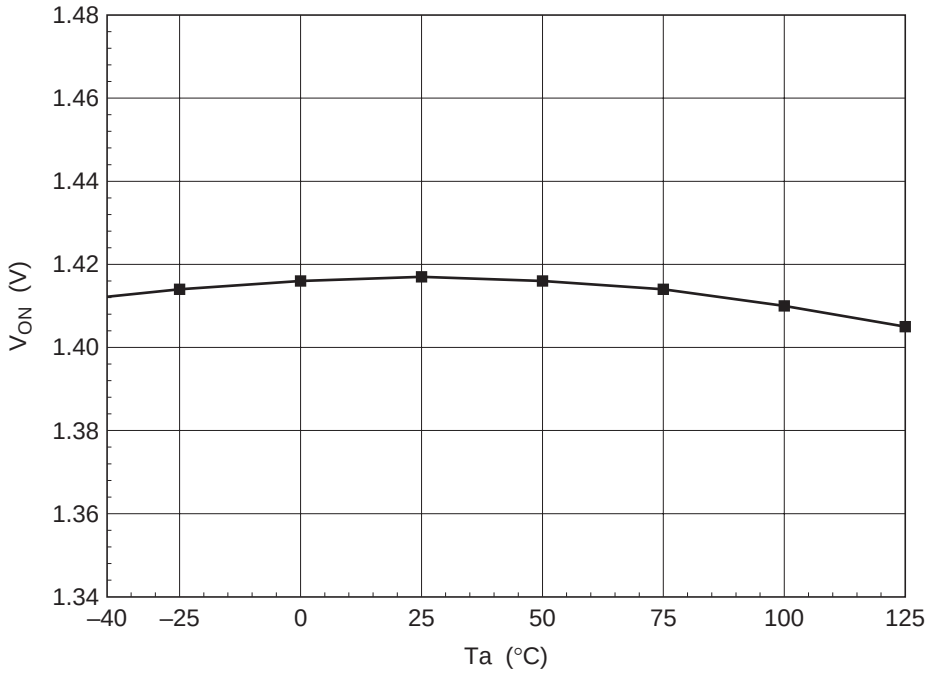
Operating Current vs. Ambient Temperature Characteristics



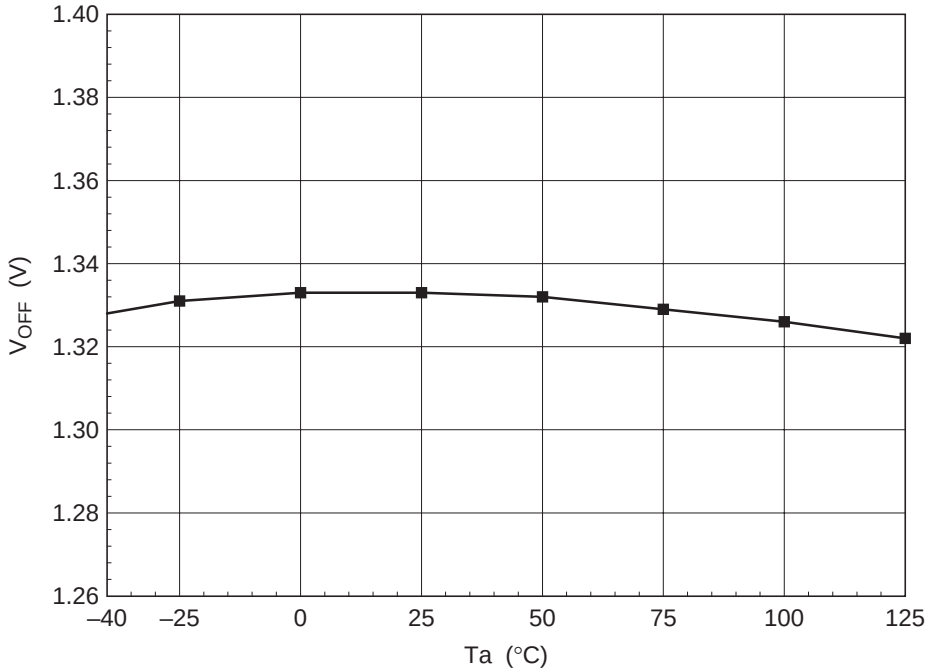
VREF Output Voltage vs. Ambient Temperature Characteristics



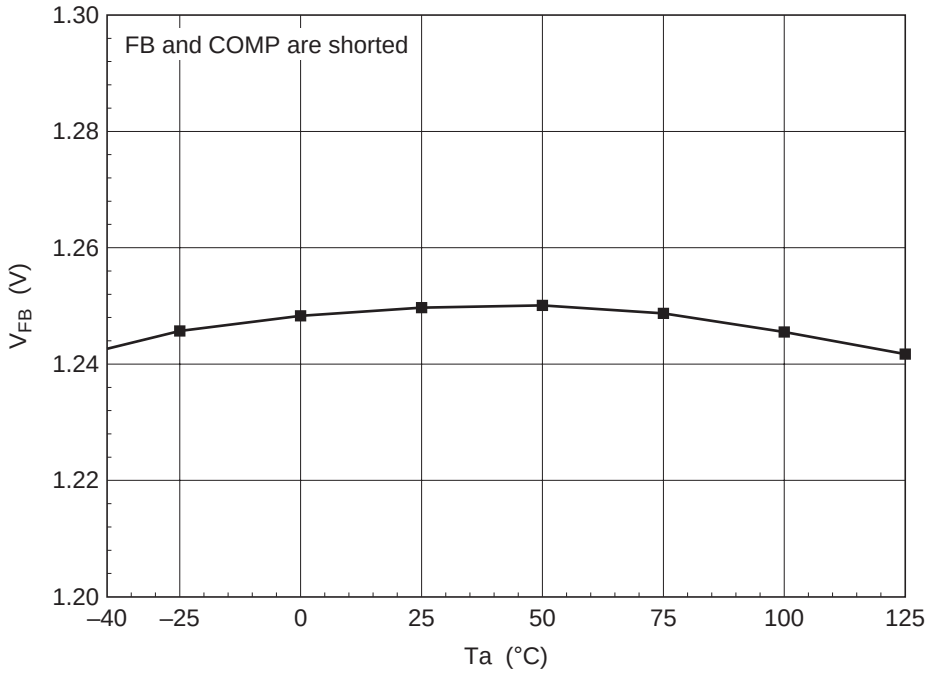
Remote-on Voltage vs. Ambient Temperature Characteristics



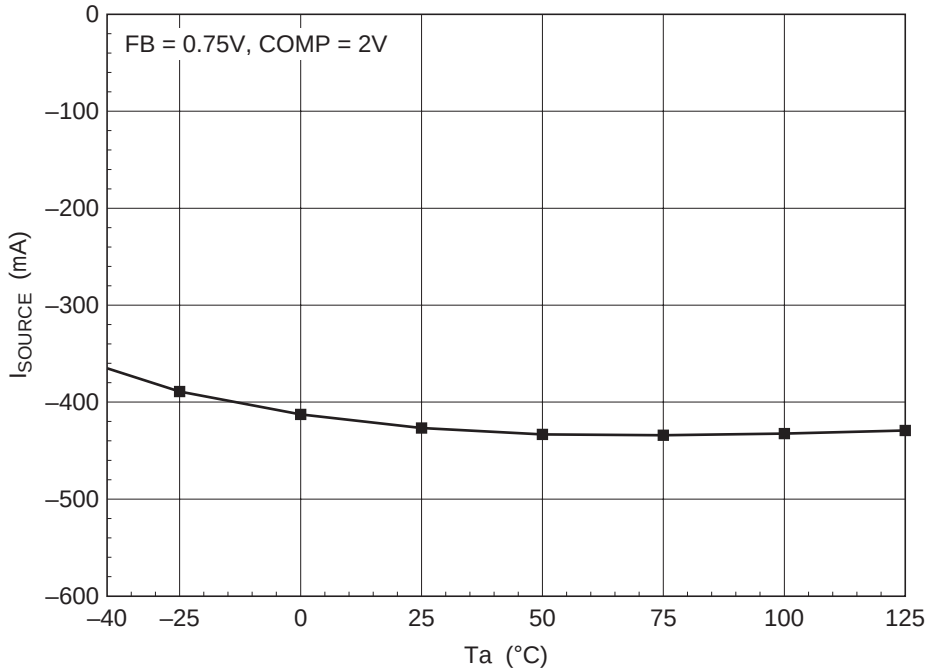
Remote-off Voltage vs. Ambient Temperature Characteristics



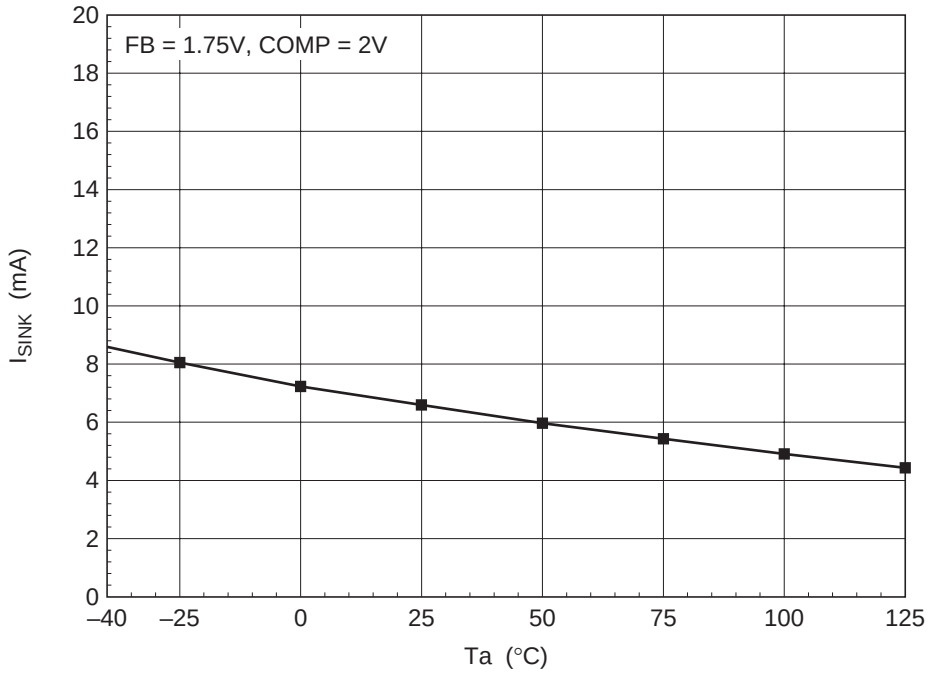
Error Amplifier Feedback Voltage vs. Ambient Temperature Characteristics



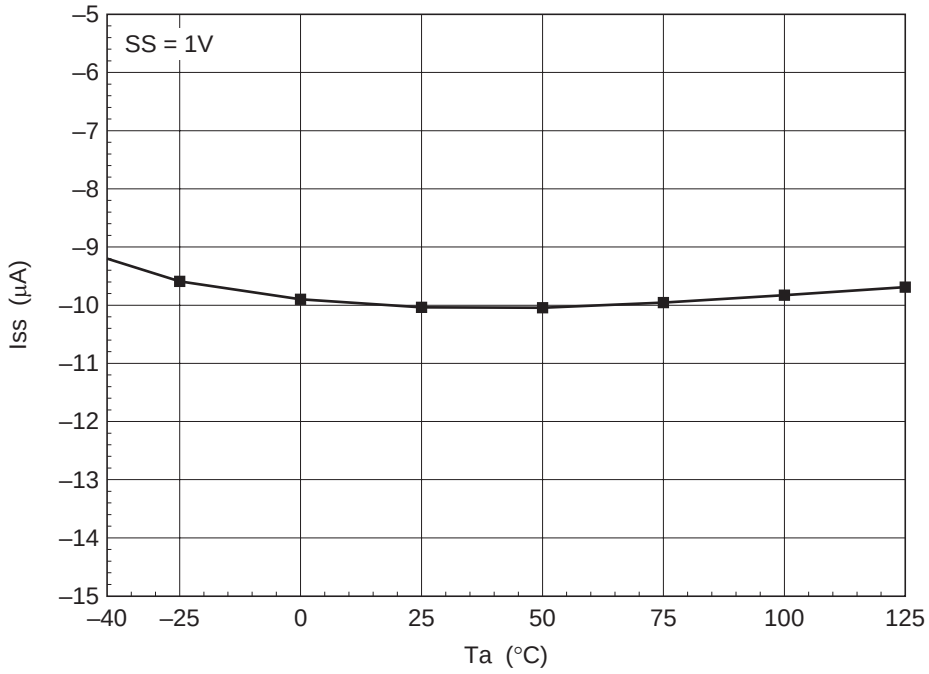
Error Amplifier Source Current vs. Ambient Temperature Characteristics



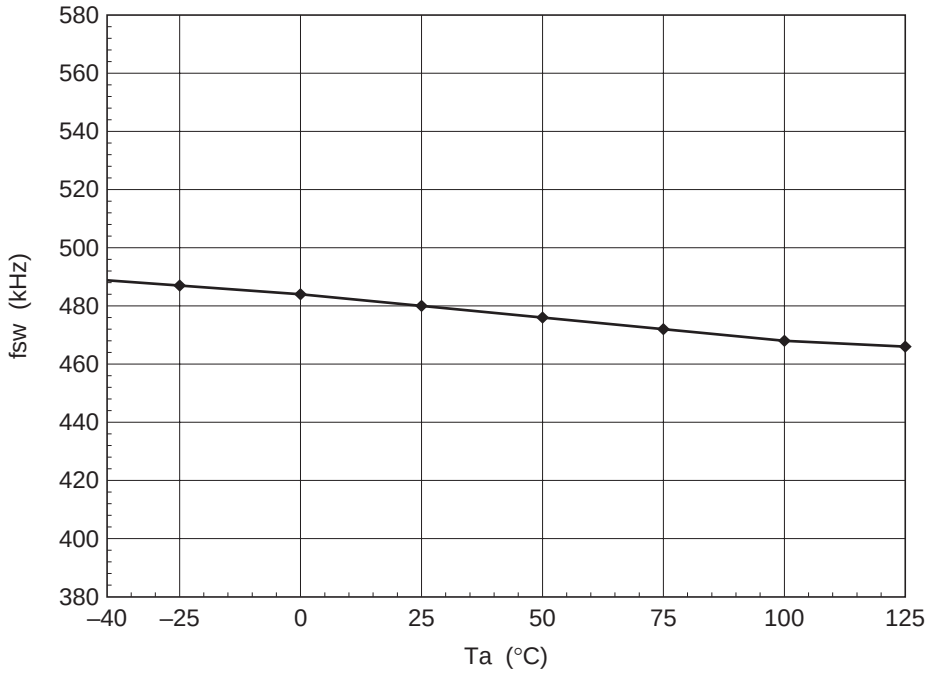
Error Amplifier Sink Current vs. Ambient Temperature Characteristics



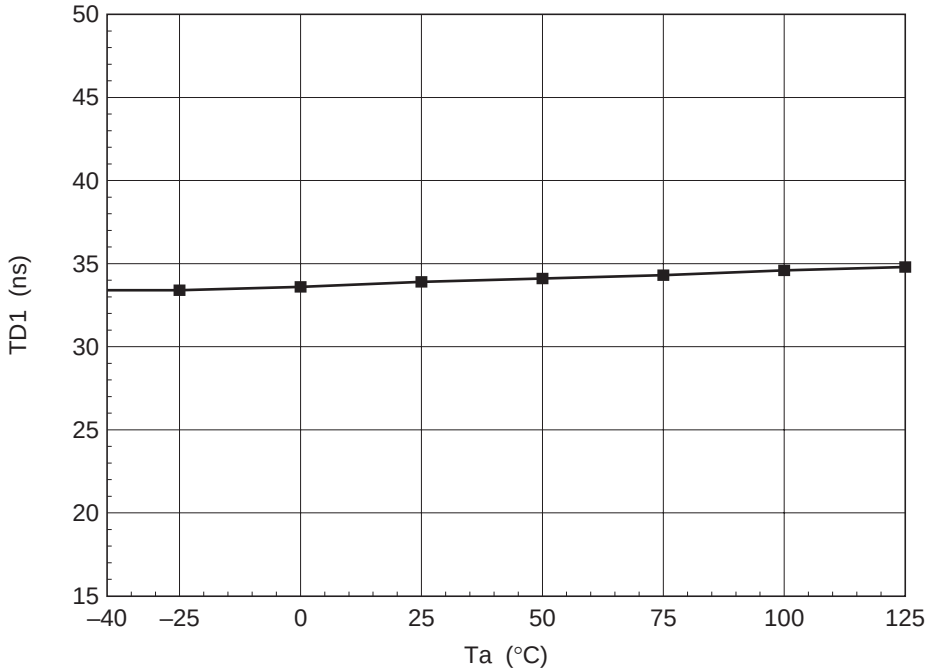
Soft-start Pin Current vs. Ambient Temperature Characteristics



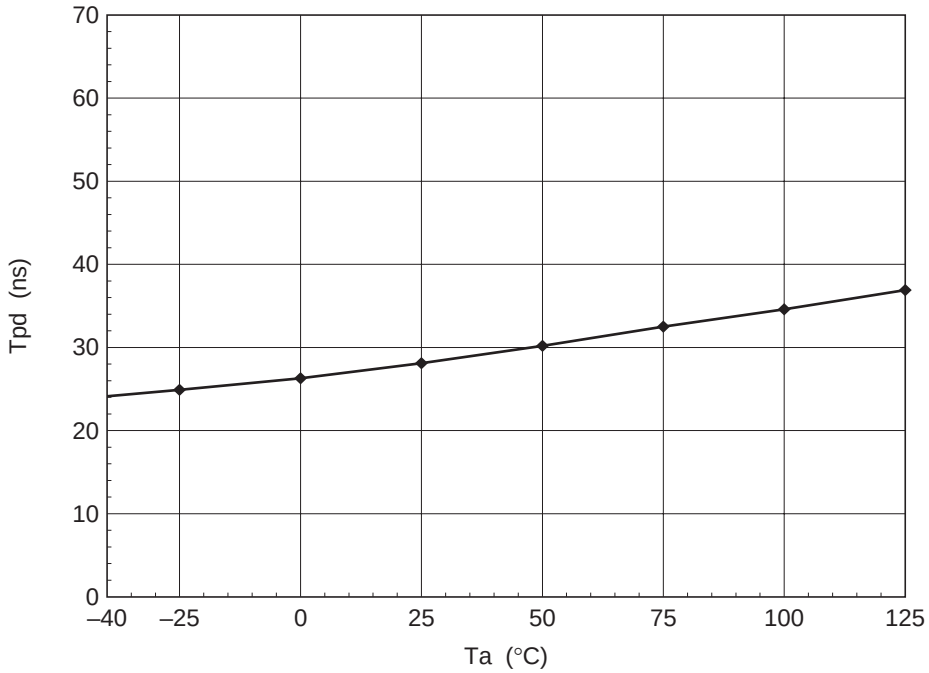
Switching Frequency vs. Ambient Temperature Characteristics



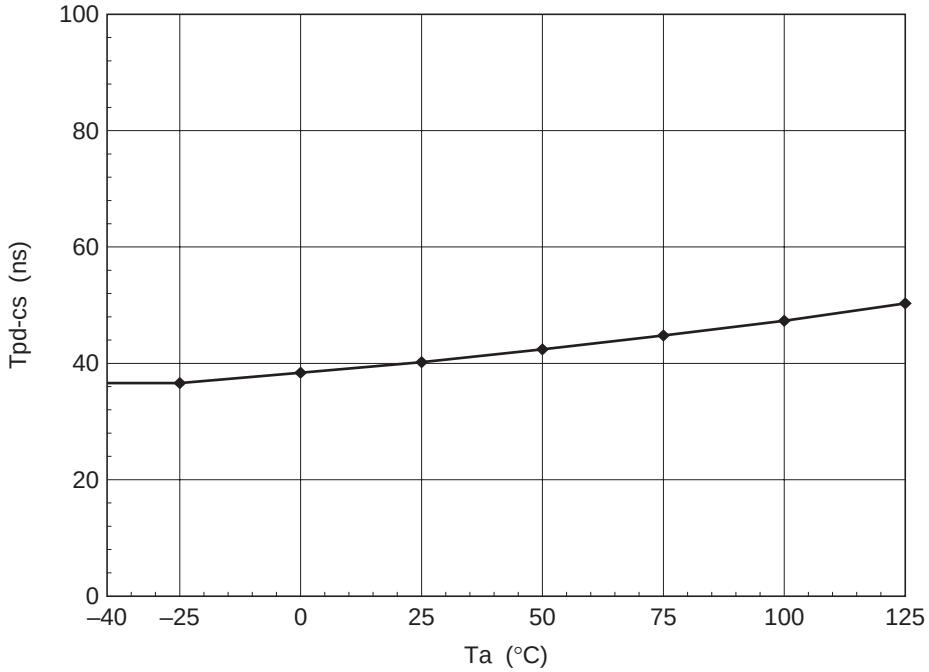
TD1 Delay vs. Ambient Temperature Characteristics



Current Sense Delay Time vs. Ambient Temperature Characteristics



Overcurrent Protection Delay Time vs. Ambient Temperature Characteristics



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
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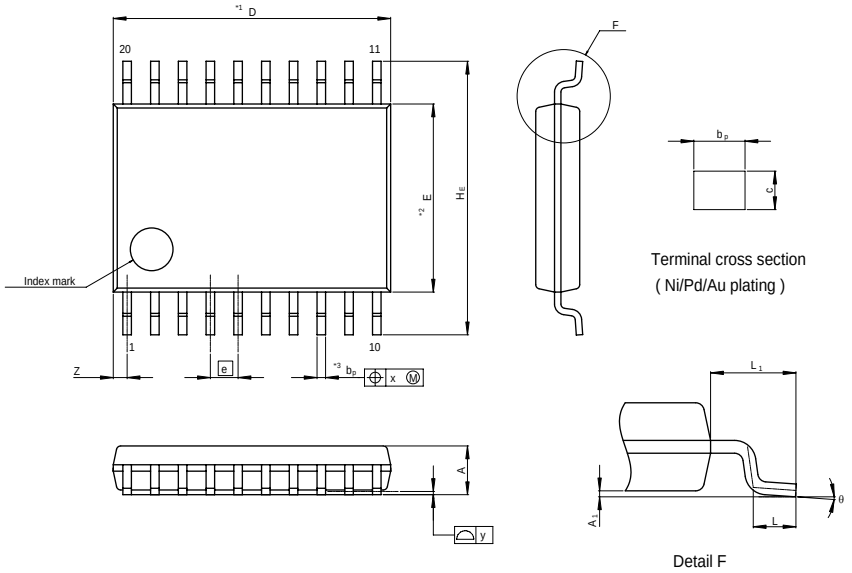

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

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Colophon .7.2