Fast Infrared Transceiver Module (FIR, 4 Mbit/s) for 2.7 V to 5.5 V Operation

Description

The TFDU6102 is a low–power infrared transceiver module compliant to the latest IrDA physical layer standard for fast infrared data communication, supporting IrDA speeds up to 4.0 Mbit/s (FIR), HP-SIR®, Sharp ASK® and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module are a photo PIN diode, an infrared emitter (IRED), and a low–power CMOS control IC to provide a total front–end solution in a single package.

Vishay FIR transceivers are available in different package options, including this BabyFace package (TFDU6102), the standard setting, once smallest FIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O devices which perform the modulation/ demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a V_{CC} bypass capacitor are the only external components required implementing a complete solution. TFDU6102 has a tri–state output and is floating in shut–down mode with a weak pull–up.

Features

- Compliant to the latest IrDA physical layer specification (Up to 4 Mbit/s), HP–SIR®, Sharp ASK® and TV Remote Control
- For 3.0 V and 5.0 V Applications
- Operates from 2.7 V to 5.5 V within specification,
- Low Power Consumption (< 3 mA Supply Current)
- Power Shutdown Mode (< 5 μA Shutdown Current in Full Temperature Range)
- Surface Mount Package
  – Universal ($9.7 \times 4.7 \times 4.0$ mm^3)
- Tri–state–Receiver Output, floating in shutdown with a weak pull–up
- High Efficiency Emitter
- BabyFace (Universal) Package Capable of Surface Mount Soldering to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices
- Built–In EMI Protection – No External Shielding Necessary
- Only One External Component Required
- Backward Pin to Pin Compatible to all Vishay Telefunken SIR and FIR Infrared Transceivers
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements, thus saving costs

Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection

Package Options

TFDU6102
Baby Face (Universal)
weight 0.20 g

Ordering Information

Part Number	Qty / Reel or Tubes	Description
TFDU6102–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU6102–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting

Functional Block Diagram

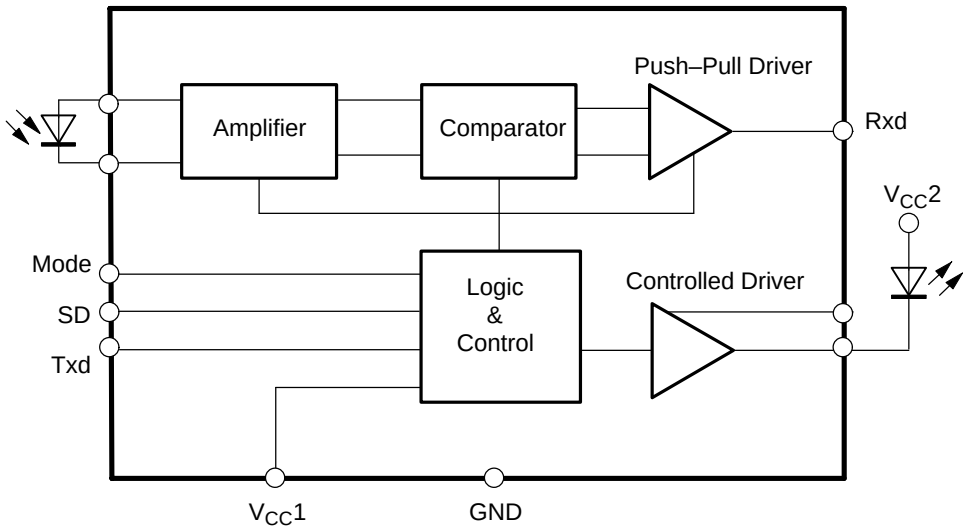

Figure 1. Functional Block Diagram

Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:
SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0
MIR 576 kbit/s to 1152 kbit/s
FIR 4 Mbit/s
VFIR 16 Mbit/s
MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any obsoletes the former version.

Pin Description

Pin Number "U"	Function	Description	I/O	Active
1	V_{CC2}, IRED Anode	IRED anode, to be externally connected to V_{CC2}. For higher voltages than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. See derating curves. This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled V_{CC1} supply		
2	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	Txd	This input is used to transmit serial data when SD is low. An on–chip protection circuit disables the LED driver if the Txd pin is asserted for longer than 80 µs. When used in conjunction with the SD pin, this pin is also used to control receiver mode.	I	HIGH
4	Rxd	Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. **Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode**	O	LOW
5	SD	Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the Txd pin is sampled and used to set receiver low bandwidth (Txd = Low, SIR) or high bandwidth (Txd = High, MIR and FIR) mode. Will be overwritten by the mode pin input, which must float, when dynamic programming is used.	I	HIGH
6	V_{CC1}	Supply Voltage		
7	Mode	HIGH: High speed mode, MIR and FIR; LOW: Low speed mode, SIR only (see chapter “Mode Switching”). Overwrites the dynamically programmed mode. Must float, when dynamic programming is used.	I	
		The mode pin can also be used to indicate the dynamically programmed mode. The maximum load is limited to 50 pF. High indicates FIR/MIR–, low indicates SIR–mode	O	
8	GND	Ground		

“U” Option Baby Face (Universal)

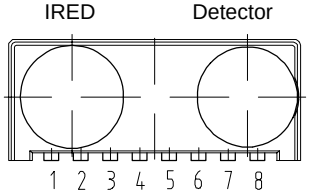

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Figure 2. Pinnings

Absolute Maximum Ratings

Reference point Pin: GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range, Transceiver	0 V <V_{CC2} <6 V	V_{CC1}	– 0.5		6	V
Supply Voltage Range, Transmitter	0 V <V_{CC1} <6 V	V_{CC2}	– 0.5		6.5	V
Input Currents	For all Pins, Except IRED Anode Pin				10	mA
Output Sinking Current					25	mA
Power Dissipation	See Derating Curve	P_D			500	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		+85	°C
Storage Temperature Range		T_{stg}	–25		+85	°C
Soldering Temperature	See Recommended Solder Profile (see Figure 6)				240	°C
Average Output Current		I_{IRED} (DC)			125	mA
Repetitive Pulsed Output Current	<90 µs, t_{on} <20%	I_{IRED} (RP)			600	mA
IRED Anode Voltage		V_{IREDA}	– 0.5		6.5	V
Voltage at all Inputs and Outputs	V_{in} >V_{CC1} is allowed	V_{in}	– 0.5		5.5	V
Load at mode pin when used as mode indicator					50	pF
Virtual Source Size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1	IEC60825–1 or EN60825–1, edition Jan. 2001	I_e			*) (500) **)	mW/sr

*) Due to the internal limitation measures the device is a “class1” device
**) IrDA specifies the max. intensity with 500 mW/sr

Electrical Characteristics

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supply Voltage		V_{CC}	2.7		5.5	V
Dynamic Supply Current	Receive mode only. In transmit mode, add additional 85 mA (typ) for IRED current. Add Rxd output current depending on Rxd load.					
	SD = Low, E_e = 0 klx	I_{CC}		2	3	mA
	SD = Low, E_e = 1 klx *)	I_{CC}		2	3	mA
Standby Supply Current	SD = High, Mode = Floating, T = 25°C, E_e = 0 klx T = 25°C, E_e = 1 klx *)	I_{SD}			 2.0 2.5	 µA µA
	SD = High, T = 85°C, Mode = Floating, Not Ambient Light Sensitive	I_{SD}			5	µA
Operating Temperature Range		T_A	–25		+85	°C
Output Voltage Low	I_{OL} = 1 mA C_{Load} = 15 pF	V_{OL}			0.4	V
Output Voltage High	I_{OH} = 500 µA I_{OH} = 250 µA C_{Load} = 15 pF	V_{OH}	0.8xV_{CC} 0.9xV_{CC}			V V
Output Rxd Current limitation High State Low State	 Short to Ground Short to V_{CC}1				 20 20	 mA mA
Rxd to V_{CC}1 Impedance		R_{Rxd}	400	500	600	kΩ
Input Voltage Low (Txd, SD, Mode)		V_{IL}	– 0.5		0.5	V
Input Voltage High (Txd, SD, Mode)	CMOS level **)	V_{IH}	V_{CC} –0.5		V_{CC} +0.5	V
	TTL level, V_{CC}1 = 4.5	V_{IH}	2.4			V
Input Leakage Current (Txd, SD, Mode)		I_L	–10		+10	µA
Input Leakage Current, Mode		I_{ICH}	–2		+2	µA
Input Capacitance, Txd, SD, Mode		C_I			5	pF

*) Standard Illuminant A
**) The typical threshold level is between 0.5 x $V_{CC/2}$ (V_{CC} = 3 V) and 0.4 x V_{CC} (V_{CC} = 5.5 V) .
It is recommended to use the specified min/ max values to avoid increased operating current.

Optoelectronic Characteristics

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

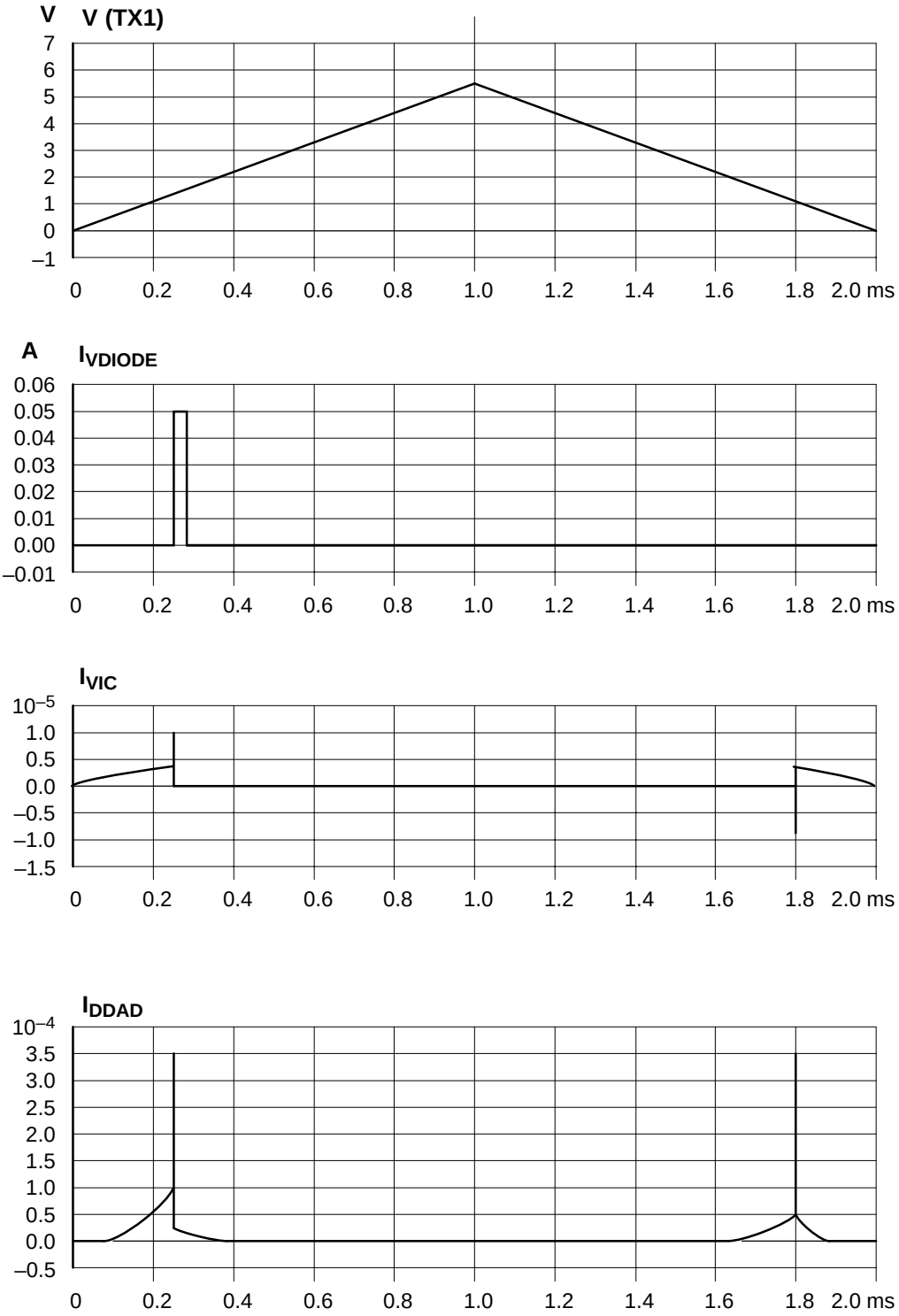
Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Minimum Detection Threshold Irradiance, SIR Mode	9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		25 (2.5)	40 (4.0)	mW/m^2 (μW/cm^2)
Minimum Detection Threshold Irradiance, MIR Mode	1.152 Mbit/s λ = 850 nm to 900 nm	E_e		65 (6.5)		mW/m^2 (μW/cm^2)
Minimum Detection Threshold Irradiance, FIR Mode	4.0 Mbit/s λ = 850 nm to 900 nm	E_e		85 (8.5)	100 (10)	mW/m^2 (μW/cm^2)
Maximum Detection Threshold Irradiance	λ = 850 nm to 900 nm	E_e		5 (500)		kW/m^2 (mW/cm^2)
Logic LOW Receiver Input Irradiance		E_e	4 (0.4)			mW/m^2 (μW/cm^2)
Rise Time of Output Signal	10% to 90%, C_L = 15 pF	$t_{r\ (Rxd)}$	10		40	ns
Fall Time of Output Signal	90% to 10%, C_L = 15 pF	$t_{f\ (Rxd)}$	10		40	ns
Rxd Pulse Width of Output Signal, 50% SIR Mode	Input pulse length 1.4 μs < P_{Wopt} < 25 μs	t_{PW}	1.5	1.8	2.1	μs
Rxd Pulse Width of Output Signal, 50% MIR Mode	Input pulse length P_{Wopt} = 217 ns, 1.152 Mbit/s	t_{PW}	110	250	270	ns
Rxd Pulse Width of Output Signal, 50% FIR Mode	Input pulse length P_{Wopt} = 125 ns, 4.0 Mbit/s	t_{PW}	100		140	ns
	Input pulse length P_{Wopt} = 250 ns, 4.0 Mbit/s	t_{PW}	225		275	ns
Stochastic Jitter, Leading Edge	Input Irradiance = 100 mW/m^2, 4.0 Mbit/s 1.152 Mbit/s 576 kbit/s ≤ 115.2 kbit/s				 20 40 80 350	 ns ns ns ns
Receiver start up time	after completion of shutdown programming sequence Power on delay				500	μs
Latency		t_L		170	300	μs

Note: All timing data measured with 4 Mbit/s are measured using the IrDA® FIR transmission header. The data given here are valid 5 μs after starting the preamble.

Optoelectronic Characteristics (continued)

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transmitter						
IRED Operating Current, Switched Current Limiter	See derating curve. For 3.3 V operation no external resistor needed. For 5 V application that might be necessary	I_D	500	550	600	mA
Output Leakage IRED Current		I_{IRED}	–1		1	µA
Output Radiant Intensity (see Figure 3) recommended appl. circuit	α = 0°, 15° Txd = High, SD = Low	I_e	120	170	350	mW/sr
Output Radiant Intensity	V_{CC}1 = 5.0 V, α = 0°, 15° Txd = Low or SD = High, (Receiver is inactive as long as SD = High)	I_e			0.04	mW/sr
Output Radiant Intensity, Angle of Half Intensity		α		±24		°
Peak – Emission Wavelength		λ_P	850		900	nm
Spectral Bandwidth		Δ_λ		40		nm
Optical Rise Time, Optical Fall Time		t_{ropt}, t_{fopt}	10		40	ns
Optical Output Pulse Duration	Input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	207	217	227	ns
	Input pulse width 125 ns, 4 Mbit/s	t_{opt}	117	125	133	ns
	Input pulse width 250 ns, 4 Mbit/s	t_{opt}	242	250	258	ns
	Input pulse width t < 80 µs Input pulse width t = 80 µs	t_{opt}	 20	t	 85	µs
Optical Overshoot					25	%



Input Load

The waveform “IDDadd” shows the additional operating current of one input buffer (in this case TXD) vs. the logic input voltage V (TXI) for the digital supply voltage V_{dd} = 3 V under typical working conditions. The current “IVIC” is the typical input current vs. the input voltage

Recommended Circuit Diagram

Operated at a clean low impedance power supply the TFDU6102 needs no additional external components. However, depending on the entire system design and board layout, additional components may be required (see figure 3).

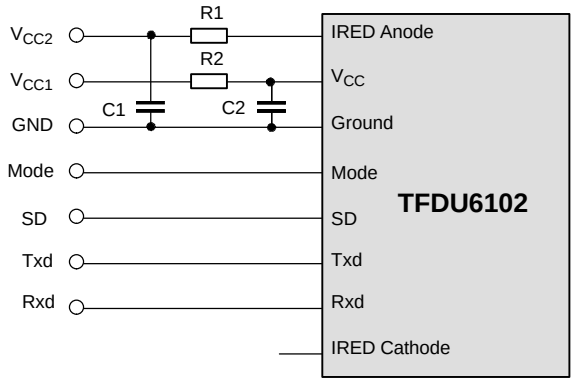


Figure 3. Recommended Application Circuit

The capacitor C1 is buffering the supply voltages and eliminates the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for higher operating voltages and elevated temperatures, see derating curve in figure 7, to avoid too high internal power dissipation.

Vishay Telefunken transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (Txd, SD/ Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit.

The capicitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage.
R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CCx} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as near as possible to the transceiver power supply pins. An Tantalum capacitor should be used for C1 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at $V_{CC2.}$ Often some power supplies are not apply to follow the fast current is rise time. In that case another 4.7 µF (type, see table under C1) at V_{CC2} will be helpful.

Keep in mind that basic RF–design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. “The Art of Electronics” Paul Horowitz, Wienfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

Table 1. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1	4.7 µF, 16 V	293D 475X9 016B
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	**5 V supply voltage:** 2 Ω (–5.6 Ω s. text) 0.25 W (recommend using two 1 Ω, 0.125 W resistors in series) **3.3 V supply voltage:** no resistor necessary, the internal controller is able to control the current.	e.g. 2 x CRCW–1206–1R0–F–RT1
R2	47 Ω , 0.125 W	CRCW–1206–47R0–F–RT1

I/O and Software

In the description, already different I/Os are mentioned. Differnt combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

Mode Switching

The TFDU6102 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the Txd and SD inputs as described below or selected by setting the Mode Pin. The Mode Pin can be used to statically set the mode (Mode Pin: LOW: SIR, HIGH: 0.576 Mbit/s to 4.0 Mbit/s). If not used or in standby mode, the mode input should float or should not be loaded with more than 50 pF. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

Setting to the High Bandwidth Mode (0.576 Mbit/s to 4.0 Mbit/s)

1. Set SD input to logic “HIGH”.
2. Set Txd input to logic “HIGH”. Wait $t_s \geq 200$ ns.
3. Set SD to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd can be set to logic “LOW”. The hold time of Txd is limited by the maximum allowed pulse length.

Txd is now enabled as normal Txd input for the high bandwidth mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD input to logic “HIGH”.
2. Set Txd input to logic “LOW”. Wait $t_s \geq 200$ ns.
3. Set SD to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.

Txd is now enabled as normal Txd input for the lower bandwidth mode.

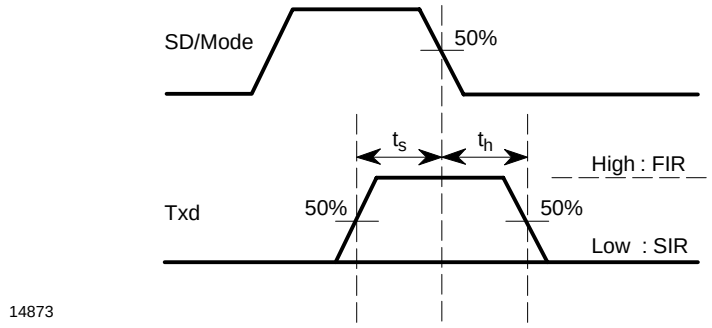


Figure 4. Mode Switching Timing Diagram

Table 2. Truth table

Inputs			Outputs	
SD	Txd	Optical input Irradiance mW/ m^2	Rxd	Transmitter
high	x	x	weakly pulled (500 kΩ to V_{CC1})	0
low	high	x	high	I_e
low	high > 80 µs	x	high	0
low	low	< 4	high	0
low	low	> Min. Detection Threshold Irradiance < Max. Detection Threshold Irradiance	low (active)	0
low	low	> Max. Detection Threshold Irradiance	x	0

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads. For more configurations see inside the device drawing.

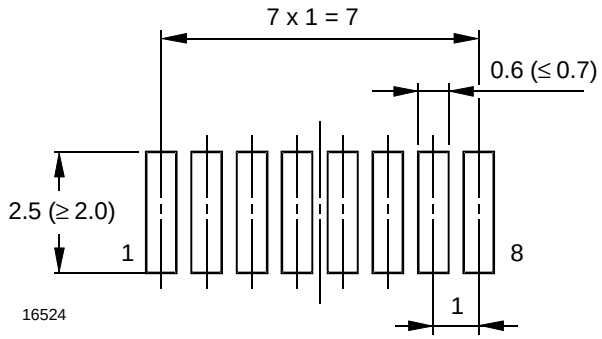


Figure 5. TFDU6102 BabyFace Series (Universal)
Note: Leads of the device should be at least 0.3 mm within the ends of the pads.

Recommended Solder Profile

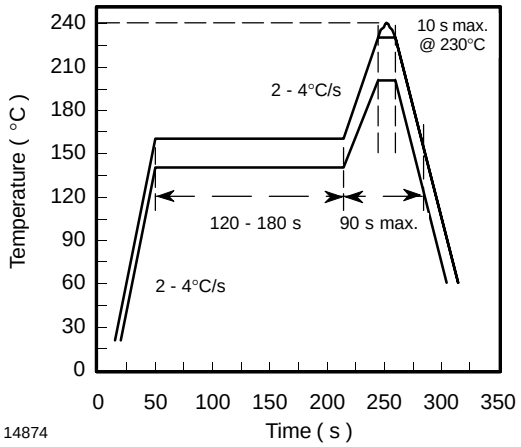


Figure 6. Recommended Solder Profile

Current Derating Diagram

Figure 7 shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to Ground for supply voltages above 4 V. In that case the device can be operated up to 85°C, too.

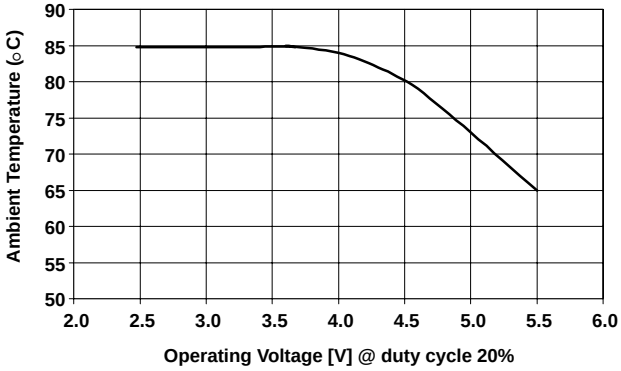
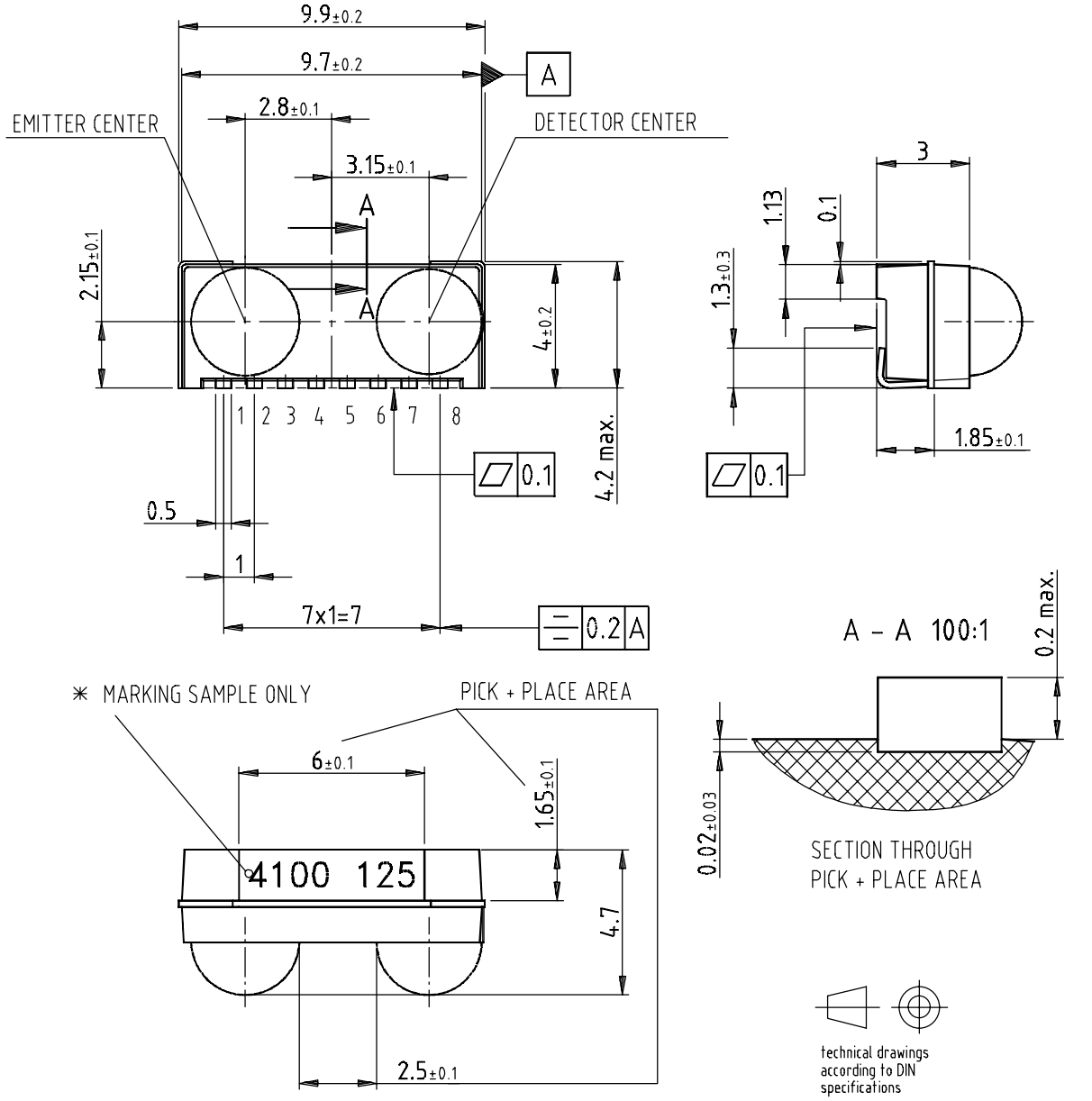


Figure 7. Current Derating Diagram

TFDU6102 – Baby Face (Universal) Package (Mechanical Dimensions)



Revision History:

A1.0, 17/07/2002 :New edition for FIR device with integrated current limiter. TFDU6102

A1.1, 02/09/2002 :TFDU6101, TFDU6102F canceled

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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