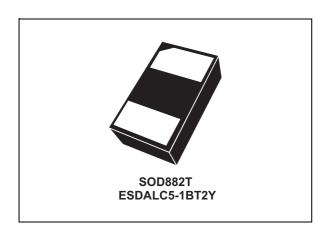
life.augmented

ESDALC5-1BT2Y

Automotive single-line low capacitance Transil™, transient surge voltage suppressor (TVS) for ESD protection

Datasheet - production data



Features

- · Single-line bidirectional protection
- Breakdown voltage = 5.8 V min.
- Low capacitance = 26 pF at 0 V
- · Lead-free packages
- ECOPACK®2 compliant component
- AEC-Q101 qualified

Benefits

- · Low capacitance for optimized data integrity
- Low leakage current < 60 nA
- Low PCB space consumption: 0.6 mm²
- · High reliability offered by monolithic integration

Complies with the following standards:

- IEC 61000-4-2 (exceeds level 4)
 - 30 kV (air discharge)
 - 30kV (contact discharge)
- ISO10605: C = 330 pF, R = 330 Ω
 - 30kV (air discharge)
 - 30kV (contact discharge)
- ISO 7637-3:
 - Pulse 3a: $V_S = -150 \text{ V}$
 - Pulse 3b: V_S = +100 V

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

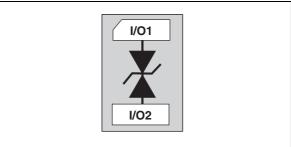
- · Automotive applications
- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC5-1BT2Y is bidirectional single-line TVS diode designed to protect data lines or other I/O ports against ESD transients.

This device is ideal for applications where both printed circuit board space and power absorption capability are required.

Figure 1. Functional diagram



TM: Transil is a trademark of STMicroelectronics

Characteristics ESDALC5-1BT2Y

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25 \text{ °C}$)

Symbol		Value	Unit		
		IEC 61000-4-2 contact dis	30		
V _{PP} Peak pulse volt		30			
	Peak pulse voltage	ISO10605 contact dischar	30	kV	
		ISO10605 air discharge	30		
		MIL STD 883G - Method 3	25		
P _{PP}	Peak pulse power dissipation (8/20 μ s) T_j initial = T_{amb}			150	W
I _{PP}	Peak pulse current (8/20 µs)			9	Α
T _{OP}	Operating junction te	- 50 to + 125	°C		
T _{stg}	Storage temperature range			- 65 to + 125	°C
T_L	Maximum lead temperature for soldering during 10 s			260	°C

Figure 2. Electrical characteristics (definitions)

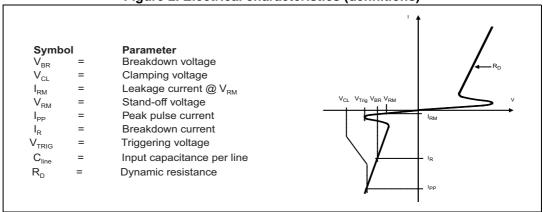


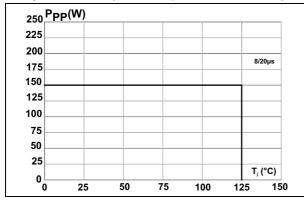
Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Тур.	Max.	Unit
From I/O1 to I/O2, I _R = 1 mA		11	13	17	V
V _{BR}	From I/O2 to I/O1, I _R = 1 mA	5.8	8	11	V
I _{RM}	V _{RM} = 5 V			60	nA
R _d	Dynamic resistance, pulse width 100 ns From I/O1 to I/O2 From I/O2 to I/O1		0.25 0.23		Ω
V _{CL}	8 kV contact discharge after 30 ns IEC 61000 4-2 From I/O1 to I/O2 From I/O2 to I/O1		17.5 12.5		V
C _{line}	F = 1 MHz, V _R = 0 V		26	30	pF

ESDALC5-1BT2Y Characteristics

Figure 3. Peak pulse power versus initial junction temperature (maximum values)

Figure 4. Junction capacitance versus reverse voltage applied (typical values)



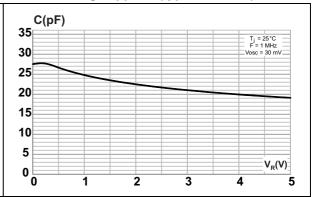
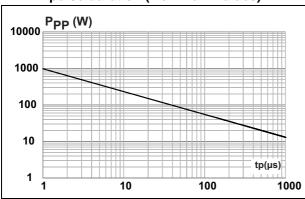


Figure 5. Peak pulse power versus exponential pulse duration (maximum values)

Figure 6. Clamping voltage versus peak pulse current (typical values)



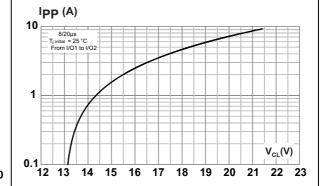
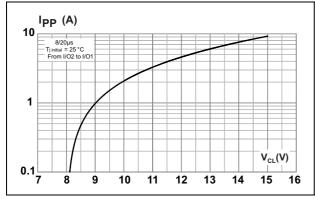
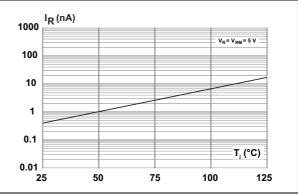


Figure 7. Clamping voltage versus peak pulse current (typical values)

Figure 8. Leakage current versus junction temperature (typical values)

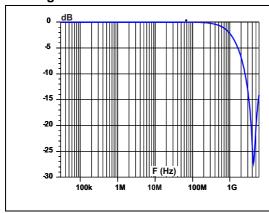




Characteristics ESDALC5-1BT2Y

Figure 9. S21 attenuation measurement

Figure 10. TLP measurements



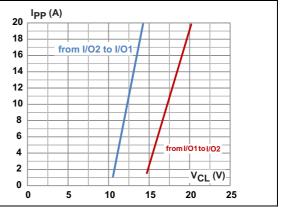
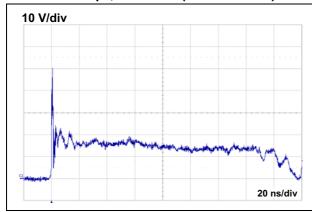


Figure 11. ESD response to ISO 10605, C = 150 pF, $R = 330 \Omega (+8 \text{ kV contact})$

Figure 12. ESD response to ISO 10605, C = 150 pF, $R = 330 \Omega$ (-8 kV contact)



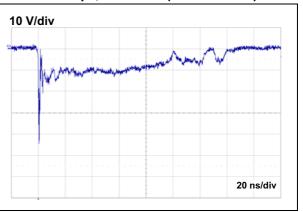
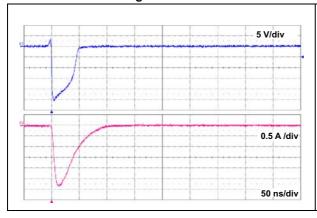
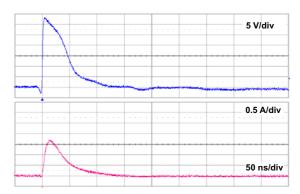


Figure 13. Response to ISO 7637-3 (pulse 3a) $U_S = -150 \text{ V}$

Figure 14. Response to ISO 7637-3 (pulse 3b) $U_S = +100 \text{ V}$





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2 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

PIN#1ID

E

E

Figure 15. SOD882T dimension definitions

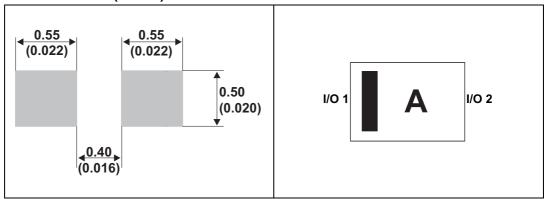
Package information ESDALC5-1BT2Y

Table 3. SOD882T dimension values

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	0.30		0.40	0.012		0.016	
A1	0.00		0.05	0.000		0.002	
b1	0.45	0.50	0.55	0.018	0.020	0.022	
b2	0.45	0.50	0.55	0.018	0.020	0.022	
D	0.55	0.60	0.65	0.022	0.024	0.026	
Е	0.95	1.00	1.05	0.037	0.039	0.041	
е	0.60	0.65	0.70	0.024	0.026	0.028	
L1	0.20	0.25	0.30	0.008	0.010	0.012	
L2	0.20	0.25	0.30	0.008	0.010	0.012	

Figure 16. SOD882T footprint in mm (inches)

Figure 17. SOD882T marking



Note:

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

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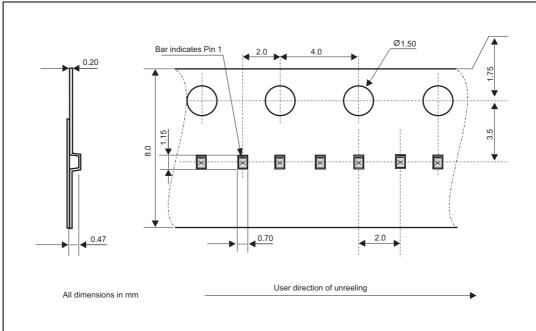


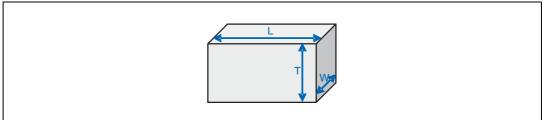
Figure 18. SOD882T tape and reel specifications

3 Recommendation on PCB assembly

3.1 Stencil opening design

- 1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 19. Stencil opening dimensions



b) General design rule

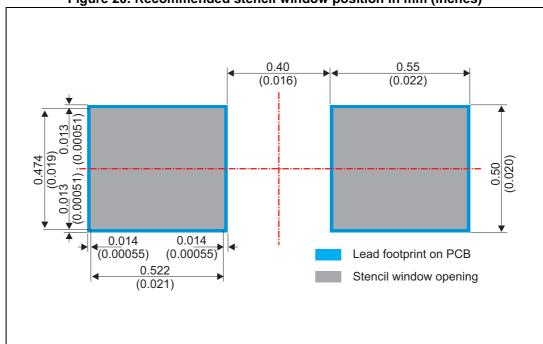
Stencil thickness (T) = 75 \sim 125 μ m

Aspect Ratio =
$$\frac{W}{T} \ge 1.5$$

Aspect Area =
$$\frac{L \times W}{2T(L + W)} \ge 0.66$$

- 2. Reference design
 - a) Stencil opening thickness: 100 µm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 20. Recommended stencil window position in mm (inches)



3.2 Solder paste

- Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Solder paste with fine particles: powder particle size is 20-45 μm.

3.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- 3. Standard tolerance of ± 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

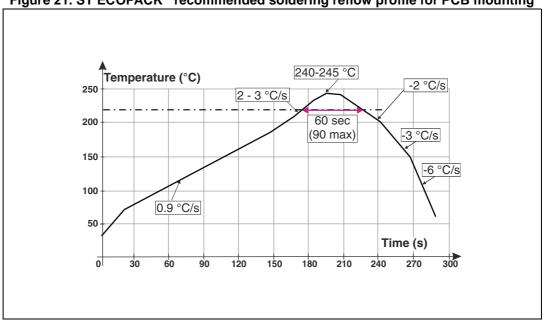
3.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



3.5 Reflow profile

Figure 21. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 22. Ordering information scheme

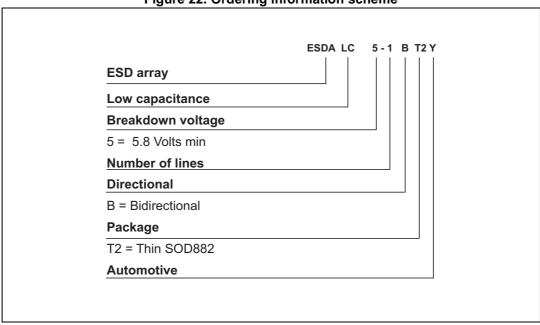


Table 4. Ordering information

Order code	Marking ⁽¹⁾	Package	Weight	Base qty	Delivery mode
ESDALC5-1BT2Y	Α	SOD882T	0.80 mg	12000	Tape and reel

^{1.} The marking can be rotated by multiples of 90° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Feb-2014	1	Initial release.

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