SPP7001K
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP7001K is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

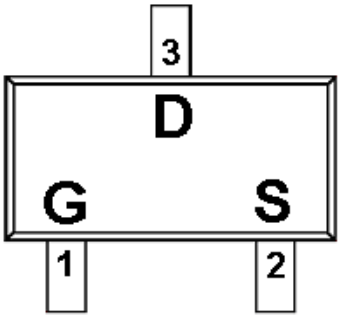
APPLICATIONS

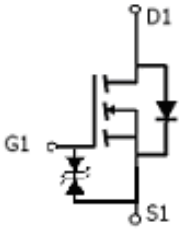
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

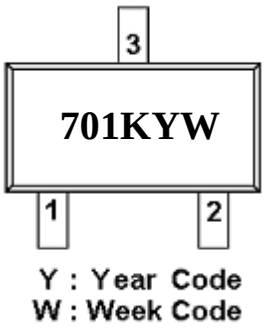
- -60V/-0.5A,$R_{DS(ON)}$= 6Ω@V_{GS}=- 10V
- -60V/-0.25A,$R_{DS(ON)}$= 10Ω@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PIN CONFIGURATION(SOT-23)





PART MARKING



SPP7001K
P-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP7001KS23RGB	SOT-23	701KYW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP7001KS23RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-0.5	A
	T_A=70℃		-0.3	
Pulsed Drain Current		I_{DM}	-1	A
Continuous Source Current(Diode Conduction)		I_S	-0.5	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	375	℃/W

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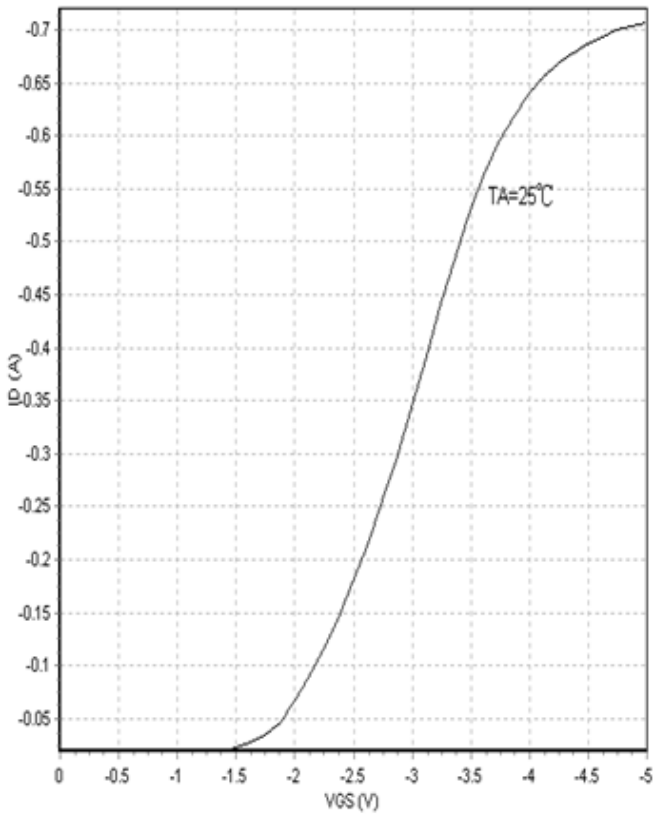
ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

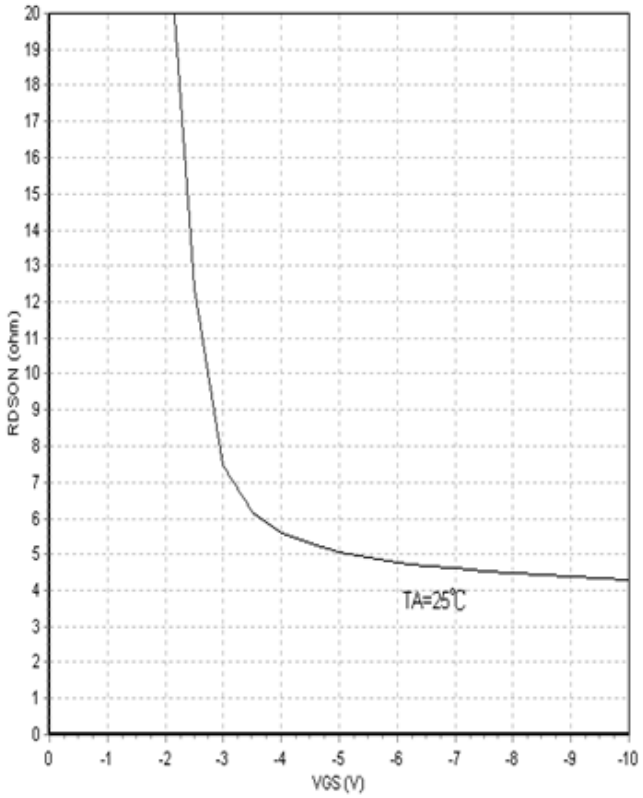
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1		-3	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V,V_{GS}=0V			-1	uA
		V_{DS}=-60V,V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-10V	-1			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=- 10V,I_D=-0.5A			6	Ω
		V_{GS}=-4.5V,I_D=-0.25A			10	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-0.5A		1		S
Diode Forward Voltage	V_{SD}	I_S=-0.2A,V_{GS}=0V			-1.5	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-30V, V_{GS}=-15V I_D= -0.5A		2		nC
Gate-Source Charge	Q_{gs}			0.53		
Gate-Drain Charge	Q_{gd}			0.72		
Input Capacitance	C_{iss}	V_{DS}=-25V,V_{GS}=0V f=1MHz		25		pF
Output Capacitance	C_{oss}			13		
Reverse Transfer Capacitance	C_{rss}			7.3		
Turn-On Time	$t_{d(on)}$	V_{DD}=-25V, I_D=-200mA, V_{GEN}=-10V		20		nS
Turn-Off Time	$t_{d(off)}$			35		

TYPICAL CHARACTERISTICS

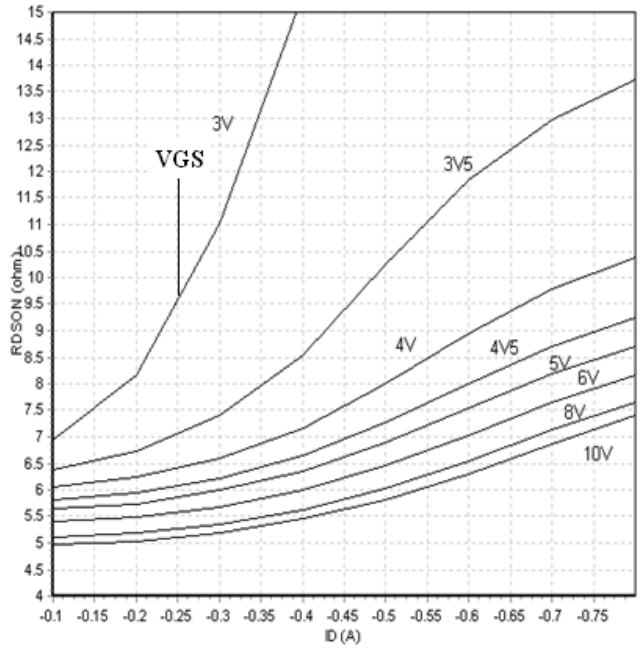
Drain-Current vs. Gate-Source Voltage



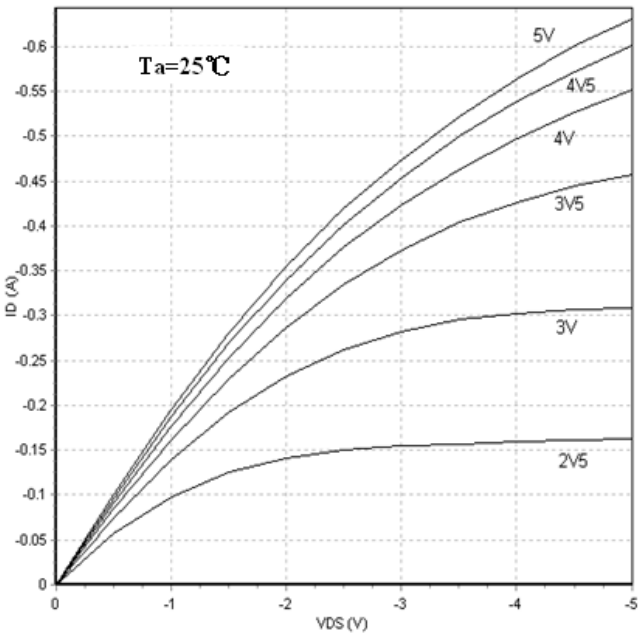
On-Resistance vs. Gate-Source Voilage



On-Resistance vs. Drain-Current

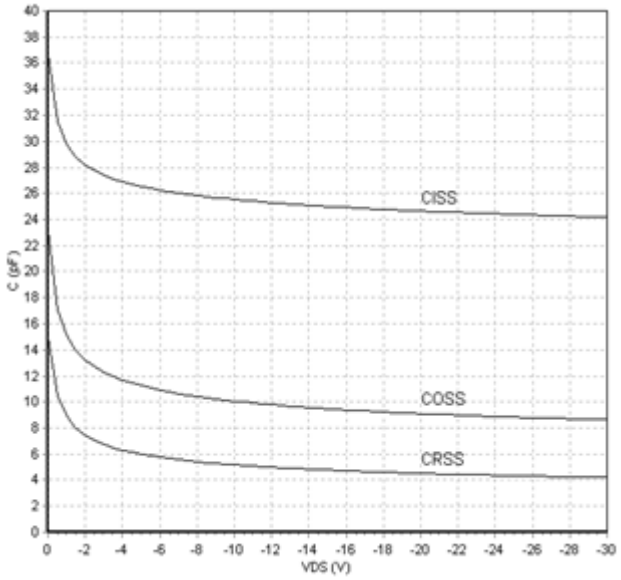


Drain-Source Current vs. Drain-Source Voltage

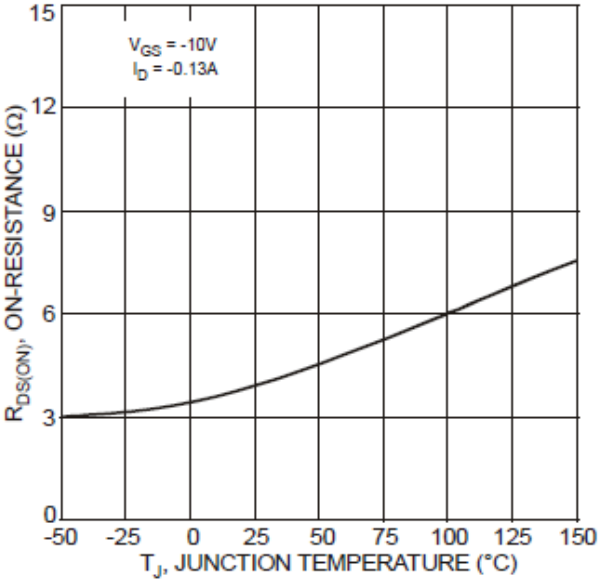


TYPICAL CHARACTERISTICS

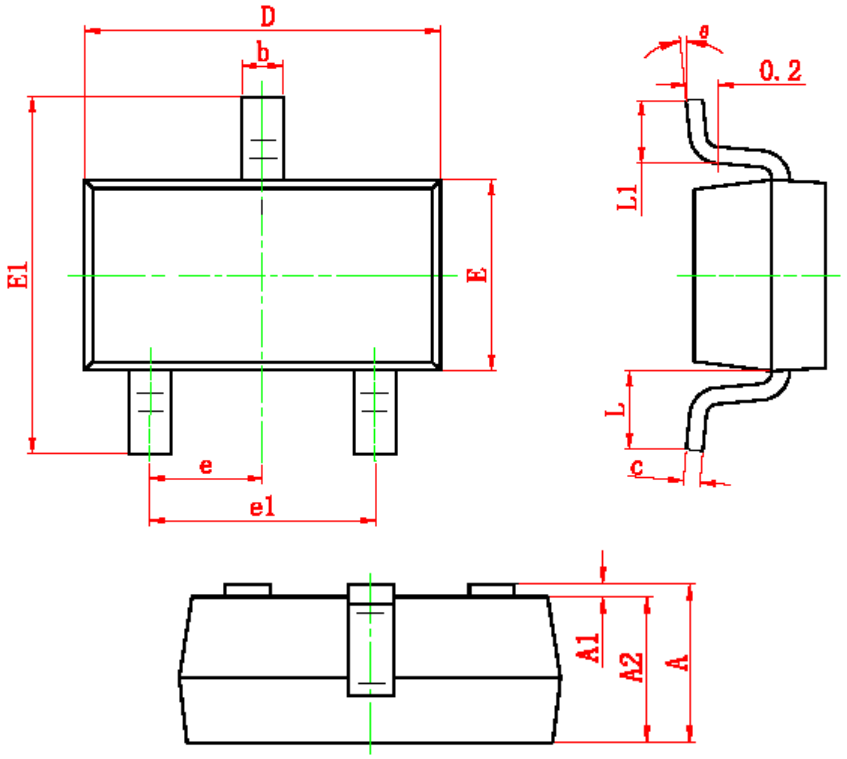
Capacitance vs. Drain-Source Voltage



On-Resistance vs. Drain-Current



SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

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