74HC4024-Q100

7-stage binary ripple counter

Rev. 1 — 27 November 2013 | Product data sheet

1. General description

The 74HC4024-Q100 is a 7-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Low power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Applications

- Frequency dividing circuits
- Time delay circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4024D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC4024PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

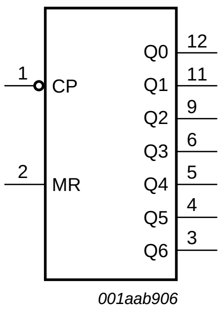


Fig 1. Logic symbol

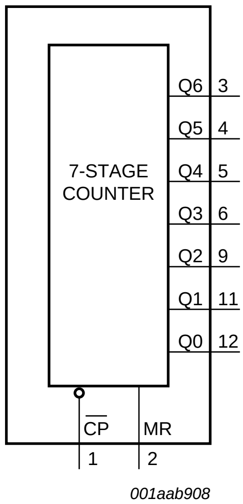


Fig 2. Functional diagram

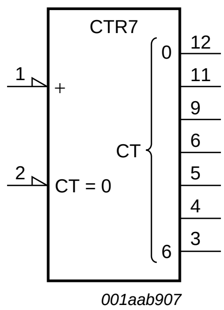


Fig 3. IEC logic symbol

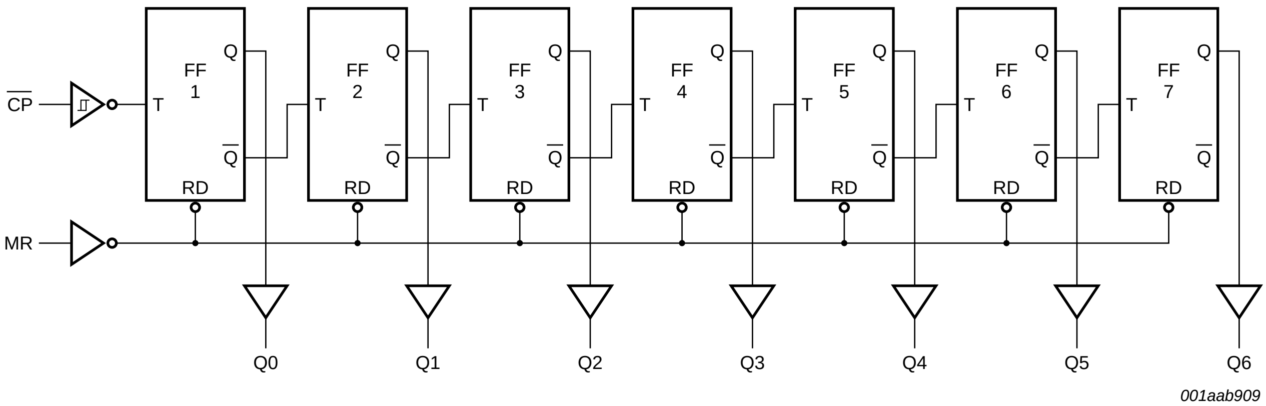


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

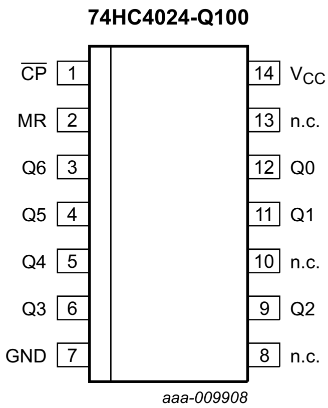


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{CP}$	1	clock input (HIGH-to-LOW, edge-triggered)
MR	2	master reset input (active HIGH)
Q6, Q5, Q4, Q3, Q2, Q2, Q1, Q0	3, 4, 5, 6, 9, 11, 12	parallel output
GND	7	ground (0 V)
n.c.	8, 10, 13	not connected
V_{CC}	14	supply voltage

7. Functional description

Table 3. Function table[1]

Input		Output
MR	**$\overline{CP}$**	**Qn**
H	X	L
L	↑	no change
	↓	count

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V		-	±20	mA
I_{OK}	output clamping current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V		-	±20	mA
I_O	output current	V_O = –0.5 V to V_{CC} + 0.5 V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 4.5$ V	-	-	0.33	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	80	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\ \mu A$; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\ \mu A$; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160	μA

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	47	175	ns
		V_{CC} = 4.5 V		-	17	35	ns
		V_{CC} = 6.0 V		-	14	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	14	-	ns
		Qn to Qn+1; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	25	80	ns
		V_{CC} = 4.5 V		-	9	16	ns
		V_{CC} = 6.0 V		-	7	14	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6					
		V_{CC} = 2.0 V		-	63	200	ns
		V_{CC} = 4.5 V		-	23	40	ns
		V_{CC} = 6.0 V		-	18	34	ns
t_t	transition time	see Figure 6	[2]				
		V_{CC} = 2.0 V		-	19	75	ns
		V_{CC} = 4.5 V		-	7	15	ns
		V_{CC} = 6.0 V		-	6	13	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Figure 6					
		V_{CC} = 2.0 V		80	17	-	ns
		V_{CC} = 4.5 V		16	6	-	ns
		V_{CC} = 6.0 V		14	5	-	ns
		MR HIGH; see Figure 6					
		V_{CC} = 2.0 V		80	22	-	ns
		V_{CC} = 4.5 V		16	8	-	ns
		V_{CC} = 6.0 V		14	6	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Figure 6					
		V_{CC} = 2.0 V		50	6	-	ns
		V_{CC} = 4.5 V		10	2	-	ns
		V_{CC} = 6.0 V		9	2	-	ns
f_{max}	maximum frequency	$\overline{CP}$; see Figure 6					
		V_{CC} = 2.0 V		6.0	27	-	MHz
		V_{CC} = 4.5 V		30	82	-	MHz
		V_{CC} = 6.0 V		35	98	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	90	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[3]	-	25	-	pF

Table 7. Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C							
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	220	ns
		V_{CC} = 4.5 V		-	-	44	ns
		V_{CC} = 6.0 V		-	-	37	ns
		Qn to Qn+1; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	100	ns
		V_{CC} = 4.5 V		-	-	20	ns
		V_{CC} = 6.0 V		-	-	17	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6					
		V_{CC} = 2.0 V		-	-	250	ns
		V_{CC} = 4.5 V		-	-	50	ns
		V_{CC} = 6.0 V		-	-	43	ns
t_t	transition time	see Figure 6	[2]				
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	16	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Figure 6					
		V_{CC} = 2.0 V		100	-	-	ns
		V_{CC} = 4.5 V		20	-	-	ns
		V_{CC} = 6.0 V		17	-	-	ns
		MR HIGH; see Figure 6					
		V_{CC} = 2.0 V		100	-	-	ns
		V_{CC} = 4.5 V		20	-	-	ns
		V_{CC} = 6.0 V		17	-	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Figure 6					
		V_{CC} = 2.0 V		65	-	-	ns
		V_{CC} = 4.5 V		13	-	-	ns
		V_{CC} = 6.0 V		11	-	-	ns
f_{max}	maximum frequency	CP; see Figure 6					
		V_{CC} = 2.0 V		4.8	-	-	MHz
		V_{CC} = 4.5 V		24	-	-	MHz
		V_{CC} = 6.0 V		28	-	-	MHz

Table 7. Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C							
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	265	ns
		V_{CC} = 4.5 V		-	-	53	ns
		V_{CC} = 6.0 V		-	-	45	ns
		Qn to Qn+1; see Figure 6	[1]				
		V_{CC} = 2.0 V		-	-	120	ns
		V_{CC} = 4.5 V		-	-	24	ns
		V_{CC} = 6.0 V		-	-	20	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6					
		V_{CC} = 2.0 V		-	-	300	ns
		V_{CC} = 4.5 V		-	-	60	ns
		V_{CC} = 6.0 V		-	-	51	ns
t_t	transition time	see Figure 6	[2]				
		V_{CC} = 2.0 V		-	-	110	ns
		V_{CC} = 4.5 V		-	-	22	ns
		V_{CC} = 6.0 V		-	-	19	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Figure 6					
		V_{CC} = 2.0 V		120	-	-	ns
		V_{CC} = 4.5 V		24	-	-	ns
		V_{CC} = 6.0 V		20	-	-	ns
		MR HIGH; see Figure 6					
		V_{CC} = 2.0 V		120	-	-	ns
		V_{CC} = 4.5 V		24	-	-	ns
		V_{CC} = 6.0 V		20	-	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Figure 6					
		V_{CC} = 2.0 V		75	-	-	ns
		V_{CC} = 4.5 V		15	-	-	ns
		V_{CC} = 6.0 V		13	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; see Figure 7.

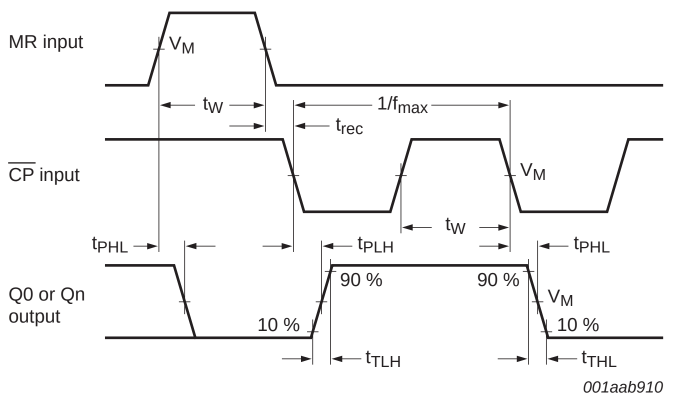
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency	CP; see Figure 6				
		V_{CC} = 2.0 V	4.0	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

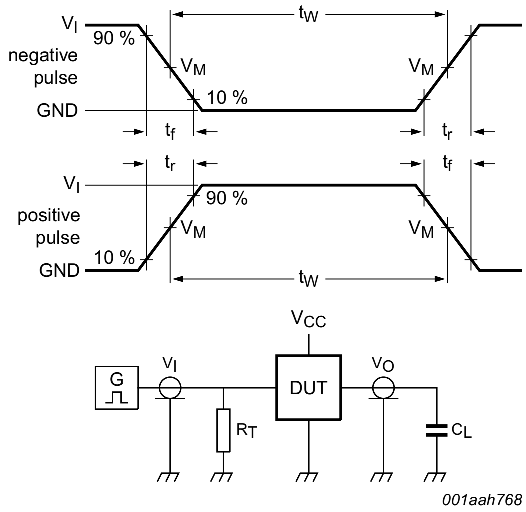
12. Waveforms



Also showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock ($\overline{CP}$) recovery time.

$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the clock ($\overline{CP}$) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum frequency



Test data is given in Table 8.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

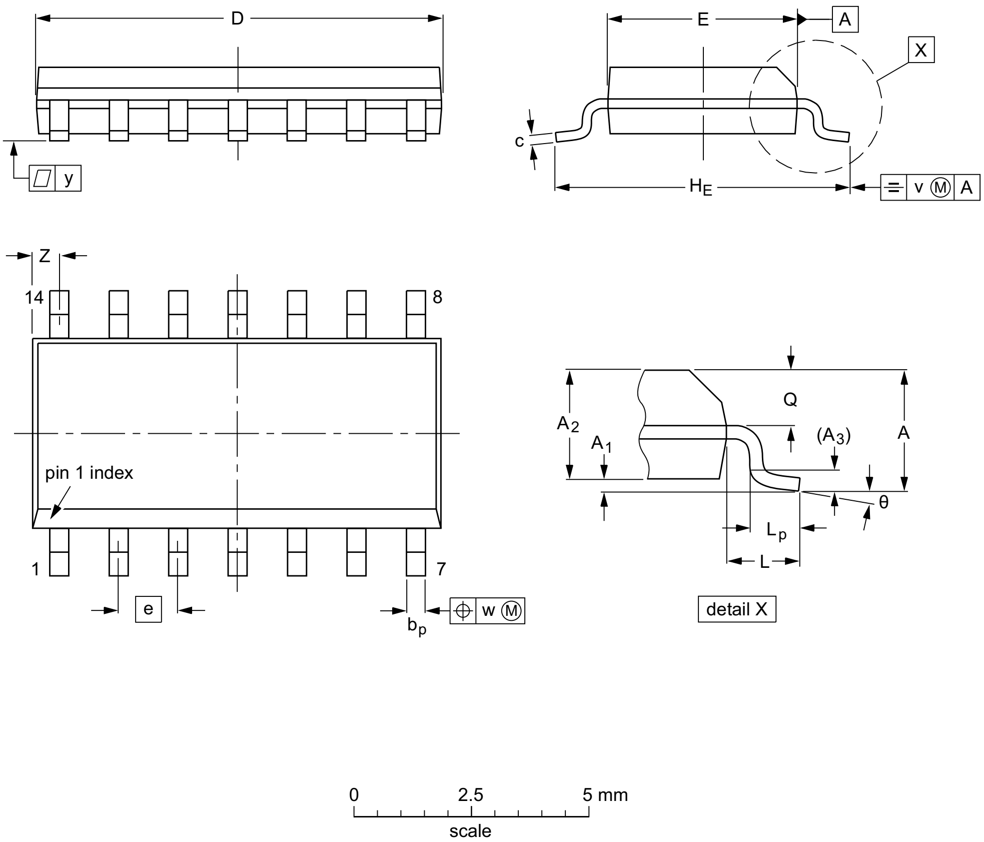
Fig 7. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

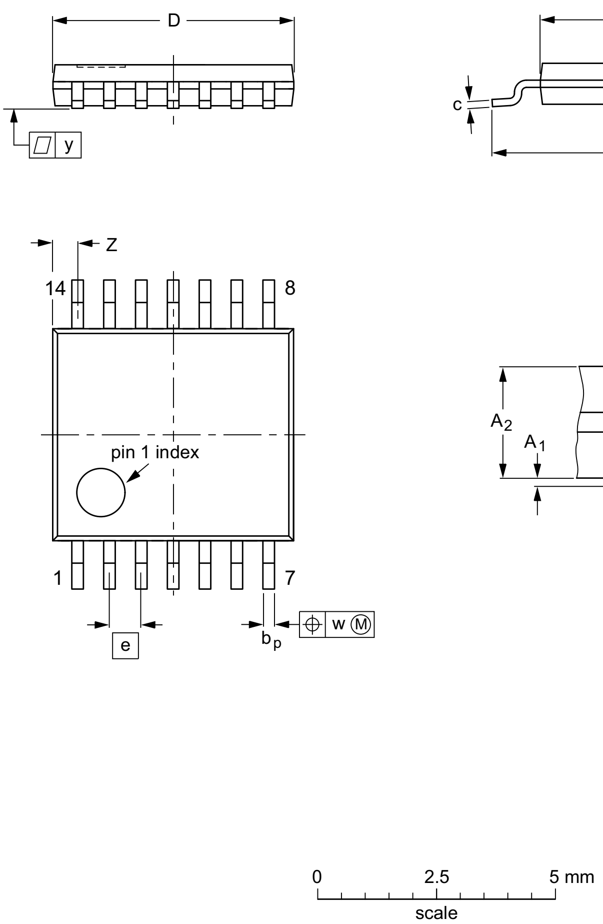
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4024_Q100 v.1	20131127	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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