SYNCHRONOUS PWM CONTROLLER WITH OVER-CURRENT PROTECTION / LDO CONTROLLER

FEATURES

- Synchronous Controller plus one LDO controller
- Current Limit using MOSFET Sensing
- Single 5V/12V Supply Operation
- Programmable Switching Frequency up to 400KHz
- Soft-Start Function
- Fixed Frequency Voltage Mode
- Precision Reference Voltage Available
- Uncommitted Error Amplifier available for DDR
- voltage tracking application

APPLICATIONS

- DDR memory source sink V_{TT} application
- Low cost on-board DC to DC such as 12V/5V to output voltages as low as 0.8V
- Graphic Card
- Hard Disk Drive
- Multi-Output Applications
- RoHS Compliant

DESCRIPTION

The APU3073 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter for multiple output applications.
The outputs can be programmed as low as 0.8V for low voltage applications.

Selectable over-current protection is provided by using external MOSFET's on-resistance for optimum cost and performance.

This device features a programmable frequency set from 200KHz to 400KHz, under-voltage lockout for all input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

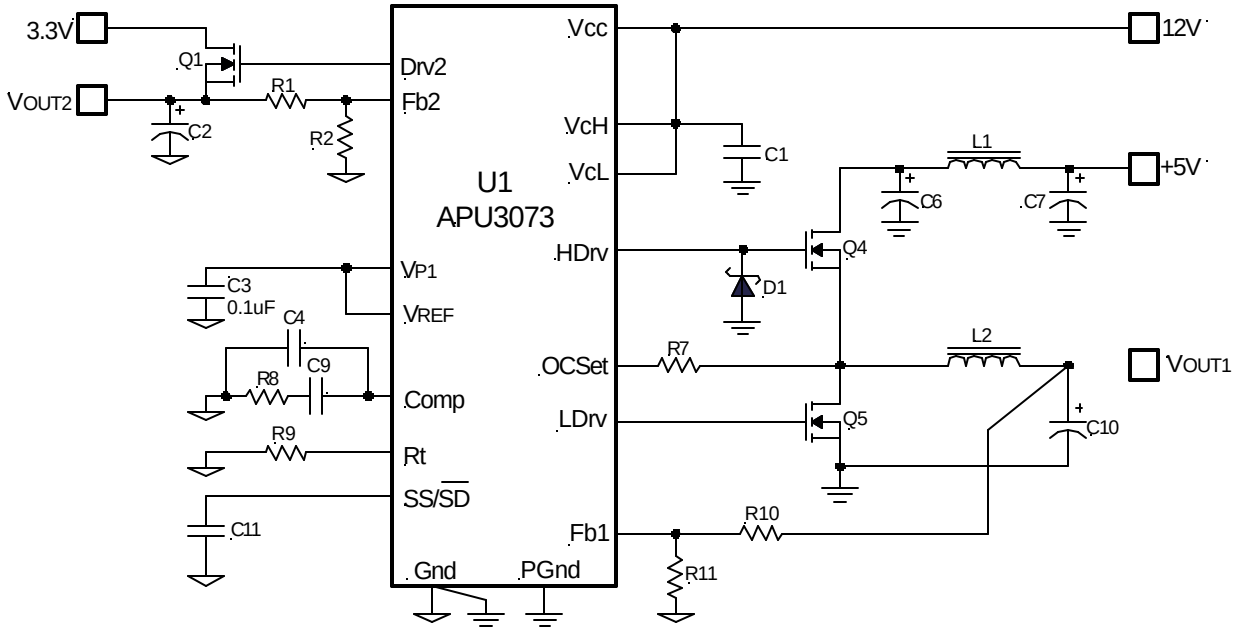


Figure 1 - Typical application of APU3073.

PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	APU3073O	16-Pin TSSOP

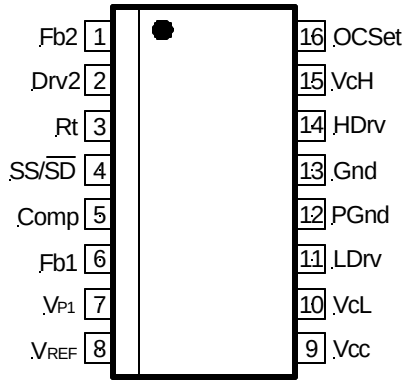
ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage ..... -0.5 - 25V
VcL, VcH Supply Voltage ..... -0.5 - 25V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

PACKAGE INFORMATION

16-Pin TSSOP (O)



θ_{JA}=90°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcL=VcH=12V and T_A=0°C to 70°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
Fb Voltage	V_{FB}		0.784	0.8	0.816	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.625	%
Reference Voltage						
Ref Voltage Initial Accuracy	V_{REF}		0.784	0.8	0.816	V
Drive Current	I_{REF}	Note 1		2		µA
UVLO						
UVLO Threshold - Vcc	UVLO V_{CC}	Supply Ramping Up	3.9	4.4	4.8	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VcH	UVLO V_{CH}	Supply Ramping Up	3.3	3.5	3.7	V
UVLO Hysteresis - VcH				0.2		V
UVLO Threshold - Fb1	UVLO Fb1	Fb Ramping Down	0.3	0.4	0.5	V
UVLO Hysteresis - Fb1				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		5	10	mA
Vc Dynamic Supply Current	Dyn I_C	Freq=200KHz, C_L=1500pF		5	15	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		3.5	10	mA
Vc Static Supply Current	I_{CQ}	SS=0V		3	5	mA
Soft-Start Section						
Charge Current	SS I_B	SS=0V	10	25	30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V	-5	-0.1	+5	μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V	35	55	75	μA
V_P Voltage Range	V_P	Note 1	0.8		1.5	V
Transconductance				700		μmho
Oscillator						
Frequency	Freq	Rt=100K	180	210	240	KHz
		Rt=50K	340	400	460	
Ramp Amplitude	V_{RAMP}	Note 1		1.25		V_{PP}
Output Drivers						
Rise Time	Tr	C_{LOAD}=1500pF		50	100	ns
Fall Time	Tf	C_{LOAD}=1500pF		50	100	ns
Dead Band Time	T_{DB}			100		ns
Max Duty Cycle	D_{MAX}	Fb=0.7V, Freq=200KHz	85	90		%
Min Duty Cycle	D_{MIN}	Fb=0.9V	0			%
LDO Controller Section						
Drive Current	Drv1		40	65		mA
Fb Voltage			0.784	0.8	0.816	V
Input Bias Current			-1	-0.1	+1	μA
Thermal Shutdown		Note 1		150		°C
Current Limit						
OC Threshold Set Current	I_{OCSET}		20	30	40	μA
OC Comp Off-Set Voltage	$V_{OC(OFFSET)}$		-5	0	+5	mV

Note 1: Guaranteed by design but not tested in production.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb2	These pins provide feedback for the linear regulator controllers.
2	Drv2	Outputs of the linear regulator controllers.
3	Rt	A resistor should be connected from this pin to ground for setting the switching frequency.
4	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin down below 0.4V.
5	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
6	Fb1	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
7	V_{P1}	Non-inverting input of error amplifier.
8	V_{REF}	Reference voltage.
9	Vcc	This pin provides biasing for the internal blocks of the IC as well as powers the LDO controller. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
10	VcL	This pin powers the low side output driver and can be connected either to Vcc or separate supply. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
11	LDrv	Output driver for the synchronous power MOSFET.

PIN#	PIN SYMBOL	PIN DESCRIPTION
12	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to system's ground plane.
13	Gnd	This pin serves as analog ground for internal reference and control circuitry. A high frequency capacitor must be connected from Vcc pin to this pin for noise free operation.
14	HDrv	Output driver for the high side power MOSFET. This pin should not go negative (below ground), this may cause problem for the gate drive circuit. It can happen when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load. To prevent negative voltage at gate drive, a low forward voltage drop diode might be connected between this pin and ground.
15	VcH	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
16	OCSet	This pin is connected to the Drain of the lower MOSFET via an external resister and it provides the positive sensing for the internal current sensing circuitry. The external resistor programs the current limit threshold depending on the $R_{DS(ON)}$ of the power MOSFET. An external capacitor can be placed in parallel with the programming resistor to provide high frequency noise filtering.

BLOCK DIAGRAM

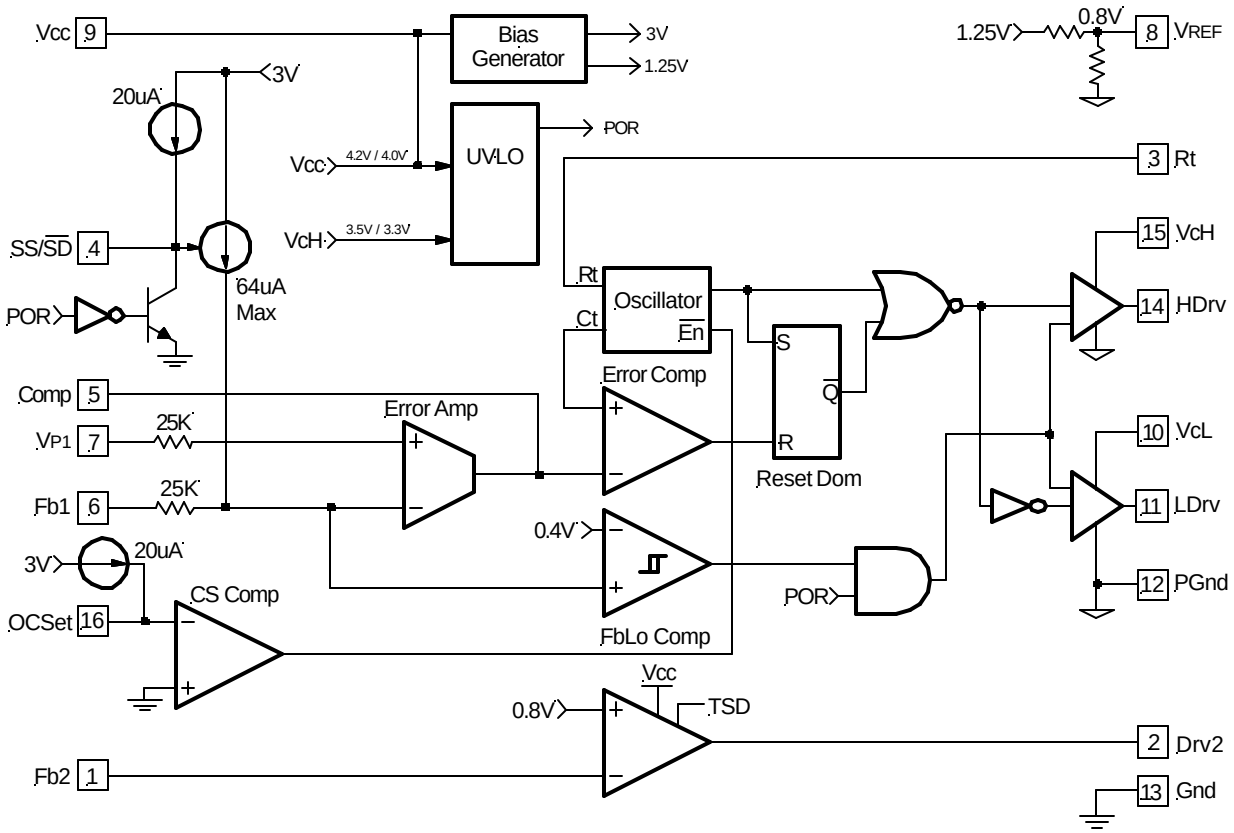


Figure 2 - Simplified block diagram of the APU3073.

THEORY OF OPERATION

Introduction

The APU3073 is designed for a two output application and it includes one synchronous buck controller and a linear regulator controller. The PWM section is a fixed frequency, voltage mode and consists of a precision reference voltage, an uncommitted error amplifier, an internal oscillator, a PWM comparator, an internal regulator, a comparator for current limit, gate drivers, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the voltage on non-inverting input of error amplifier(V_P). This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor. The oscillation frequency is programmable between 200KHz to 400KHz by using an external resistor. Figure 14 shows switching frequency vs. external resistor (Rt).

Soft-Start

The APU3073 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the input supplies rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter and disables the short circuit protection. During the power up of the buck converter, the output starts at zero and voltage at Fb1 is below 0.4V. The feedback UVLO is disabled during this time by injecting a current (64μA) into the Fb1. This generates a voltage about 1.6V (64μA × 25K) across the negative input of E/A and positive input of the feedback UVLO comparator (see Fig3).

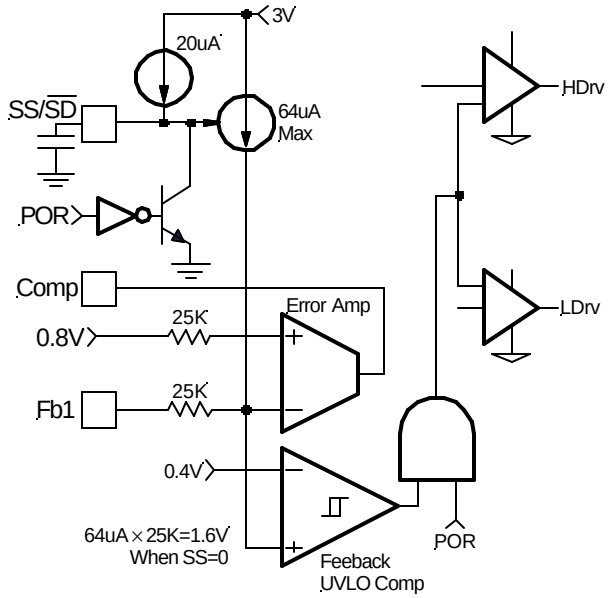


Figure 3 - APU3073 soft-start diagram.

The magnitude of this current is inversely proportional to the voltage at soft-start pin.

The 20μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb1 pin starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb1 pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25K = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb1 pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb1 is:

$$V_{FB1} = 0.8\text{-}25K \times (\text{Injected Current})$$

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

As shown in Figure 4, the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

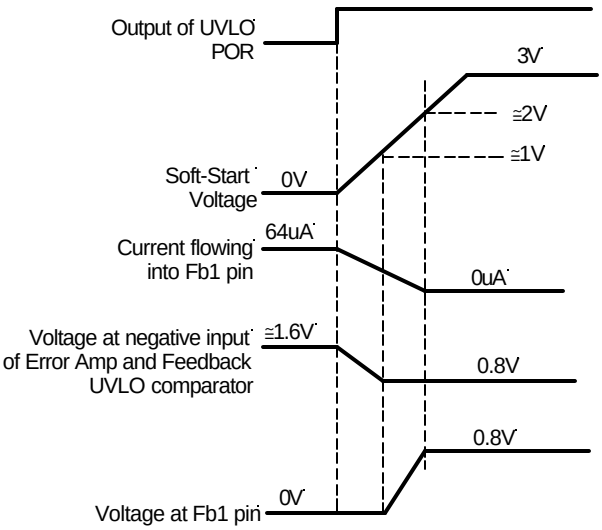


Figure 4 - Theoretical operation waveforms during Soft-Start.

From this analysis, the output start-up time is defined as when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor and can be estimated by:

$$20\mu A \times T_{START}/C_{SS} = 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be calculated as:

$$C_{SS} = 20\mu A \times T_{START}/1V$$

MOSFET Drivers

The driver capabilities of both high and low side drivers are optimized to maintain fast switching transitions. They are sized to drive a MOSFET that can deliver up to 20A output current.

The low side MOSFET diver is supplied directly by V_{CC} while the high side driver is supplied by V_C.

An internal dead time control is implemented to prevent cross-conduction and allows the use of several kinds of MOSFETs.

LDO Controller

The LDO section is powered directly from Vcc. The output of LDO can be set as low as 0.8V and can be programmed to higher voltages by using two external resistors.

Supply Voltage Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs, remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vcc or VcH fall below 4.0V and 3.3V respectively. Normal operation resumes once these voltages rise above the set values.

Shutdown

The PWM section can be shutdown by pulling the soft-start pin below 0.4V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Over-Current Protection

Over-current protection is achieved with a cycle by cycle scheme and it is performed by sensing current through the $R_{DS(ON)}$ of low side MOSFET. As shown in Figure 5, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) and sets the current limit set point. The internal current source develops a voltage across R_{SET}. When the low side switch is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times i_L \qquad \text{---(1)}$$

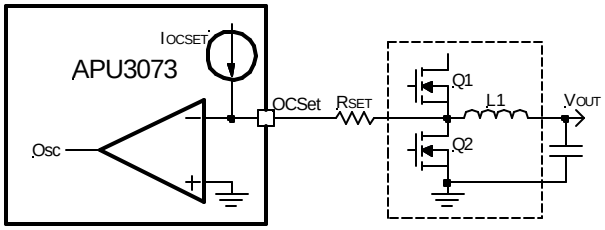


Figure 5 - Diagram of the over current sensing.

When voltage V_{OCSET} is below zero, the current sensing comparator flips and disables the oscillator. The high side MOSFET is turned off and the low side MOSFET is turned on until the inductor current reduces to below current set value. The critical inductor current can be calculated by setting:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCSET}}{R_{DS(ON)}} \qquad \text{---(2)}$$

If the over-current condition is temporary and goes away quickly, the APU3073 will resume its normal operation.

If output is shorted or over-current condition persists, the output voltage will keep going down until it is below 0.4V. Then the output under-voltage lock out comparator goes high and turns off both MOSFETs. The operation waveforms are shown in Figure 6.

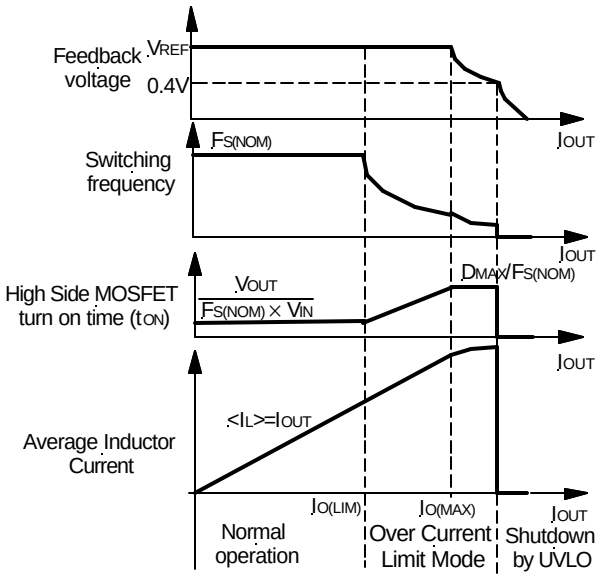


Figure 6 - Diagram of over-current operation.

Operation in current limit is shown in Figure 7, the high side MOSFET is turned off and inductor current starts to decrease. Because the output inductor current is higher than the current limit setpoint (I_{SET}), the over-current comparator keeps high until the inductor current decreases to be below I_{SET}. Then another cycle starts.

During over-current mode, the valley inductor current is:

$$i_{L(VALLEY)} = I_{SET}$$

The peak inductor current is given as:

$$I_{L(PEAK)} = I_{SET} + (V_{IN} - V_{OUT}) \times t_{ON} / L \qquad ---(3)$$

To avoid undesirable trigger of over-current protection, this relationship must be satisfied:

$$I_{SET} \geq I_{O(NOM)} - \frac{\Delta I_{PK-PK(NOM)}}{2}$$

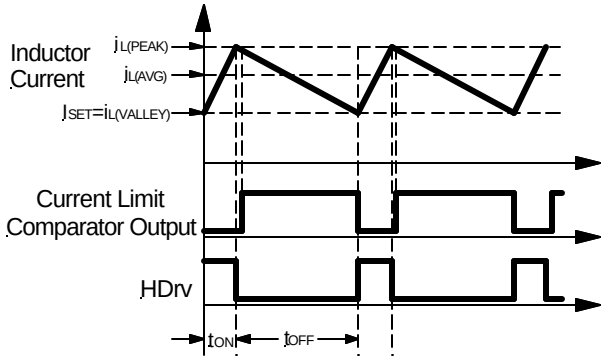


Figure 7 - Operation waveforms during current limit.

From Figure 7, the average inductor current during the current limit mode is:

$$I_{O(LIM)} = I_{SET} + \frac{\Delta I_{PK-PK(LIM)}}{2} \qquad ---(4)$$

The inductor's ripple current can be expressed as:

$$\Delta I_{PK-PK(LIM)} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times f_S}$$

Combination of above equation and (4) results in:

$$I_{SET} = I_{O(LIM)} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times f_S \times L \times V_{IN}} \right) \qquad ---(5)$$

Combination of equations (5) and (2) results in the relationship between R_{SET} and output current limit:

$$R_{SET} = \frac{R_{DS(ON)}}{I_{OCSET}} \times \left[I_{O(LIM)} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times f_S \times L \times V_{IN}} \right) \right] \qquad ---(6)$$

Where:

$I_{O(LIM)}$ = The Output Current Limit -typical is 50% higher than nominal output current.

V_{IN} = Maximum Input Voltage

V_{OUT} = Output Voltage

f_S = Switching Frequency

L = Output Inductor

$R_{DS(ON)}$ = $R_{DS(ON)}$ of Low Side MOSFET

I_{OCSET} = OC Threshold Set Current

From the above analysis, the current limit is not only dependent on the current setting resistor R_{SET} and $R_{DS(ON)}$ of low side MOSFET but it is also dependent on the input voltage, output voltage, inductance and switching frequency as well.

The cycle-by-cycle over-current limit will hold for a certain amount of time, until the output voltage drops below 0.4V, the under-voltage lock out activates and latches off the output driver. The operation waveform is shown in Figure 4. Normal operation will resume after APU3073 is powered up again.

APPLICATION INFORMATION

Design Example:

The following example is a typical application for APU3073, the schematic is Figure 17 on page 16.

Supply Voltage	Switcher	Linear Regulator
V_{CC}=V_{CL}=V_{CH}=12V	V_{IN} = 5V	V_{IN} = 2.5V
	V_{OUT} = 2.5V	V_{OUT} = 1.6V
	I_{OUT} = 8A	I_{OUT} = 2A
	ΔV_{OUT} = 50mV	
	f_S = 200KHz	

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is referenced to the voltage on non-inverting pin of error amplifier. For this application, this pin (V_P) is connected to reference voltage (V_{REF}). The output voltage is defined by using the following equation:

$$V_{OUT} = V_P \times \left(1 + \frac{R_6}{R_5}\right) \quad ---(7)$$

$V_P = V_{REF} = 0.8V$

When an external resistor divider is connected to the output as shown in Figure 8.

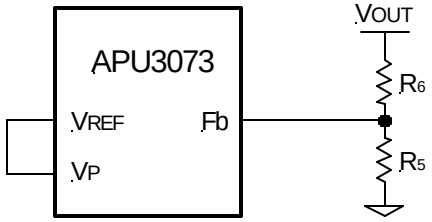


Figure 8 - Typical application of the APU3039 for programming the output voltage.

Equation (7) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_P} - 1\right)$$

Choose R_5 = 1K. This will result to R_6 = 2.15K

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$Css \cong 20 \times t_{START} \quad (\mu F) \quad ---(8)$$

Where t_{START} is the desirable start-up time (s)

For a start-up time of 5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Supply VcL and VcH

To drive the high side switch, it is necessary to supply a gate voltage at least 4V greater than the Bus voltage. For this application, VcL and VcH are biased with a separate 12V supply.

Input Capacitor Selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT}\sqrt{D \times (1\text{-}D)} \quad ---(9)$$

Where:

D is the Duty Cycle, D=V_{OUT}/V_{IN}.

I_{RMS} is the RMS value of the input capacitor current.

I_{OUT} is the output current for each channel.

For V_{IN}=5V, I_{OUT}=8A and D=0.5, the I_{RMS}=4A

For higher efficiency, a low ESR capacitor is recommended. Choose two Poscap from Sanyo 6TPB47M (16V, 47μF) with a max allowable ripple current of 5.2A.

Inductor Selection

The inductor is selected based on operating frequency, transient performance and allowable output voltage ripple.

Low inductor value results to faster response to step load (high di/dt) and smaller size but will cause larger output ripple due to increase of inductor ripple current. As a rule of thumb, select an inductor that produces a ripple current of 10-40% of full load DC.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \quad ---(11)$$

Where:

V_{IN} = Maximum Input Voltage

V_{OUT} = Output Voltage

Δi = Inductor Ripple Current

f_S = Switching Frequency

Δt = Turn On Time

D = Duty Cycle

If $\Delta i = 25\%(I_O)$, then the output inductor will be:

$L = 3.125\mu H$

The Coilcraft DO5022HC series provides a range of inductors in different values, low profile suitable for large currents. 3.3μH is a good choice for this application. This will result to a ripple approximately 23% of output current.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad \text{---(10)}$$

Where:

ΔV_O = Output Voltage Ripple

Δi = Inductor Ripple Current

ΔV_O = 50mV and $\Delta I \cong$ 23% of 8A = 1.89A

This results to: ESR=26.5mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC330M, 330μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of ≅ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Power MOSFET Selection

The APU3073 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7832 for both control MOSFET and synchronous MOSFET. This device provides low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7832

V_{DSS} = 30V

I_D = 16A @ 70°C

$R_{DS(ON)}$ = 4mΩ

The total conduction losses will be:

$$P_{CON(TOTAL)} = P_{CON(UPPER)} + P_{CON(LOWER)}$$

$P_{CON(TOTAL)}$ = 0.38W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad \text{---(12)}$$

Where:

$V_{DS(OFF)}$ = Drain to Source Voltage at off time

t_r = Rise Time

t_f = Fall Time

T = Switching Period

I_{LOAD} = Load Current

The switching time waveform is shown in Figure 9.

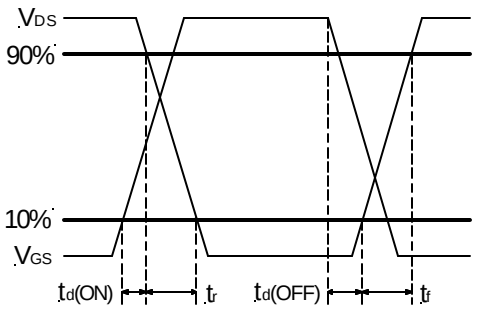


Figure 9 - Switching time waveforms.

From IRF7832 data sheet we obtain:

IRF7832

t_r = 12.3ns

t_f = 21ns

These values are taken under a certain condition test. For more details please refer to the IRF7832 datasheet.

By using equation (12), we can calculate the total switching losses.

$P_{SW(TOTAL)}$ = 133mW

Programming the Over-Current Limit

The over-current threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (2).

The $R_{DS(ON)}$ has a positive temperature coefficient and it should be considered for the worse case operation.

$R_{DS(ON)} = 4m\Omega \times 1.5 = 6m\Omega$

$I_{SET} \cong I_{O(LIM)} = 8A \times 1.5 = 12A$

(50% over nominal output current)

This results to: $R_{SET} \cong 4.8K\Omega$

Select: $R_{SET} = 5K\Omega$

Feedback Compensation

The APU3073 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 10). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad \text{---(13)}$$

Figure 10 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

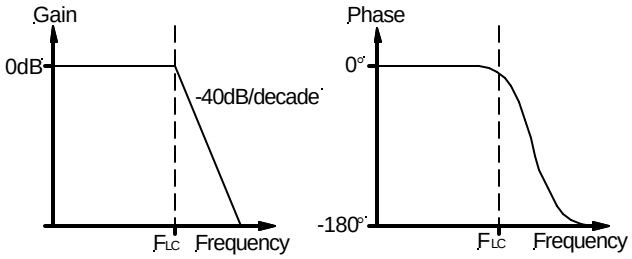


Figure 10 - Gain and phase of LC filter.

The APU3073's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 11.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad \text{---(14)}$$

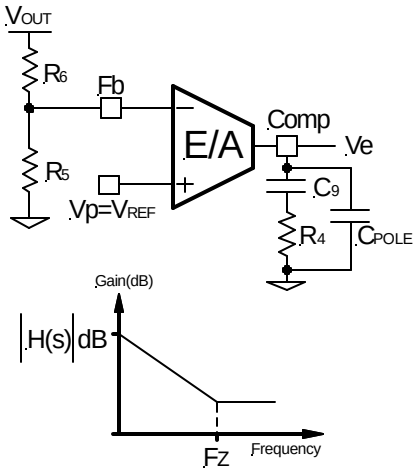


Figure 11 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(15)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s=j \times 2\pi \times F_O)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(16)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(17)$$

|H(s)| is the gain at zero cross frequency.

First select the desired zero-crossover frequency (Fo):

$$Fo > F_{ESR} \text{ and } F_O \leq (1/5 \sim 1/10) \times f_S$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(18)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:

V_{IN} = 5V	F_{LC} = 3.41KHz
V_{OSC} = 1.25V	R_5 = 1K
Fo = 20KHz	R_6 = 2.15K
F_{ESR} = 12KHz	g_m = 700μmho

This results to R_4=23.14K
Choose R_4=24K

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\%F_{LC}$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(19)$$

For:

Lo = 3.3μH	F_Z = 2.5KHz
Co = 660μF	R_4 = 24K

Using equations (17) and (19) to calculate C_9, we get:

$C_9 \cong$ 2590pF; Choose C_9=2200pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for ceramic capacitor with very low ESR and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 12.

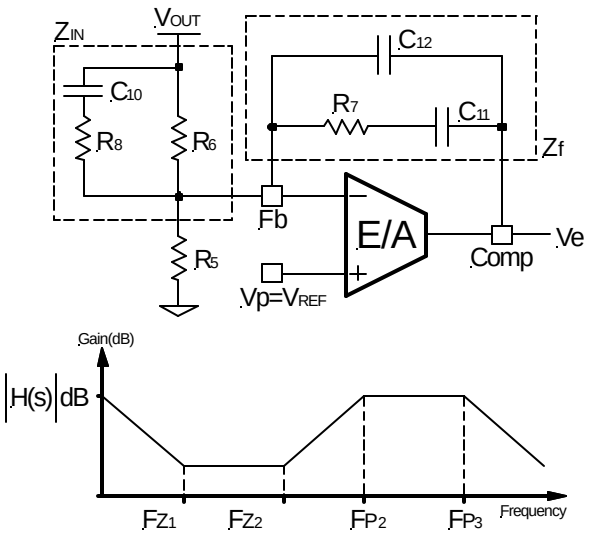


Figure 12 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(20)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(21)}$$

Where:

V_{IN} = Maximum Input Voltage

V_{OSC} = Oscillator Ramp Voltage

Lo = Output Inductor

Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (20) regarding transconductance error amplifier.

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Based on the frequency of the zero generated by ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation type and location of crossover frequency.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{PO} < F_{ZO} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{PO} < F_O < F_{ZO} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{PO} < F_O < f_S/2 < F_{ZO}$	Ceramic

Table - The compensation type and location of zero crossover frequency.

Detail information is dicussed in application Note AN-1043 which can be downloaded from the IR Web-Site.

LDO Section

Output Voltage Programming

Output voltage for LDO is programmed by reference voltage and external voltage divider. The Fb2 pin is the inverting input of the error amplifier, which is internally referenced to 0.8V. The divider is ratioed to provide 0.8V at the Fb2 pin when the output is at its desired value. The output voltage is defined by using the following equation

$$V_{OUT2} = V_{REF} \times \left(1 + \frac{R_7}{R_{10}}\right)$$

For:

V_{OUT2} = 1.6V

V_{REF} = 0.8V

R_{10} = 1KΩ

Results to R_7=1KΩ

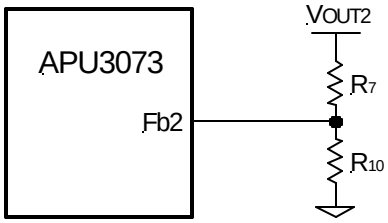


Figure 13 - Programming the output voltage for LDO.

LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the linear regulator is to select the maximum $R_{DS(ON)}$ based on the input to the dropout voltage and the maximum load current.

$$R_{DS(ON)} = \frac{V_{IN(LDO)} - V_{OUT2}}{I_{OUT2}}$$

For:

$V_{IN(LDO)}$ = 2.5V

V_{OUT2} = 1.6V

I_{OUT2} = 2A

Results to: $R_{DS(ON)(MAX)}$ = 0.45Ω

Note that since the MOSFET $R_{DS(ON)}$ increases with temperature, this number must be divided by ~1.5 in order to find the $R_{DS(ON)(MAX)}$ at room temperature. The IRLR2703 has a maximum of 0.065Ω $R_{DS(ON)}$ at room temperature, which meets our requirements.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET. To reduce the ESR, replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources and be placed close to the IC. In multilayer PCB, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

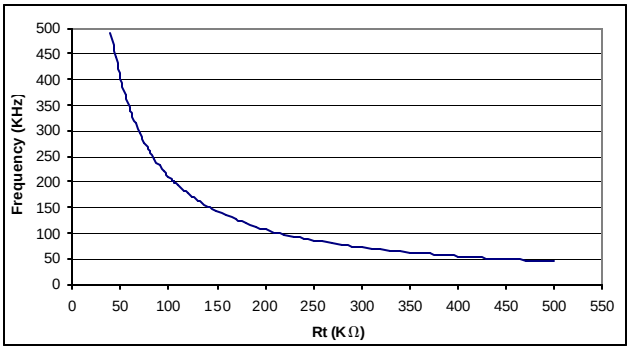


Figure 14 - Switching Frequency vs. Rt.

TYPICAL APPLICATION

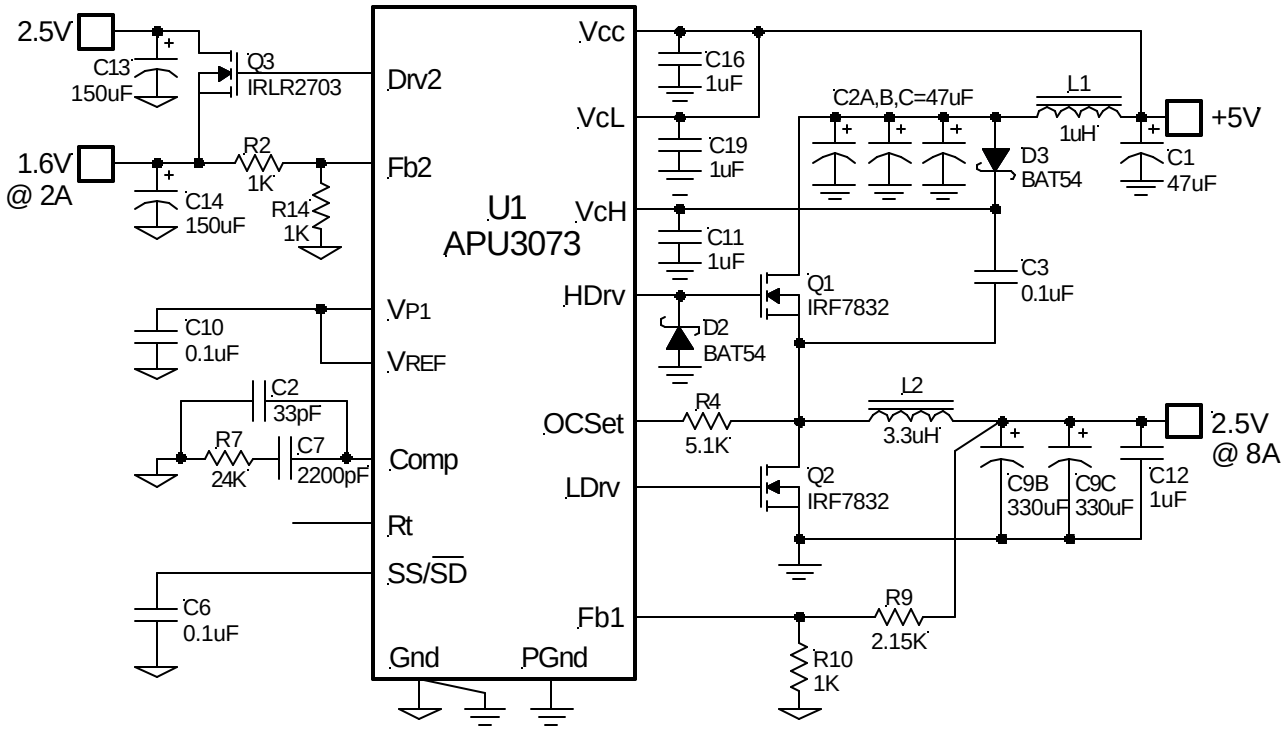


Figure 15 - Typical application of APU3073 for single 5V.

TYPICAL APPLICATION

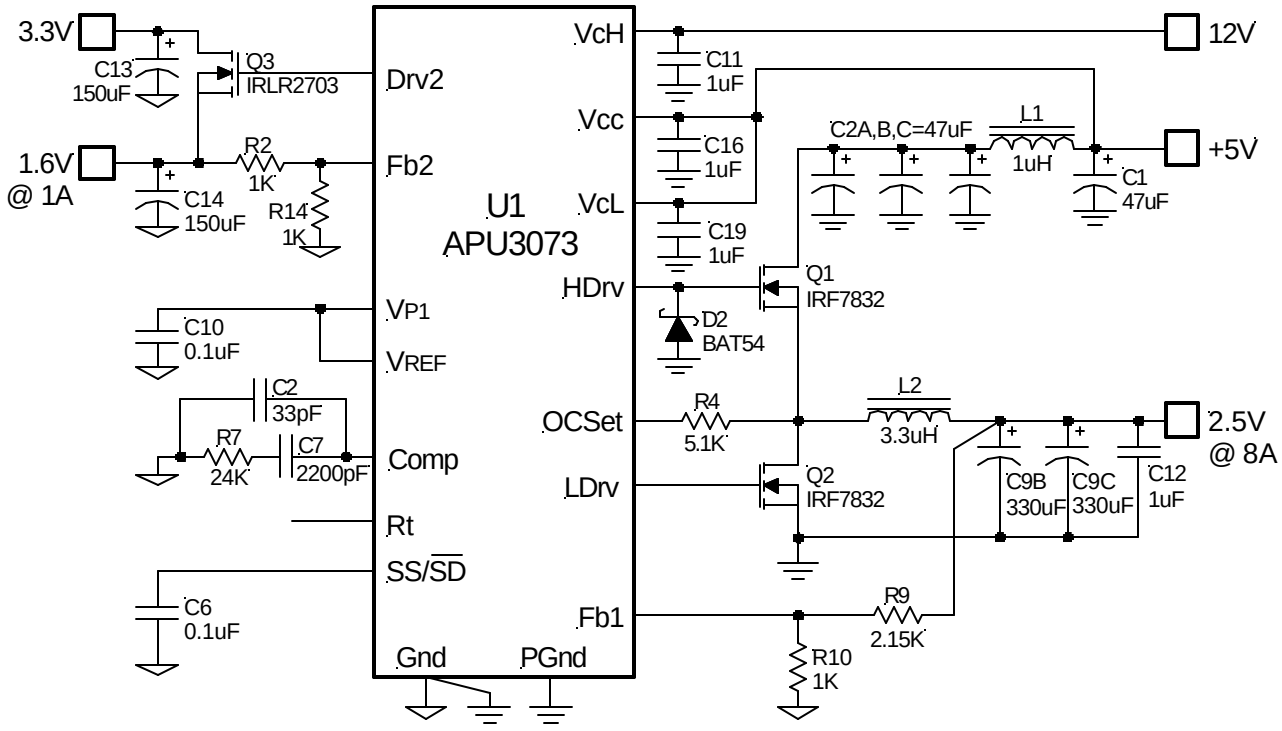


Figure 16 - Typical application of APU3073.

APPLICATION EXPERIMENTAL WAVEFORMS

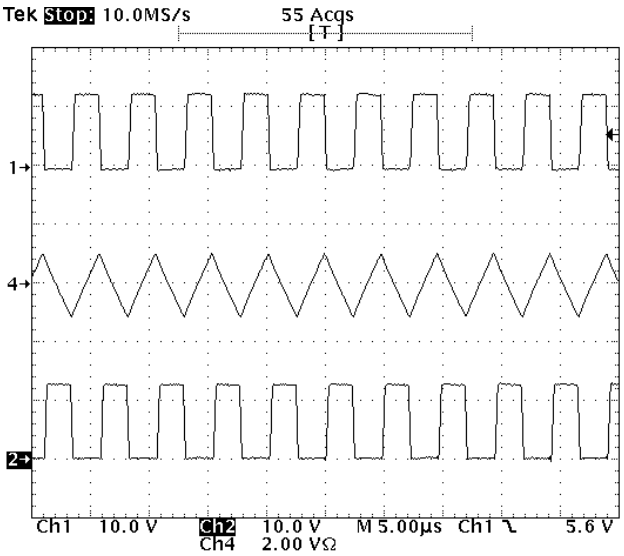


Figure 18 - Normal condition at no load.
Ch1: HDrv
Ch2: LDrv
Ch4: Inductor Current

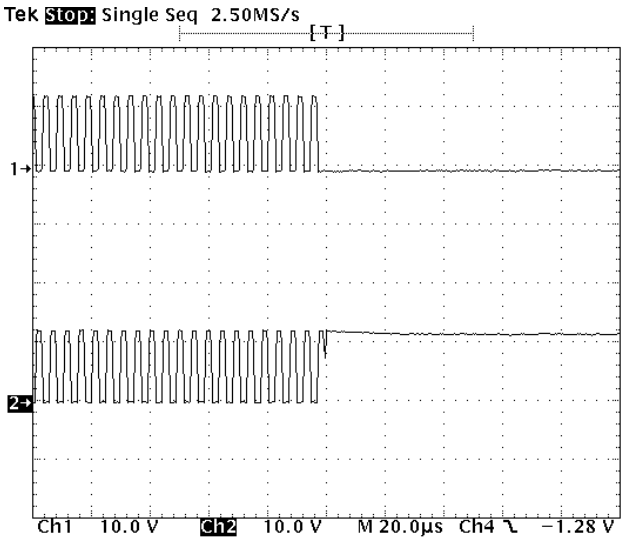


Figure 19 - Gate signals when SS pin pulls low.
Ch1: HDrv
Ch2: LDrv

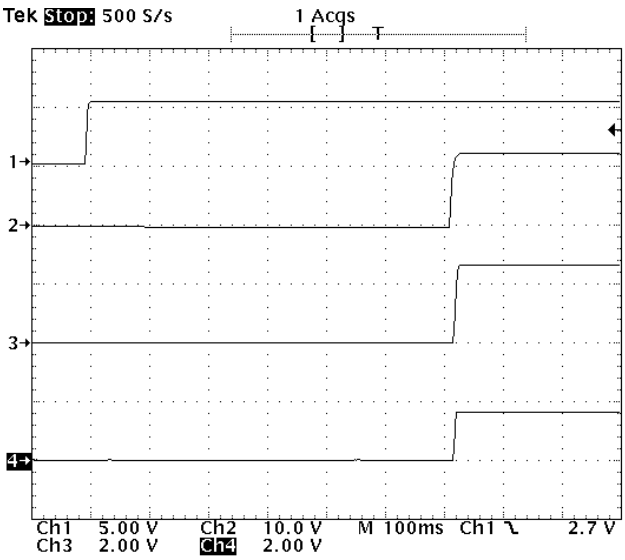


Figure 20 - Soft-Start.
Ch1: V_{IN} (5V)
Ch2: Bias Voltage (12V)
Ch3: V_{OUT1} (PWM)
Ch4: V_{OUT2} (LDO)

APPLICATION EXPERIMENTAL WAVEFORMS

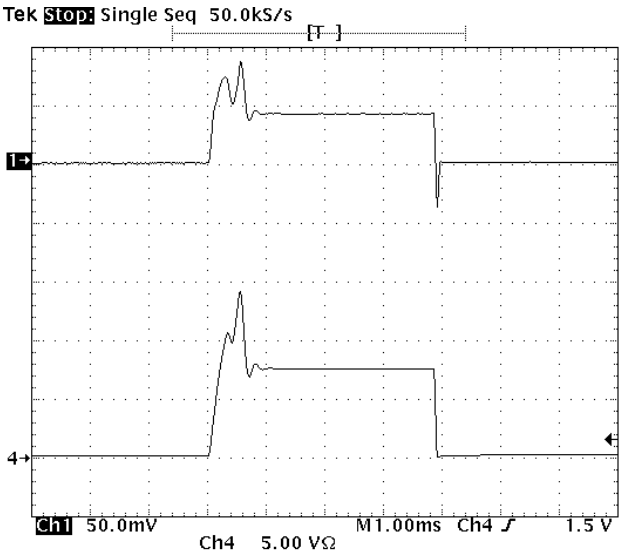


Figure 21 - Output Shorted at start-up.
Ch1: V_{OUT}
Ch4: I_{OUT}

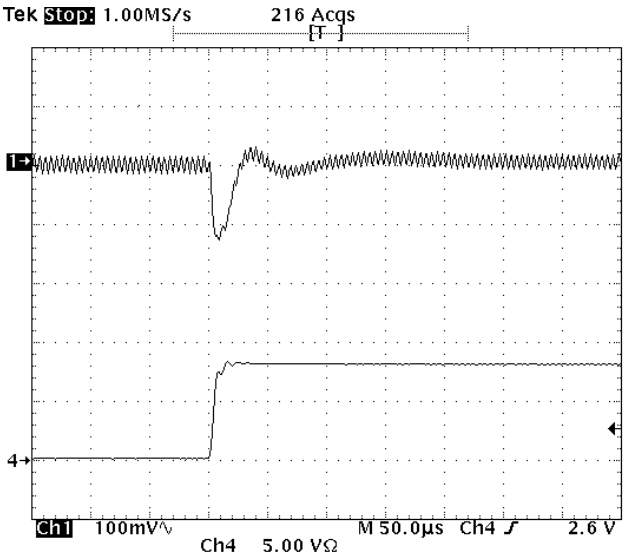


Figure 22 - Load Transient Response (PWM Section).
Ch1: V_{OUT1}
Ch4: I_{OUT1} (0-8A)

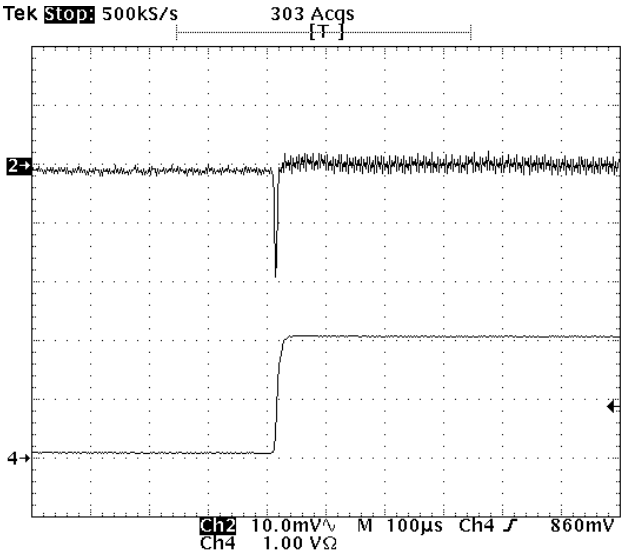


Figure 23 - Load Transient Response (LDO Section).
Ch2: V_{OUT2}
Ch4: I_{OUT2} (0-2A)