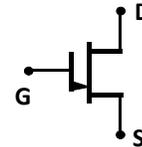
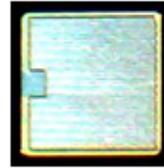


## Normally – OFF Silicon Carbide Junction Transistor

$V_{DS}$	=	1200 V
$R_{DS(ON)}$	=	60 m $\Omega$
$I_D$ ( $T_c = 25^\circ\text{C}$ )	=	45 A
$h_{FE}$ ( $T_c = 25^\circ\text{C}$ )	=	80

### Features

- 250°C maximum operating temperature
- Gate Oxide Free SiC switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Co-efficient of  $R_{DS,ON}$
- Suitable for connecting an anti-parallel diode



### Advantages

- Compatible with Si MOSFET/IGBT gate-drivers
- > 20  $\mu\text{s}$  Short-Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

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### Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$	1200	V	
Continuous Drain Current	$I_D$	$T_c = 25^\circ\text{C}$	45	A	
Continuous Drain Current	$I_D$	$T_c = 145^\circ\text{C}$	20	A	
Continuous Gate Current	$I_G$		1.3	A	
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 250^\circ\text{C}$ , Clamped Inductive Load	$I_{D,max} = 20$ @ $V_{DS} \leq V_{DSmax}$	A	
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 250^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 800\text{ V}$ , Non Repetitive	20	$\mu\text{s}$	
Reverse Gate – Source Voltage	$V_{SG}$		30	V	
Reverse Drain – Source Voltage	$V_{SD}$		25	V	
Storage Temperature	$T_{stg}$		-55 to 250	$^\circ\text{C}$	

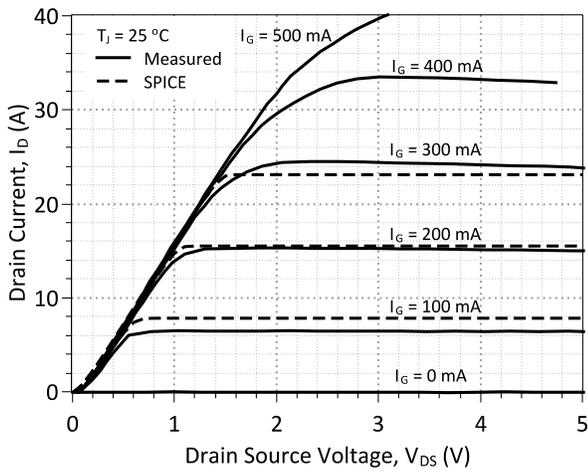
**Section II: Static Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: On State</b>							
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 20\text{ A}, T_J = 25\text{ °C}$		60		mΩ	Fig. 5
		$I_D = 20\text{ A}, T_J = 125\text{ °C}$		96			
		$I_D = 20\text{ A}, T_J = 175\text{ °C}$		128			
Gate On Voltage	$V_{GS,ON}$	$I_D = 20\text{ A}, V_{DS} = 16\text{ V}, T_J = 25\text{ °C}$		3.7		V	Fig. 4
		$I_D = 20\text{ A}, V_{DS} = 16\text{ V}, T_J = 175\text{ °C}$		3.4			
DC Current Gain	$h_{FE}$	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}, T_J = 25\text{ °C}$		80		–	Fig. 5
		$V_{DS} = 5\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ °C}$		50			
		$V_{DS} = 5\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ °C}$		43			
<b>B: Off State</b>							
Drain Leakage Current	$I_{DSS}$	$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25\text{ °C}$		0.1		μA	Fig. 6
		$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		0.1			
		$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$		1			
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20\text{ V}, T_J = 25\text{ °C}$		20		nA	

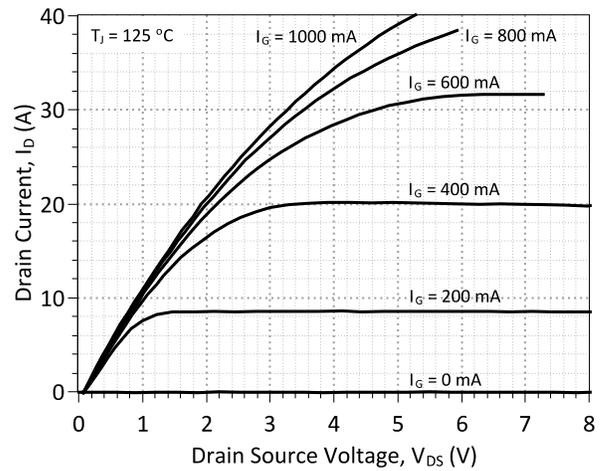
**Section III: Dynamic Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		3091		pF	Fig. 9
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		53		pF	Fig. 9
Output Capacitance Stored Energy	$E_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		17		μJ	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		96		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		70		pF	
Gate-Source Charge	$Q_{GS}$	$V_{GS} = -5\dots 3\text{ V}$		23		nC	
Gate-Drain Charge	$Q_{GD}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		77		nC	
Gate Charge - Total	$Q_G$			100		nC	
Gate Resistance, Internal	$R_{G(INT-ZERO)}$	$f = 1\text{ MHz}, V_{AC} = 50\text{ mV}, V_{DS} = 0\text{ V}, V_{GS} = 0\text{ V}, T_J = 250\text{ °C}$		1.7		Ω	
	$R_{G(INT-ON)}$	$V_{GS} > 2.5\text{ V}, V_{DS} = 0\text{ V}, T_J = 250\text{ °C}$		0.13		Ω	

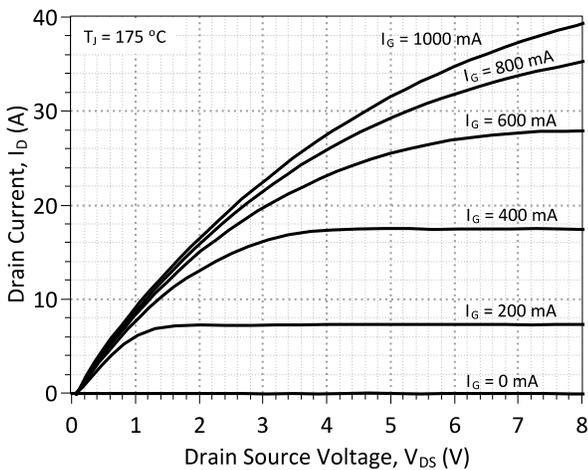
**Section IV: Figures**



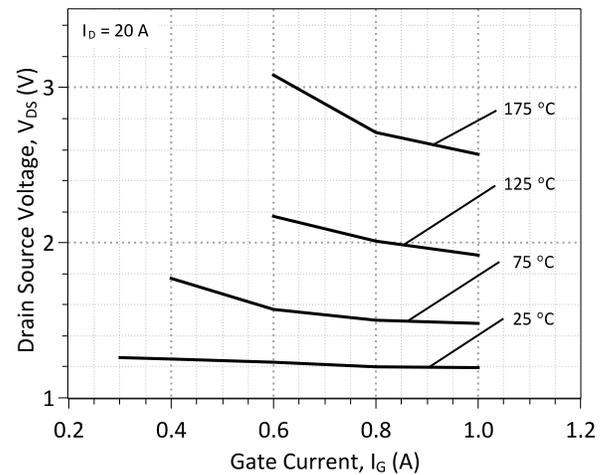
**Figure 1: Typical Output Characteristics at 25 °C**



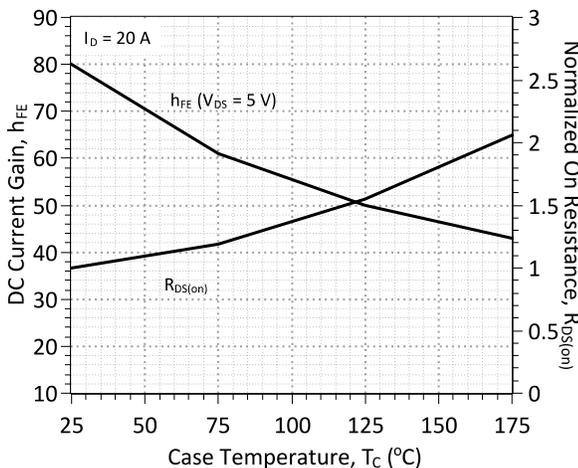
**Figure 2: Typical Output Characteristics at 125 °C**



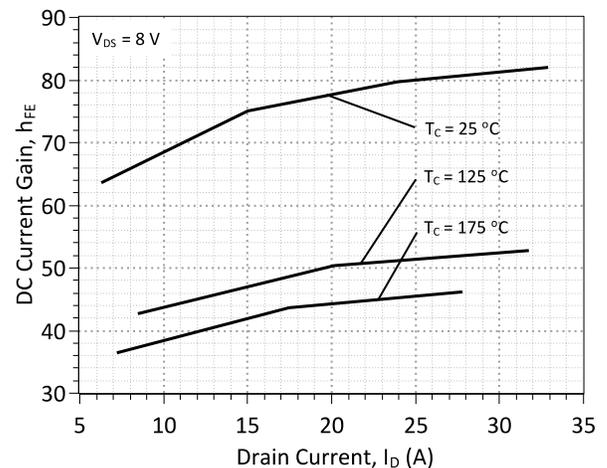
**Figure 3: Typical Output Characteristics at 175 °C**



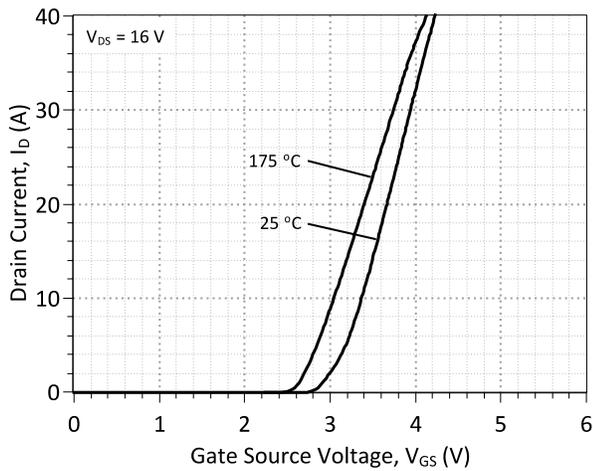
**Figure 4: Drain-Source Voltage vs. Gate Current**



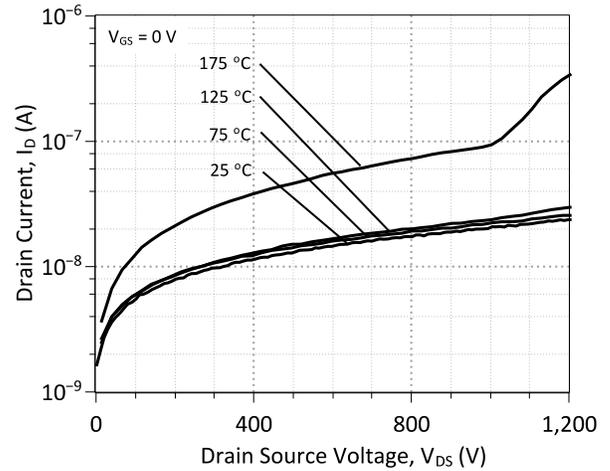
**Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature**



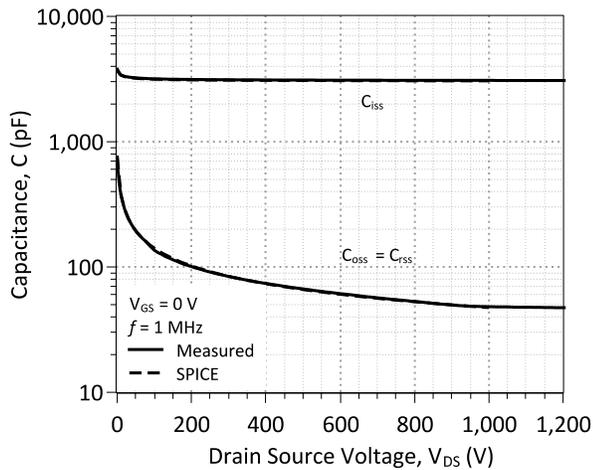
**Figure 6: DC Current Gain vs. Drain Current**



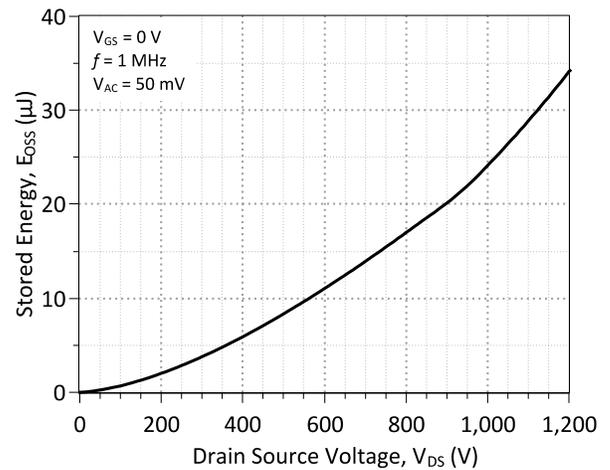
**Figure 7: Typical Transfer Characteristics**



**Figure 8: Typical Blocking Characteristics**



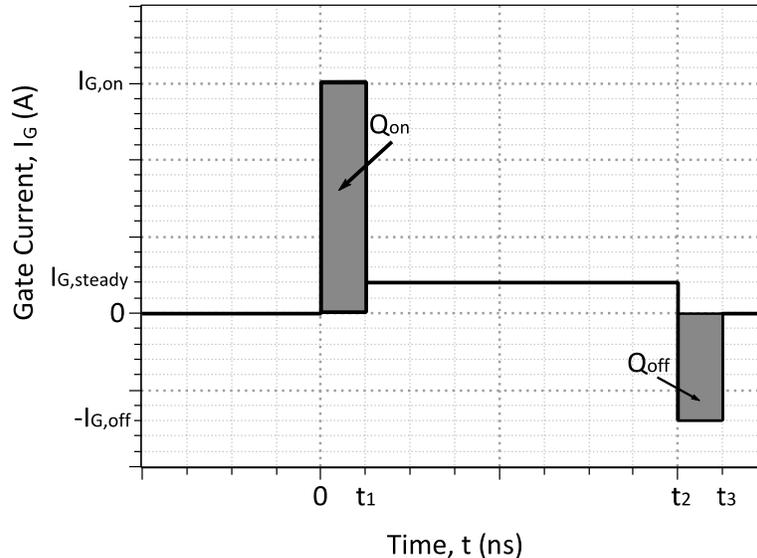
**Figure 9: Input, Output, and Reverse Transfer Capacitance**



**Figure 10: Output Capacitance Stored Energy**

## Section V: GA20JT12-CAL Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 11.



**Figure 11: Idealized Gate Current Waveform**

### A: Gate Currents, $I_{G,pk}/-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

As an example, an  $I_{G,on} \geq 3$  A is required to achieve a 25 ns  $V_{DS}$  fall time for a 800 V switching transition, due to the gate-drain charge,  $Q_{GD}$  of 77 nC for the GA20JT12-CAL. The  $I_{G,on}$  pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G,on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the TO-247 package and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the  $V_{GS,ON}$  (see Figure 7) level to counter these effects.

A high negative peak current,  $-I_{G,off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

### B: Steady On-State

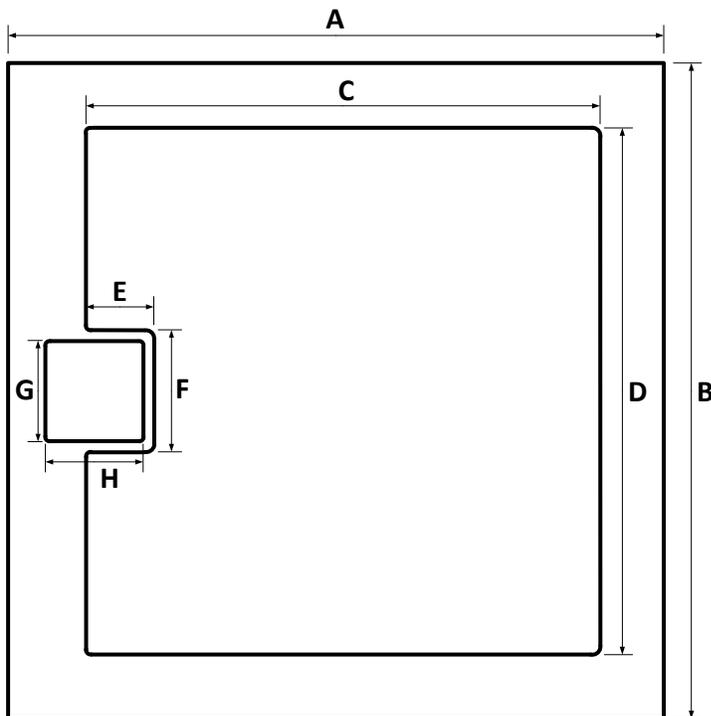
After the device is turned on,  $I_G$  may be advantageously lowered to  $I_{G,steady}$  for reducing unnecessary gate drive losses. The  $I_{G,steady}$  is determined by noting the DC current gain,  $h_{FE}$ , of the device from Figures 5 and 6.

The desired  $I_{G,steady}$  is determined by the peak device junction temperature  $T_J$  during operation, drain current  $I_D$ , DC current gain  $h_{FE}$ , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

**Section VI: Mechanical Parameters**

Raster Size	2.85 x 2.85	mm <sup>2</sup>	112 x 112	mil <sup>2</sup>
Area total / active	8.12/6.60	mm <sup>2</sup>	12544/10237	mil <sup>2</sup>
Thickness	360	μm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Passivation frontside	Polyimide			
Pad Metal (Anode)	4000 nm Al			
Backside Metal (Cathode)	400 nm Ni + 200 nm Au -system			
Die Bond	Electrically conductive glue or solder			
Wire Bond	Al ≤ 10 mil (Source) Al ≤ 3 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

**Section VII: Chip Dimensions:**


		mm	mil
<b>DIE</b>	A	2.85	112
	B	2.85	112
<b>SOURCE WIREBONDABLE</b>	C	2.23	88
	D	2.29	90
	E	0.30	12
	F	0.53	21
<b>GATE WIREBONDABLE</b>	G	0.44	17
	H	0.43	17

**Revision History**

Date	Revision	Comments	Supersedes
2014/08/25	1	Updated Electrical Characteristics	
2014/07/14	0	Initial release	

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**Section VIII: SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/products\\_sic/sjt/GA20JT12-CAL\\_SPICE.pdf](http://www.genesicsemi.com/images/products_sic/sjt/GA20JT12-CAL_SPICE.pdf)) into LTSPICE (version 4) software for simulation of the GA20JT12-CAL.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   2.0           $
*      $Date:      25-AUG-2014   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
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*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA20JT12 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.23
+ BF      78
+ BR      0.55
+ IKF     5000
+ NF      1
+ NE      2
+ RB      0.1
+ RE      0.005
+ RC      0.050
+ CJC     752.4E-12
+ VJC     3.17
+ MJC     0.480
+ CJE     3.014E-09
+ VJE     3.568
+ MJE     0.538
+ XTI     3
+ XTB     -1.5
+ TRC1    8.500E-3
+ VCEO    1200
+ ICRATING 20
+ MFG     GeneSiC_Semiconductor
*
*      End of GA20JT12 SPICE Model
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