SPC56EL60xx- differences between cut 1.0 and cut 2.0

1 Introduction

This document describes the differences between SPC56EL60xx cut2 and the predecessor cut1.

Table 1. Order codes

Order codes	Flash/SRAM	Package	Speed (MHz)	Other features
SPC564L60L3	1 MB/128 KB	LQFP100 3.3 V	80	Single core FlexRay - 40 - 105 °C
SPC56EL60L5	1 MB/128 KB	LQFP144 3.3 V	120	Dual core FlexRay - 40 - 125 °C

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2 Differences cut1 and cut2

The listed differences between the two revisions of SPC56EL60xx are related to:

- Errata fixes
- Feature enhancements
- ID codes
- Pin muxing

2.1 Errata fixes

Table 2 shows the currently known errata for cut1 and the planned fixes for cut2.

Please refer to SPC56EL60L5 - SPC56EL60C3 errata sheet, rev. 2 (see *Appendix A: Reference document*).

Table 2. Errata for cut1 and the fixes for cut2

Errata number	Module	Description
e5299PS	NEXUS	Critical signals of Nexus debugger not monitored by FCCU.
e5302PS	JTAG	Critical signals of JTAG not monitored by FCCU.
e5681PS	NEXUS	Nexus interface availability is indicated too early.
e6842PS	DPM	CPU core 1 in unknown state after HALT0 or STOP0 mode exit when device configured in DPM.
e7292PS	XOSC	External oscillator is not controllable.
e7811PS	ADC1	Enabling of conversions of shared channels using ADC1.
e8521PS	CTU	CTU: Invalid Command Error is not detected in case of dual conversion mode on shared ADC channels.
e8826PS	PMU	Destructive reset triggered during a mode transition from run mode to safe/halt/stop mode.
e5932PS	FLASH	RWW errors not correctly flagged at high system frequencies.
e6934IPG	DSPI	DSPI: changing CTARs between frames in continuous PCS mode causes error.
e10483IPG	DSPI	DSPI: PCS Continuous Selection Format limitation.
e18427IPG	DSPI	DSPI: DSPI Microsecond Bus Limitations.
e8814PS	ADC	ADC parameters on negative current injection out of specification.
e7764PS	NEXUS	Nexus stall feature not supported in lockstep mode.
e5455PS	BAM	BAM: BookE mode not supported for serial downloads.
e6020PS	BAM	BAM: autobaud feature is not available.
e3771PS	RGM	MC_RGM: FCCU_SOFT is incorrectly configurable to generate a 'long' reset sequence.
e4107PS	ME	MC_CGM and MC_PCU: a data storage exception is not generated on an access to MC_CGM or MC_PCU when the respective peripheral is disabled at MC_ME.

Table 2. Errata for cut1 and the fixes for cut2 (continued)

Errata number	Module	Description
e5301PS	RGM	MC_RGM: SAFE mode exit may be possible even though condition causing the SAFE mode request has not been cleared.
e6041PS	ME	MC_ME: peripherals in unknown state after SAFE mode exit.
e6440PS	MC	SWT interrupt does not cause STOP0 mode exit.
e6699PS	CGM	MC_CGM: short glitch may occur on output clock.
e7583 PS	RGM	MC_RGM: RGM_FES content incorrect after startup LBIST execution.
e8291PS	CGM	System clock source change may cause a "CMU0 system clock frequency too high or too low event".
e9367PS	eTimer	eTimer: configuring an eTimer counter channel in GATED-COUNT mode or in SIGNED-COUNT mode it may cause a possible incorrect counting of 1 tick.
e9414PS	eTimer	Possible false DMA requests from eTimer.
e6886PS	NPC	MCKO clock gating not implemented.
e9376 PS	PWM	FlexPWM: configuring the count value to set PWMA/PWMB first low and then high in the same cycle the output signals are low.
e6309PS	SSCM	Debugging functionality could be lost when unsecuring a secured device.
e6500PS	ADC	VREFP and VDD_HV_ADC power up sequencing constraint.
e5485PS	ADC	ADC: ADC_DMAE[DCLR] should not be used.
e9154 PS	ADC	ADC: abort request during last sampling cycle corrupts the data register of next channel conversion.
e1685PS	FMPLL	FMPLL: FMPLL_CR[UNLOCK_ONCE] wrongly set.
e7220PS	SWG	SWG: SGEN_CTRL.NRO bit is reserved *).
e5816PS	SWG	SWG: Sinewave generator (SWG) is active during self-test execution.
e26553IPG	e200z4	e200z4: mtlr followed by se_rfi/se_rfci/se_rfdi/se_rfmci can give unexpected results.
e8099 PS	DMA	Limiations for DMA access to LINFlex.
e9471 PS	IPBUS	CAN Register/Message Buffer Access can reset or block the device if certain clock divider ratios (PeriN: System Clock) are selected.
e7752PS	Platform	ICache commands ICBTLS and ICBLC do not work as specified.

2.2 Feature enhancements

The list below shows feature enhancements for cut2.

- Nexus - NXSS
- Nexus - RDY PIN
- Nexus – DDR mode – I/O timing
- DSPI enhanced version
- CRC Unit - support for additional polynominal
- AIPS MPROT - enhanced protection features
- MC_RGM - destructive reset can be triggered by software
- SSCM - easier access to NVM calibration data
- Selftest - reduction of execution time

2.2.1 Nexus - NXSS

The Nexus Crossbar Slave Port Data Trace Module for System SRAM allows to trace all DMA/SRAM accesses.

2.2.2 Nexus - RDY PIN

To increase the transfer rate of the IEEE 1149.1 port, an additional pin has been implemented to signal when data are ready to be transferred to and from NRRs. This may eliminate the need to poll NRRs for status information for synchronization purposes. This capability becomes especially important when performing read/write access transfers to different speed target memories.

This functionality is only available on BGA257 package (ball K3). RDY is muxed with GPIO (GPIO is default out of reset).

2.2.3 Nexus - DDR mode – I/O timing

The I/O timing has been changed so that the MDO / MSEO outputs are valid during the MCKO rising and falling edges.

2.2.4 DSPI - enhanced version

Support higher net through put in slave mode by reducing required dead cycles in back to back operation.

2.2.5 CRC Unit - support for additional polynominal

An additional 8-bit CRC polynomial has been implemented. The bit field 28:29 of the register CRC_CFG for each context selects the polynomial preserving compatibility with previous versions of this IP used on cut1.

2.2.6 AIPS MPROT - enhanced protection features

The default reset MPROT (Master Protection) configuration for each AIPS bridge is determined via the aips_rstcfg vector which has been changed.

In general in both modes of operation only the two cores (Instruction Port, Load/Store Port and the Nexus subsystem) have access rights to the IPS peripherals per default configuration.

2.2.7 MC_RGM - destructive reset can be triggered by software

Additional support for software triggerable destructive reset event (D[14]) has been implemented.

2.2.8 SSCM - easier access to NVM calibration data

The selftest execution time has been reduced compared to cut1 by appr. 13 ms. The information is documented in the SPC56EL60L3, SPC56EL60L5 datasheet (see *Appendix A: Reference document*) as part of the reset sequence specification.

2.3 Device ID codes

SPC56EL60xx contains ID codes which identify the device.

- JTAG ID
  Cut1: 0000_1010_1110_1010__0010_0000_0100_0001
  Cut2: 0000_1010_1110_1010__0011_0000_0100_0001
- MCU ID Register 1 (MIDR1)
- MCU ID Register 2 (MIDR2)

The values of these ID codes differ between cut1 and cut2.

2.4 Pin muxing

SPC56EL60xx cut2 is pin-compatible with cut1. Cut2 specifies an additional RDY pin for the BGA257 package (ball K3). On cut1 this ball is not connected to any function. The RDY pin on cut2 is muxed with GPIO (GPIO is default out of reset).

Appendix A Reference document

1. 32-bit Power Architecture™ microcontroller for automotive SIL3/ASILD chassis and safety applications (SPC56EL60L5 - SPC56EL60C3 errata sheet - Doc ID 16945).
2. 32-bit Power Architecture® microcontroller for automotive SIL3/ASILD chassis and safety applications (SPC56EL60L5 - SPC56EL60C3 datasheet - Doc ID 15457).

Revision history

Table 3. Document revision history

Date	Revision	Changes
03-Jan-2011	1	Initial release.
18-Sep-2013	2	Updated Disclaimer.