

Document No.	853-1494
ECN No.	00731
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

# 74AC/ACT11194

## 4-bit bidirectional universal shift register

### FEATURES

- Shift left and shift right capability
- Synchronous Parallel and Serial data transfers
- Easily expanded for both Serial and Parallel operation
- Asynchronous reset
- Output capability:  $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- $50\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11194 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11194 4-bit Bidirectional Universal Shift Register is fully synchronous, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

(continued)

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay CP to $Q_n$ ( $\overline{\text{MR}} = \text{High}$ )	$C_L = 50\text{pF}$	4.2	6.2	ns
$C_{PD}$	Power dissipation capacitance <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	66	69	pF
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	4.0	4.0	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50\text{pF}$	130	130	MHz

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

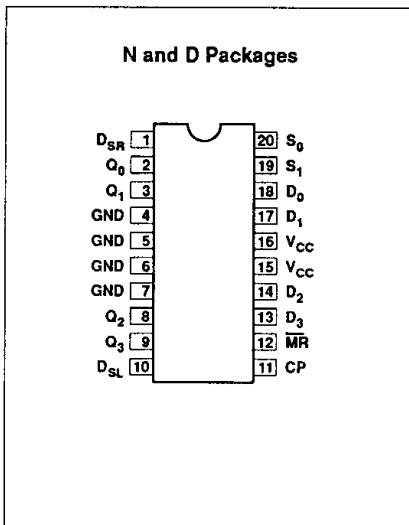
$f_o$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

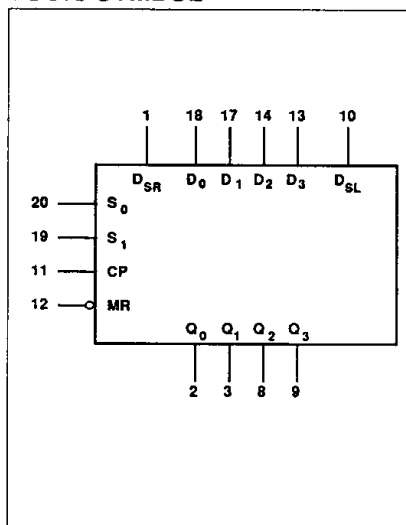
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11194N 74ACT11194N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11194D 74ACT11194D

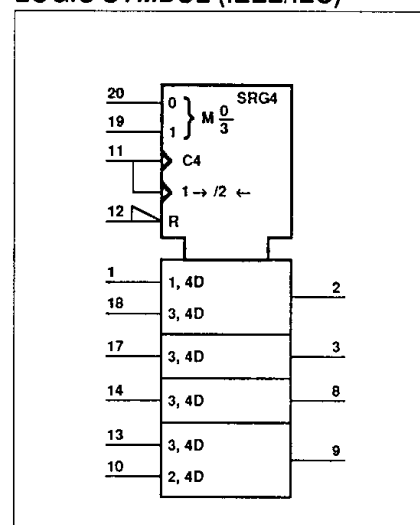
### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# 4-bit bidirectional universal shift register

# 74AC/ACT11194

The 74AC/ACT11194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs,  $S_0$  and  $S_1$ . As shown in the Function Table, data can be entered and shifted from left to right (shift right,  $Q_0 \text{ } \overline{A} \text{ } Q_1$ , etc.), or right to left (shift left,  $Q_3 \text{ } \overline{A} \text{ } Q_2$ , etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both  $S_0$  and  $S_1$  are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Se-

rial Data input ( $D_{SR}$ ,  $D_{SL}$ ) to allow multi-stage shift right or shift left data transfers without interfering with parallel load operation.

The only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select ( $S_0$ ,  $S_1$ ), Parallel Data ( $D_0 - D_3$ ) and Serial Data ( $D_{SR}$ ,  $D_{SL}$ ) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with

respect to the clock rising edge are observed.

The four Parallel Data inputs ( $D_0 - D_3$ ) are D-type inputs. Data appearing on  $D_0 - D_3$  inputs when  $S_0$  and  $S_1$  are High is transferred to the  $Q_0 - Q_3$  outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ( $\overline{MR}$ ) overrides all other input conditions and forces the Q outputs Low.

### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{MR}$	Asynchronous master reset (active Low)
11	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	$D_0 - D_3$	Data inputs
1	$D_{SR}$	Serial data input (shift right)
10	$D_{SL}$	Serial data input (shift left)
20, 19	$S_0, S_1$	Mode control inputs
2, 3, 8, 9	$Q_0 - Q_3$	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	$V_{CC}$	Positive supply voltage

### FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	$S_1$	$S_0$	$D_{SR}$	$D_{SL}$	$D_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	$\uparrow$	H	h	l	X	l	X	$q_1$	$q_2$	$q_3$	L
	$\uparrow$	H	h	l	X	h	X	$q_1$	$q_2$	$q_3$	H
Shift Right	$\uparrow$	H	l	h	l	X	X	L	$q_0$	$q_1$	$q_2$
	$\uparrow$	H	l	h	h	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	$\uparrow$	H	h	h	X	X	$d_n$	$d_0$	$d_1$	$d_2$	$d_3$

H = High voltage level

L = Low voltage level

h = High voltage level one setup time prior to the Low-to High clock transition

l = Low voltage level one setup time prior to the Low-to High clock transition

X = Don't care

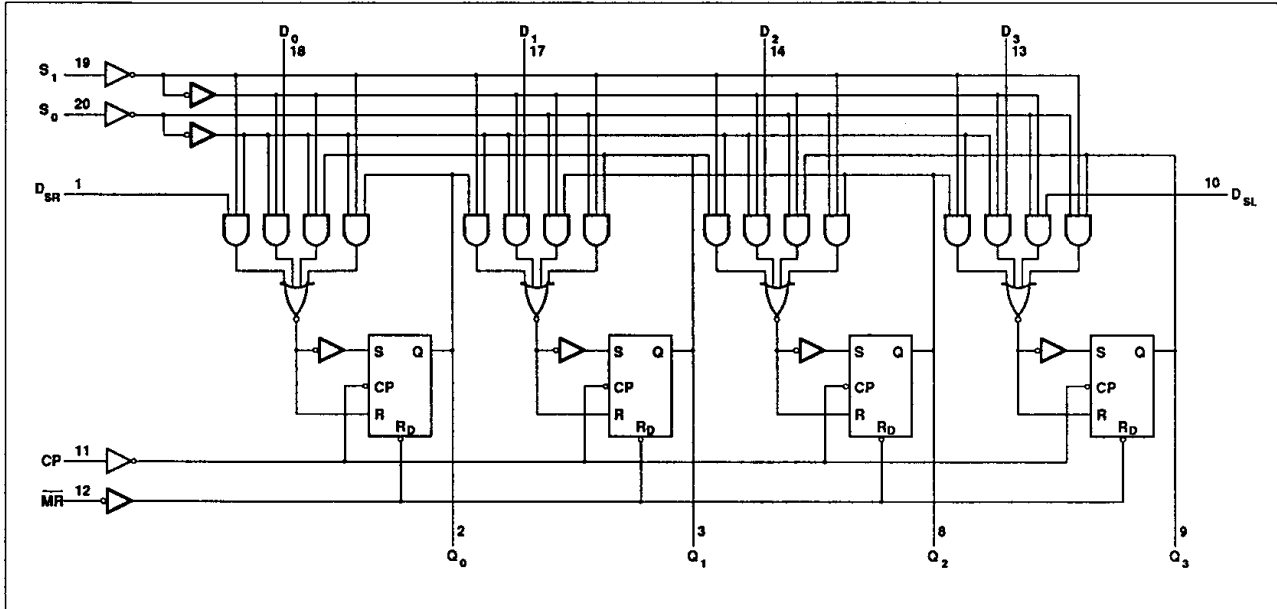
$d_n$  ( $q_n$ ) = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition

$\uparrow$  = Low-to-High clock transition

# 4-bit bidirectional universal shift register

74AC/ACT1194

## LOGIC DIAGRAM



## 4-bit bidirectional universal shift register

## 74AC/ACT11194

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11194			74ACT11194			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_i$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_o$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

## NOTE:

1. No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_i$	DC input diode current <sup>2</sup>	$V_i < 0$	-20	mA
		$V_i > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_o$	DC output diode current <sup>2</sup>	$V_o < 0$	-50	mA
		$V_o > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_o$	DC output source or sink current per output pin	$V_o = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		$\pm 100$	mA
	DC ground current		$\pm 100$	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

## NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 4-bit bidirectional universal shift register

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11194				74ACT11194				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I <sub>OH</sub> = -75mA <sup>1</sup>	3.0			3.85				3.85					
	5.5												
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	3.0				1.65				1.65				
	5.5												
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

## 4-bit bidirectional universal shift register

## 74AC/ACT11194

AC ELECTRICAL CHARACTERISTICS AT 3.3V  $\pm 0.3V$ 

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	90	120		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	1.0 1.0	5.8 6.6	8.4 8.9	1.0 1.0	9.5 10.2	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	1.7	7.1	9.5	1.7	10.7	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	3	4.0			4.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub>	3	0.5			0.5		ns
t <sub>S</sub>	Setup time, High or Low S <sub>n</sub> to CP	3	5.0			5.0		ns
t <sub>H</sub>	Hold time, High or Low CP to S <sub>n</sub>	3	1.5			1.5		ns
t <sub>W</sub>	Clock pulse width (load) High or Low	1	5.5			5.5		ns
t <sub>W</sub>	Clock pulse width (count) High or Low	1	5.5			5.5		ns
t <sub>W</sub>	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V  $\pm 0.5V$ 

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	100	130		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	0.8 1.1	3.9 4.4	6.2 6.6	0.8 1.1	6.8 7.7	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	1.5	4.6	7.0	1.5	7.8	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	3	2.5			2.5		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub>	3	1.0			1.0		ns
t <sub>S</sub>	Setup time, High or Low S <sub>n</sub> to CP	3	4.0			4.0		ns
t <sub>H</sub>	Hold time, High or Low CP to S <sub>n</sub>	3	1.5			1.5		ns
t <sub>W</sub>	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t <sub>W</sub>	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t <sub>W</sub>	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

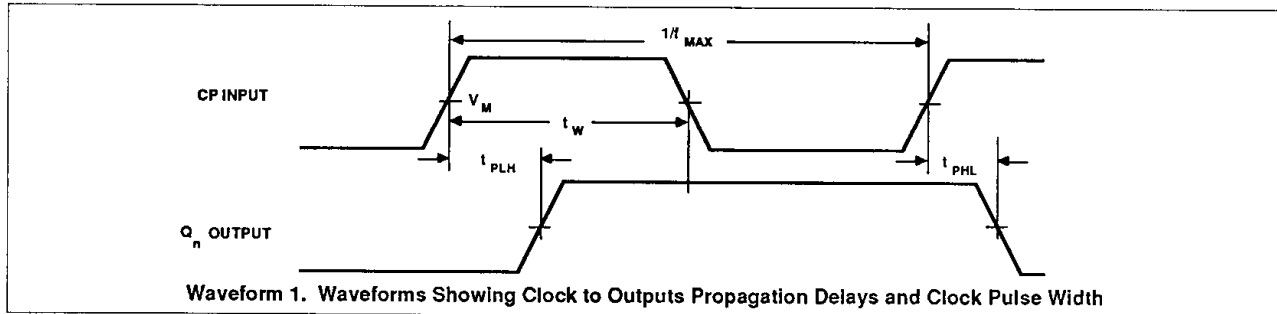
# 4-bit bidirectional universal shift register

# 74AC/ACT11194

## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11194					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	100	130		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	2.2 2.6	5.8 6.6	6.9 7.7	2.2 2.6	7.7 8.8	ns
t <sub>PHL</sub>	Propagation delay MR to Q <sub>n</sub>	2	2.9	7.1	9.1	2.9	10.3	ns
t <sub>S</sub>	Setup time, High or Low D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	3	4.0			4.0		ns
t <sub>H</sub>	Hold time, High or Low CP to D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub>	3	1.0			1.0		ns
t <sub>S</sub>	Setup time, High or Low S <sub>n</sub> to CP	3	6.0			6.0		ns
t <sub>H</sub>	Hold time, High or Low CP to S <sub>n</sub>	3	1.5			1.5		ns
t <sub>W</sub>	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t <sub>W</sub>	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t <sub>W</sub>	MR pulse width, Low	2	4.5			4.5		ns
t <sub>REC</sub>	Recovery time MR to CP	2	1.0			1.0		ns

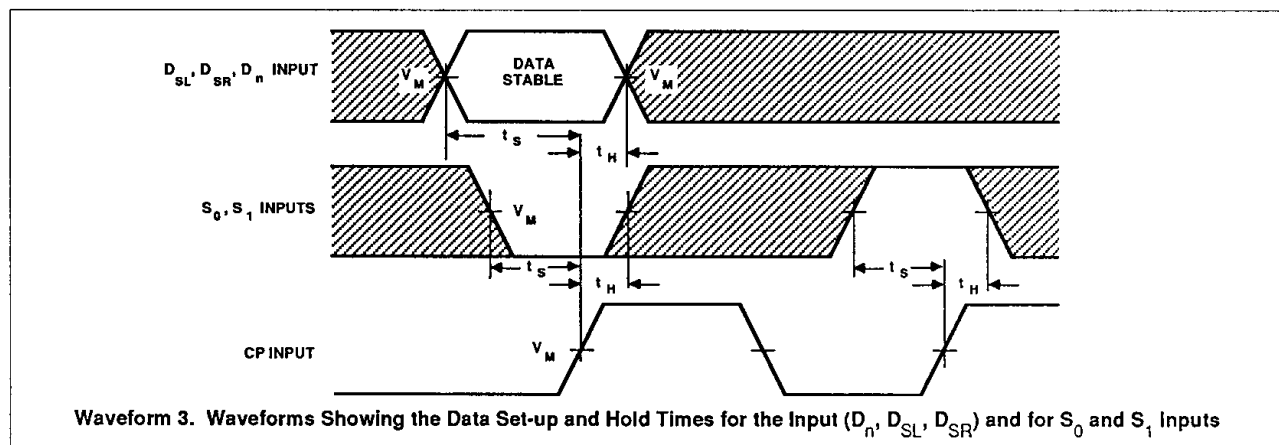
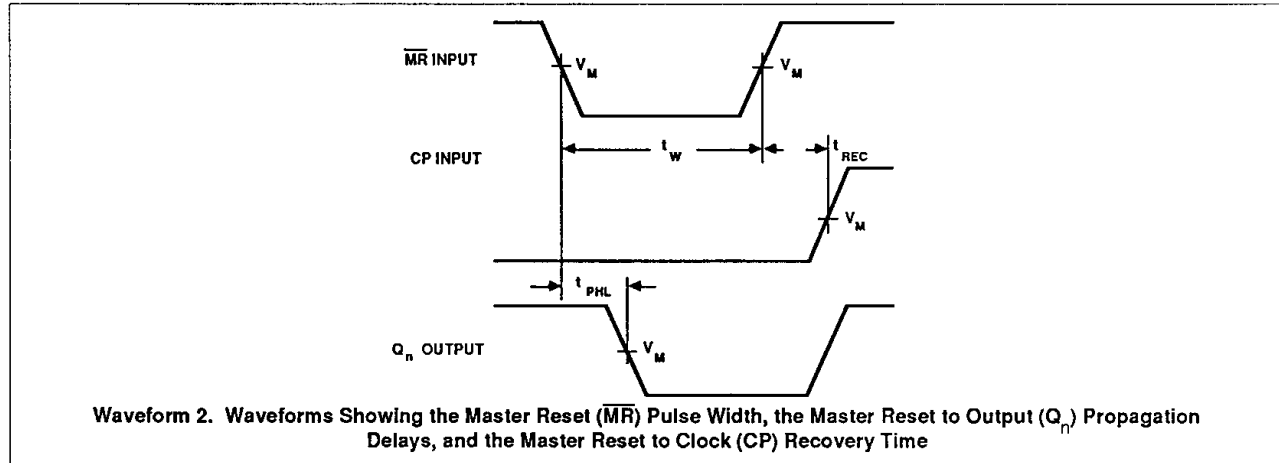
## AC WAVEFORMS



# 4-bit bidirectional universal shift register

# 74AC/ACT11194

## AC WAVEFORMS (Continued)



## WAVEFORM CONDITIONS

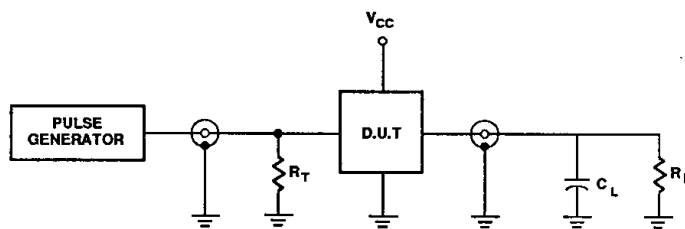
	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC},$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V,$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$



**4-bit bidirectional universal shift register**

**74AC/ACT11194**

**TEST CIRCUIT**



**Test Circuit**

**DEFINITIONS**

$C_L$  = Load capacitance, 50pF; includes jig and probe capacitance

$R_L$  = Load resistor, 500Ω

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$