1M x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

MAY 2009

FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - 30 mW (typical) operating
  - 12 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V V_{DD} (62/65WV10248DALL)
  - 2.4V--3.6V V_{DD} (62/65WV10248DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Automotive temperature (-40°C to +125°C)
- Lead-free available

DESCRIPTION

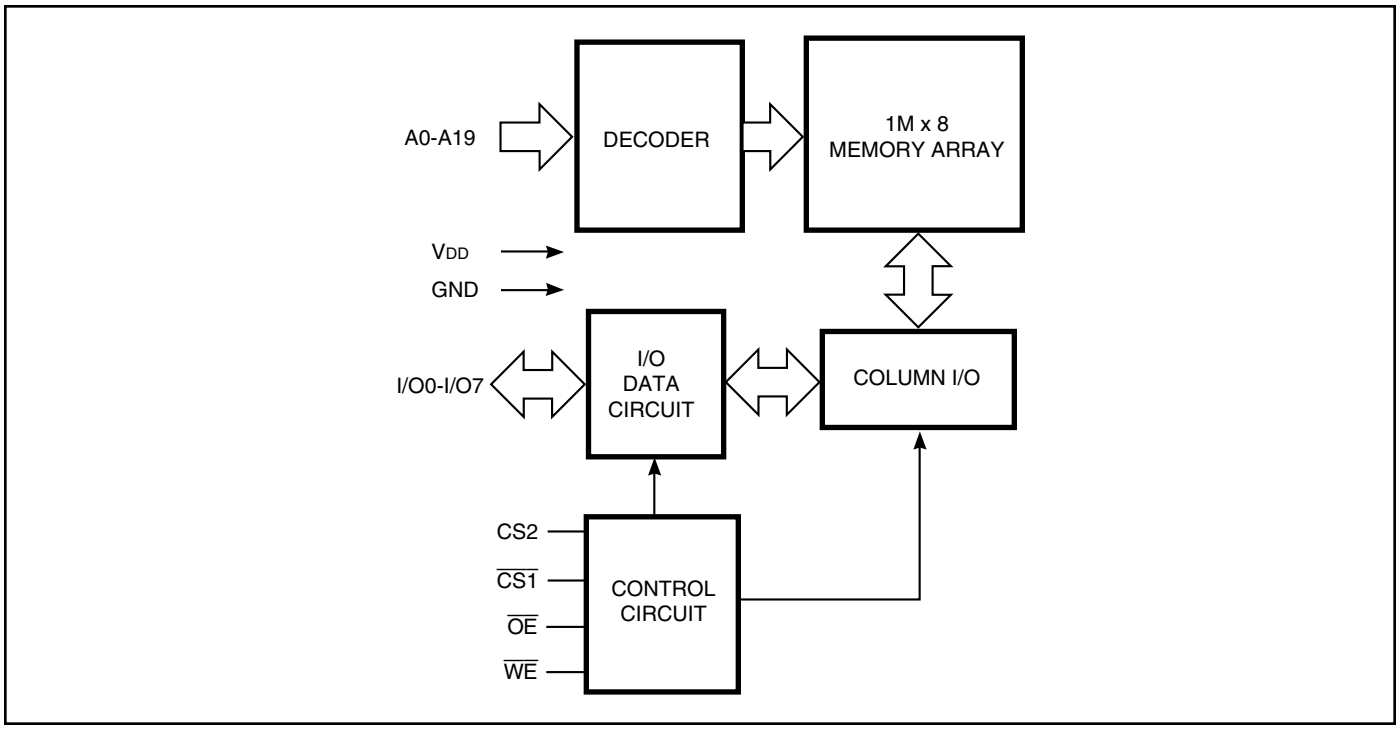
The *ISSI* IS62WV10248DALL/ IS62WV10248DBLL are high-speed, 8M bit static RAMs organized as 1M words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

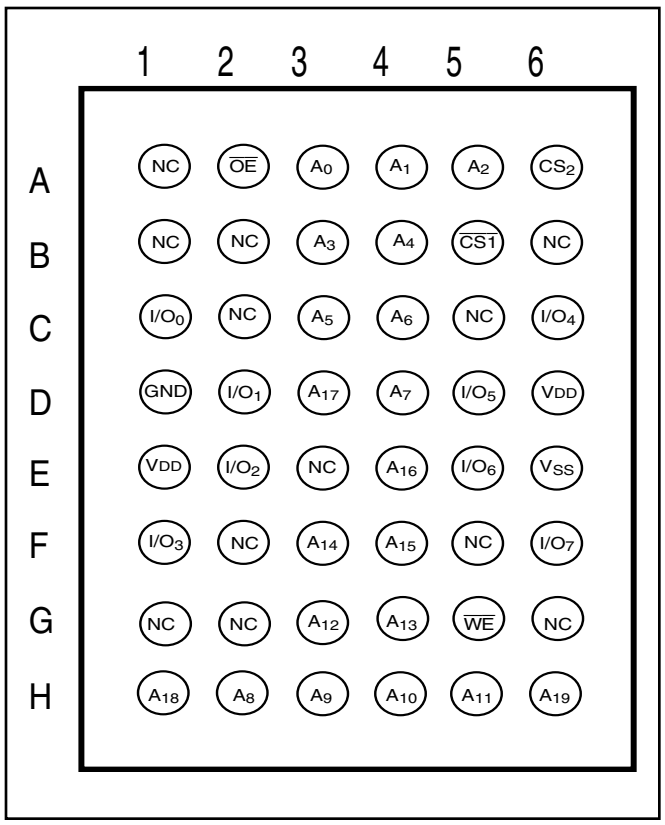
The IS62WV10248DALL and IS62WV10248DBLL are packaged in the JEDEC standard 48-pin mini BGA (9mm x 11mm) and 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM

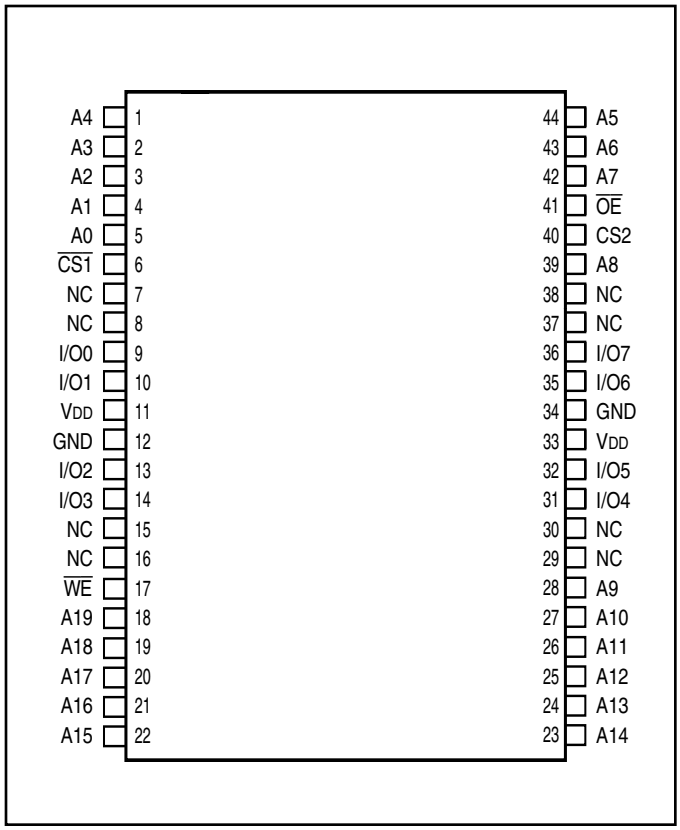


PIN CONFIGURATION (1M x 8 Low Power)

48-pin mini BGA (B) (9mm x 11mm)



44-pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	1.65V - 2.2V	2.4V - 3.6V
Commercial	0°C to +70°C	IS62WV10248DALL (55ns)	IS62WV10248DBLL (55ns)*
Industrial	–40°C to +85°C	IS62WV10248DALL (55ns)	IS62WV10248DBLL (55ns)*
Automotive	–40°C to +125°C	IS65WV10248DALL (70ns)	IS65WV10248DBLL (55ns)

*When operated in the range for 3.3V ± 5% or when operated in the temperature range of 0°C to 70°C, the device meets 45ns.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.0V.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +125	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.4-3.6V	1.8	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 1 mA	2.4-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
			2.4-3.6V	2.0	V_{DD} + 0.3	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
			2.4-3.6V	–0.2	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% tested.

AC TEST CONDITIONS

Parameter	62WV10248DALL (Unit)	62WV10248DBLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	62W10248DALL (1.65V - 2.2V)	62WV10248DBLL (2.4V - 3.6V)
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	3.0V

AC TEST LOADS

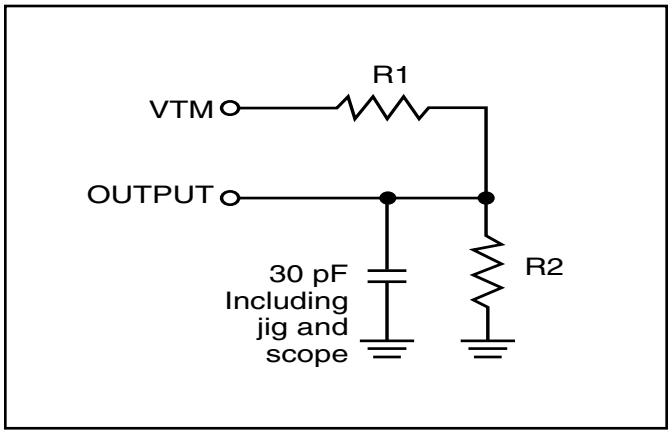


Figure 1

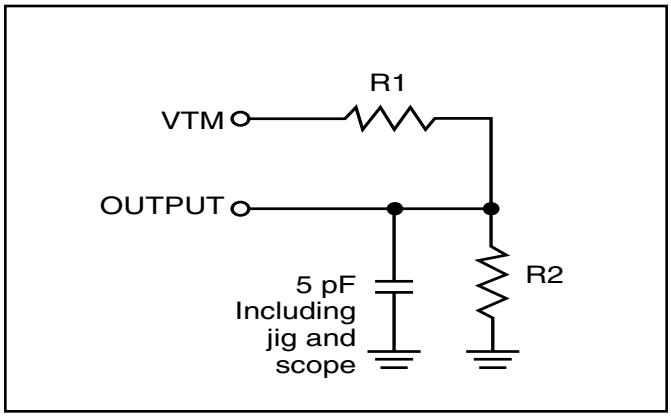


Figure 2

1.65V-2.2V, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	20	20	mA
			Ind.	25	25	
			Auto.	–	35	
			typ.[1]	10		
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V	Com.	4	4	mA
		$\overline{WE}$ = V_{DD} – 0.2V	Ind.	4	4	
		CS2 = V_{DD} – 0.2V, f = 1MHZ	AUTO.	–	4	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	20	20	µA
		$\overline{CS1} \geq V_{DD}$ – 0.2V,	Ind.	40	40	
		CS2 ≤ 0.2V,	Auto.	–	90	
		$V_{IN} \geq V_{DD}$ – 0.2V, or	typ.[1]	4		
		$V_{IN} \leq$ 0.2V, f = 0				

Note:.

1. Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

2.4V-3.6V, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 45	Max. 55	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	20	17	mA
			Ind.	25	22	
			Auto.	–	35	
			typ.[2]	10		
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V	Com.	5	5	mA
		$\overline{WE}$ = V_{DD} – 0.2V	Ind.	5	5	
		CS2 = V_{DD} – 0.2V, f = 1MHZ	Auto.	–	5	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	20	20	µA
		$\overline{CS1} \geq V_{DD}$ – 0.2V,	Ind.	40	40	
		CS2 ≤ 0.2V,	Auto.	–	110	
		$V_{IN} \geq V_{DD}$ – 0.2V, or	typ. [2]	4		
		$V_{IN} \leq$ 0.2V, f = 0				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

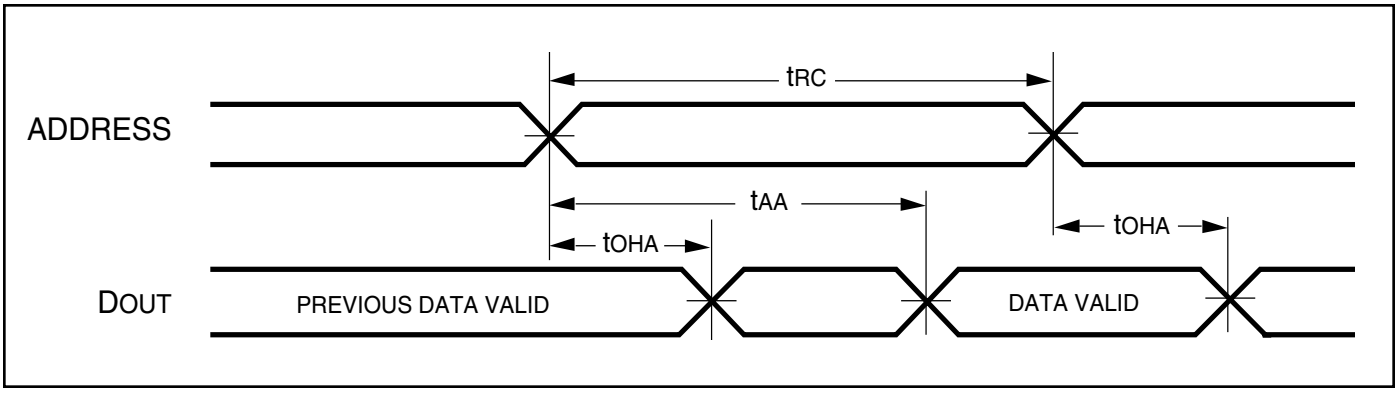
Symbol	Parameter	45 ns Min.	45 ns Max.	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	45	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	15	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	15	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

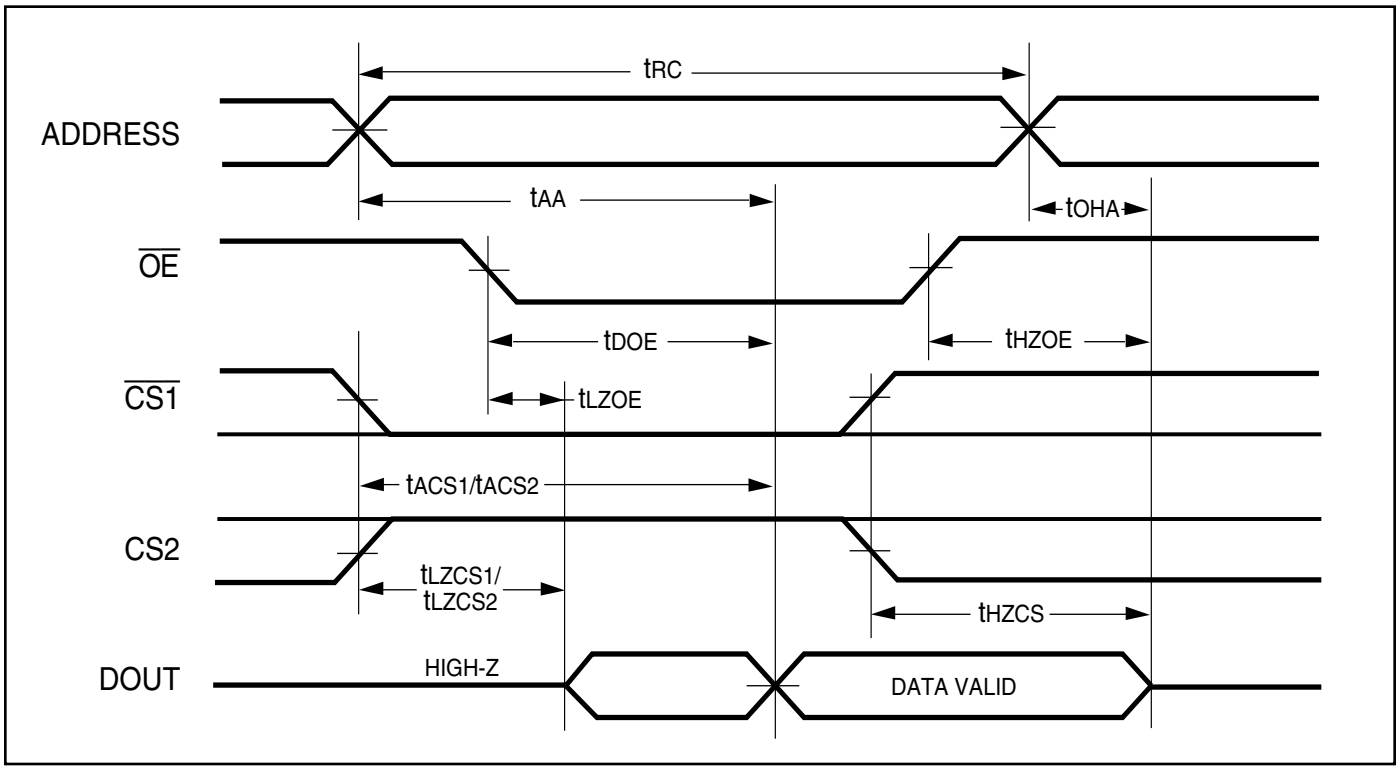
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$= V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

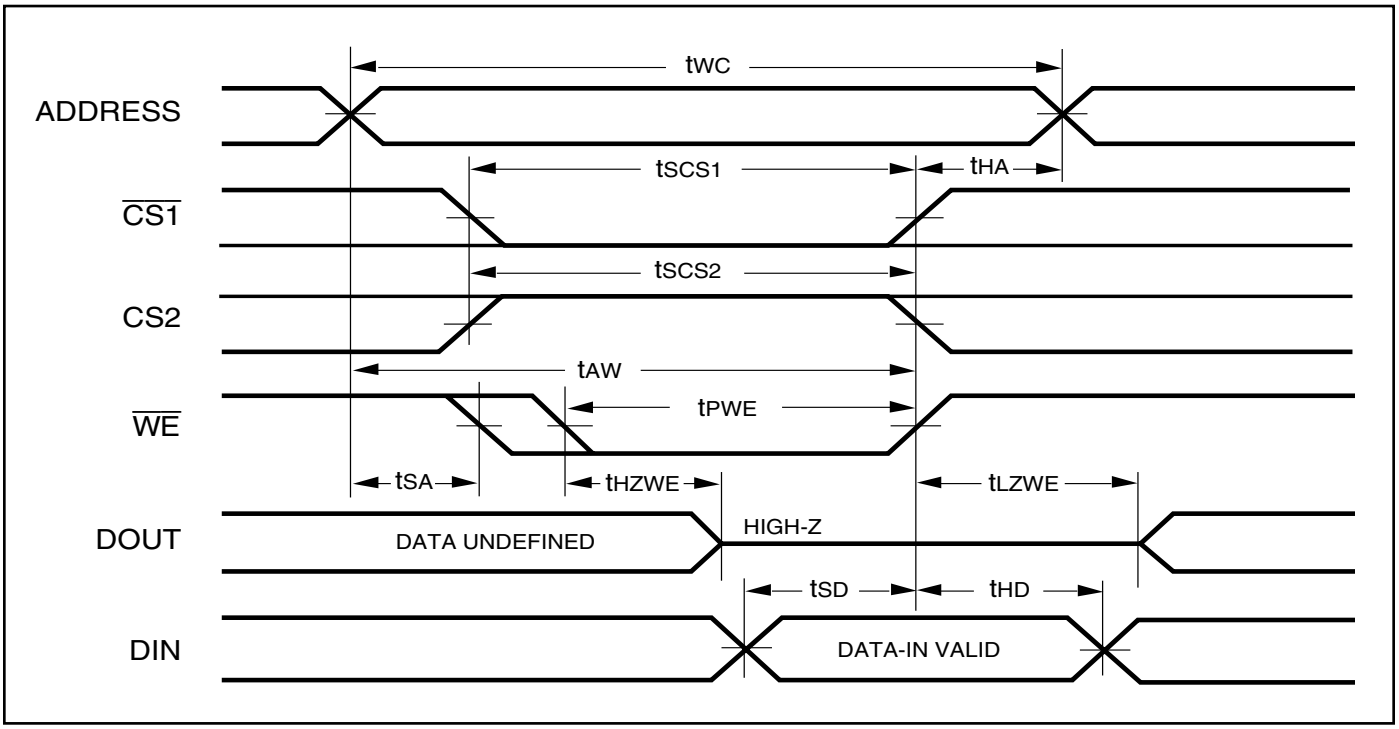
Symbol	Parameter	45ns Min.	45ns Max.	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	35	—	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	35	—	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
t_{SD}	Data Setup to Write End	20	—	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	30	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

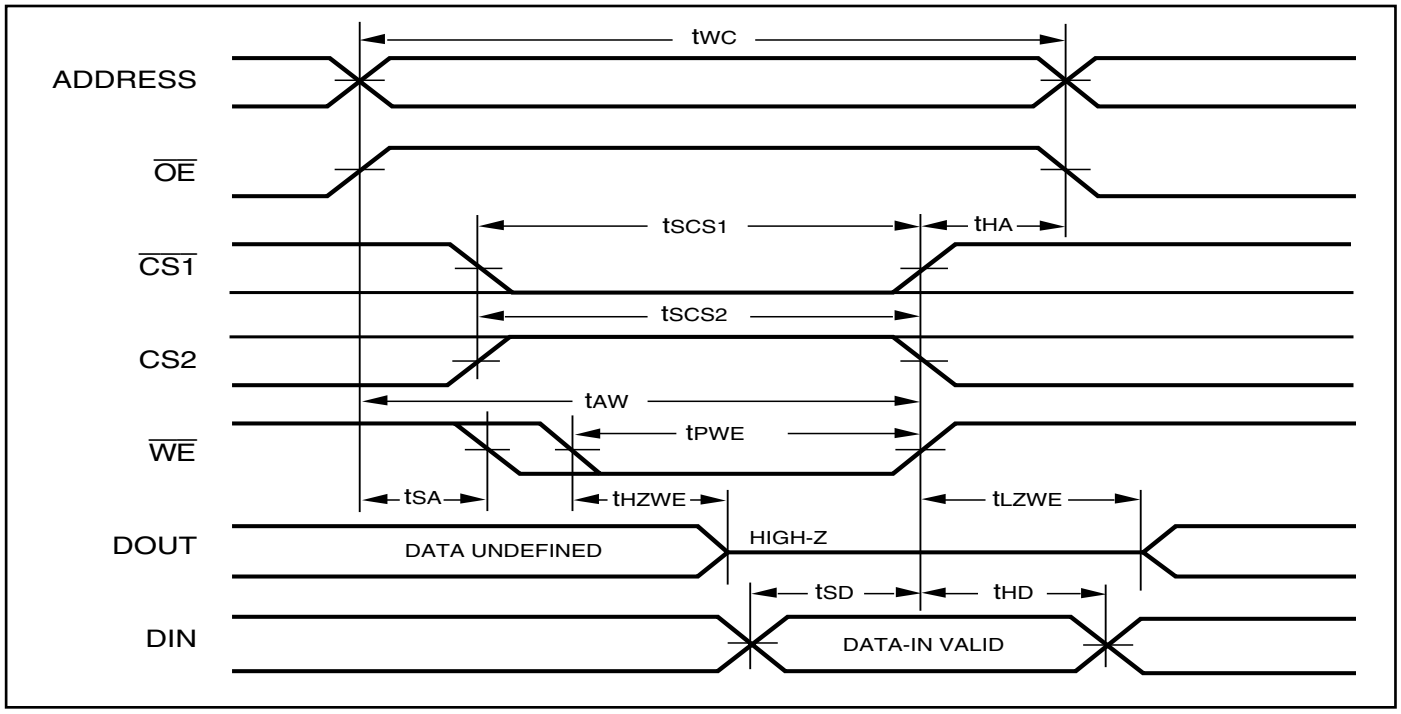
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

AC WAVEFORMS

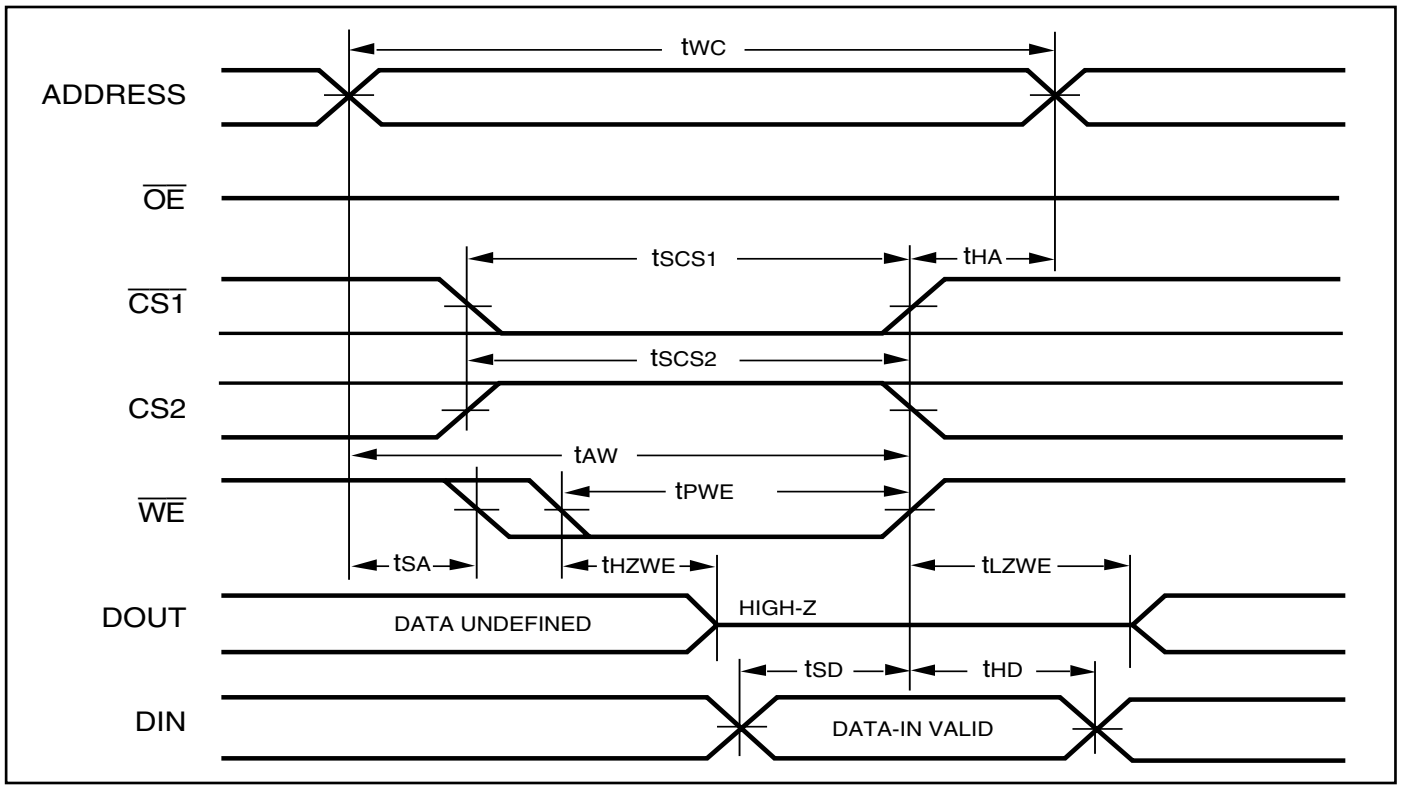
WRITE CYCLE NO. 1 ($\overline{CS1}$/CS2 Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

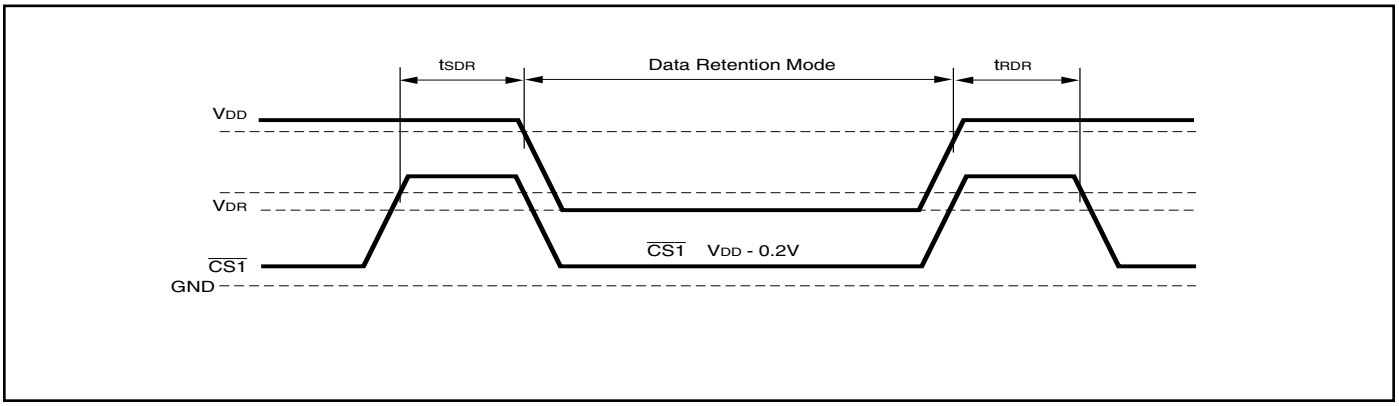


DATA RETENTION SWITCHING CHARACTERISTICS (1.65V - 3.6V)

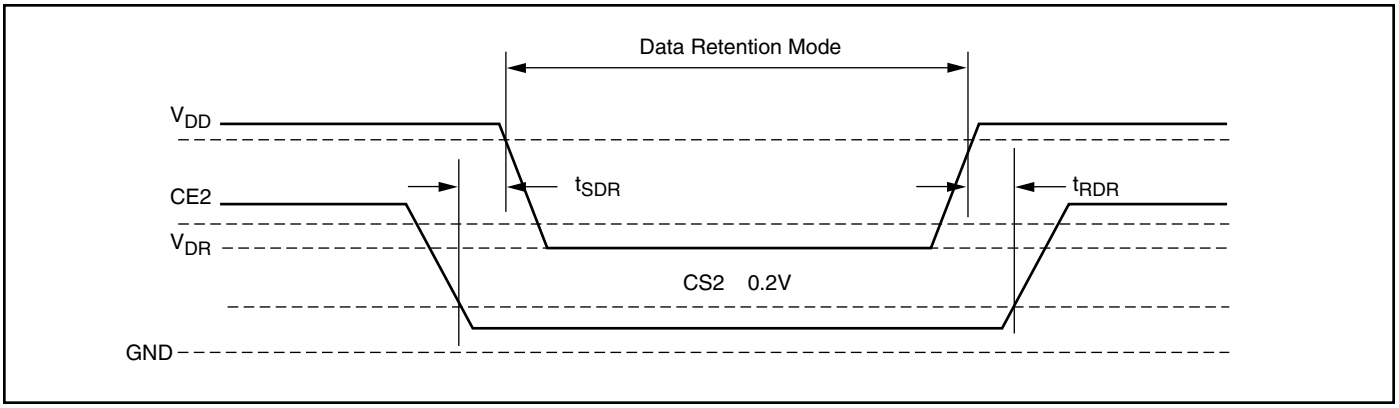
Symbol	Parameter	Test Condition		Min.	Typ.*	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.4		3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.4V, $\overline{CS1} \geq V_{DD} - 0.2V$	Com.	—	4	20	µA
			Ind.	—		40	
			Auto.	—		95	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

* Typical Values are measured at VDD = 3V, TA = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION

IS62WV10248DALL (1.65V - 2.2V)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV10248DALL-55TI	TSOP-II
	IS62WV10248DALL-55TLI	TSOP-II, Lead-free
	IS62WV10248DALL-55MI	mini BGA (9mmx11mm)
	IS62WV10248DALL-55MLI	mini BGA (9mmx11mm), Lead-free

IS62WV10248DBLL (2.4V - 3.6V)
Industrial Range: –40°C to +85°C

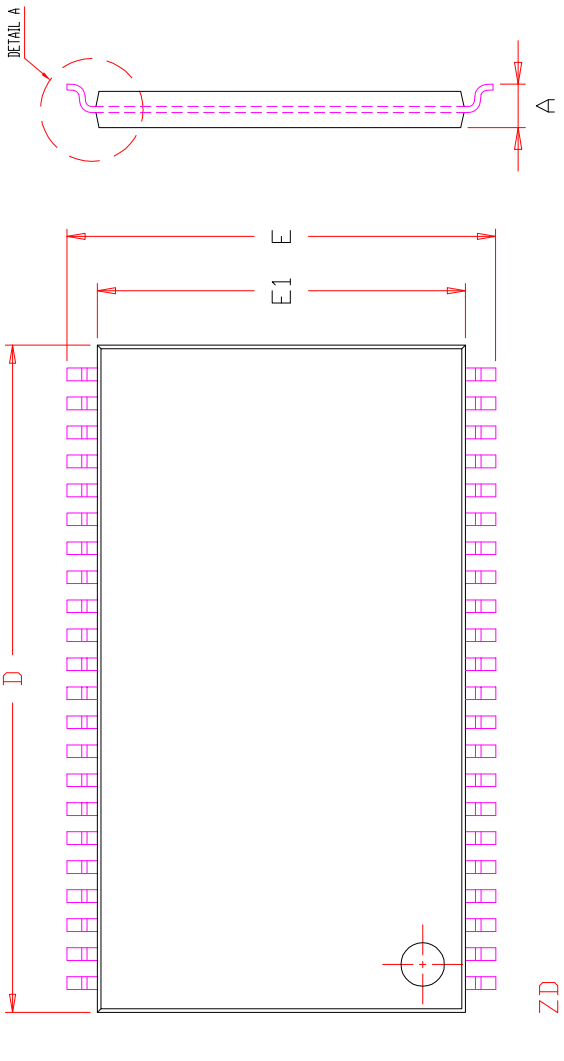
Speed (ns)	Order Part No.	Package
55*	IS62WV10248DBLL-55TI	TSOP-II
	IS62WV10248DBLL-55TLI	TSOP-II, Lead-free
	IS62WV10248DBLL-55MI	mini BGA (9mmx11mm)
	IS62WV10248DBLL-55MLI	mini BGA (9mmx11mm), Lead-free

*When operated in the range for 3.3V ± 5% or when operated in the temperature range of 0°C to 70°C, the device meets 45ns.

IS65WV10248DBLL (2.4V - 3.6V)
Industrial Range: –40°C to +125°C

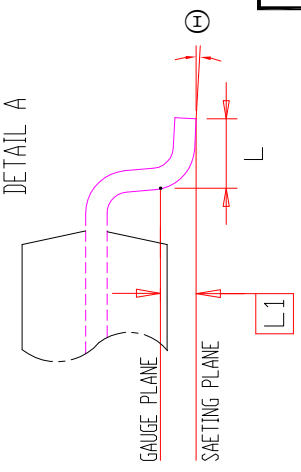
Speed (ns)	Order Part No.	Package
55	IS65WV10248DBLL-55CTLA3	TSOP-II, Lead-free, Copper Lead-frame

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
θ	0°	—	8°	0°	—	8°



NOTE:

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

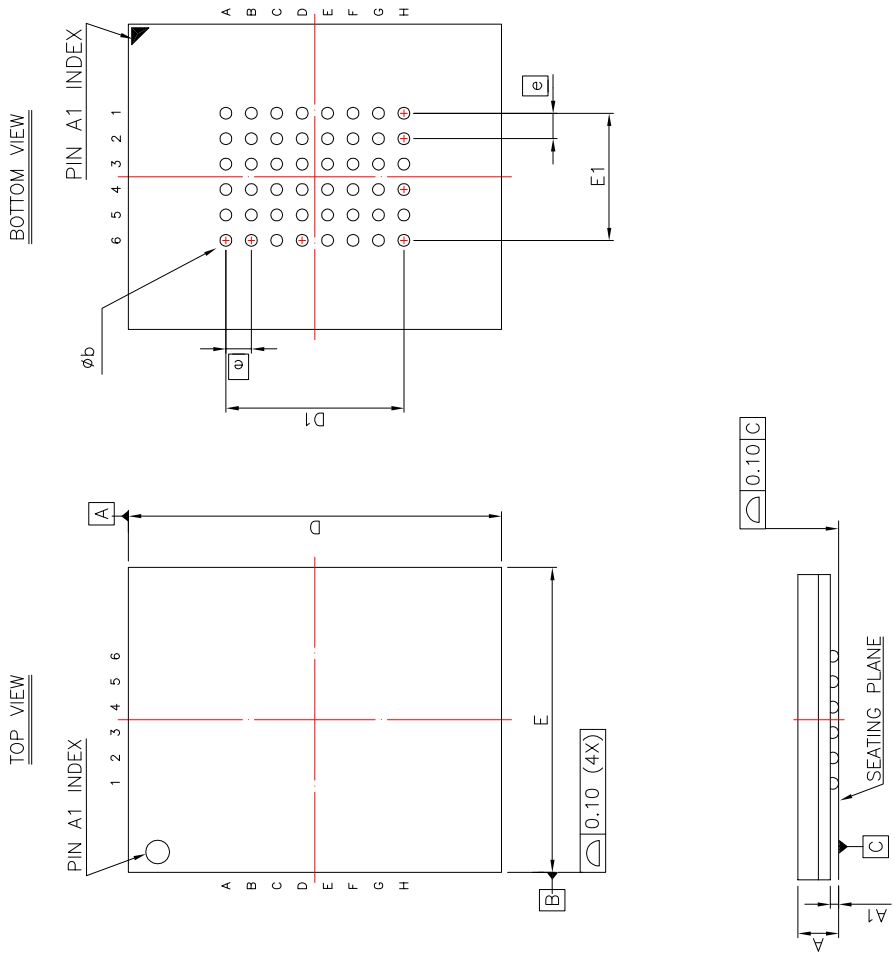


	TITLE	REV.	DATE
ISSI	44L 400mil TSOP-2 Package Outline	F	06/04/2008

SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



ISSI	TITLE	REV.	DATE
	48L 9x11mm TF-BGA Package Outline	B	08/21/2008