AP2303

DDR BUS TERMINATION REGULATOR

Description

The AP2303 is a low dropout linear regulator to generate termination voltage of DDR-SDRAM system. The regulator can source or sink up to 1.75A current continuously. The output voltage is regulated to track tightly with the reference voltage ($1/2V_{DDQ}$) within ±10mV.

The AP2303 supports soft start-up when used to turn on the VCNTL and VREFEN. It integrates a shutdown circuit that will be triggered once the voltage of VIN, VCNTL or VREFEN falls below a certain value.

AP2303 features over temperature protection and current limit protection for both source and sink.

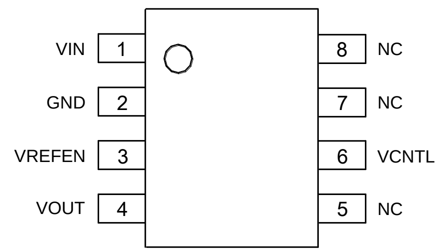
AP2303 is available in packages of SOIC-8 and PSOP-8.

Features

- Support DDR-II (V_{TT}=0.9V), DDR-III (V_{TT}=0.75V), DDR-IIIL (V_{TT}=0.675V), DDR-IV (V_{TT}=0.6V) Application
- Source and Sink up to 1.75A Current
- Output Voltage Accuracy Over Full Load: ±2% (Max.)
- Soft Start-up and Shutdown along with V_{IN}, V_{CNTL} and V_{REFEN} Rising and Shutdown along with V_{IN}, V_{CNTL} and V_{REFEN} Dropping
- Flexible Output by 2 External Resistors
- Requires Minimum 10µF Output Ceramic Capacitor for Application
- Current Limit Protection for Both Source and Sink
- OTSD Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

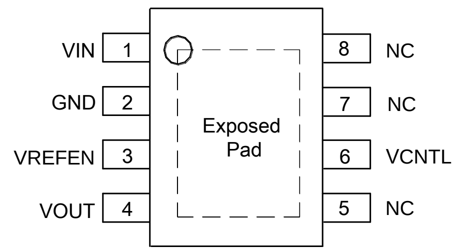
Pin Assignments

(Top View)



SOIC-8

(Top View)



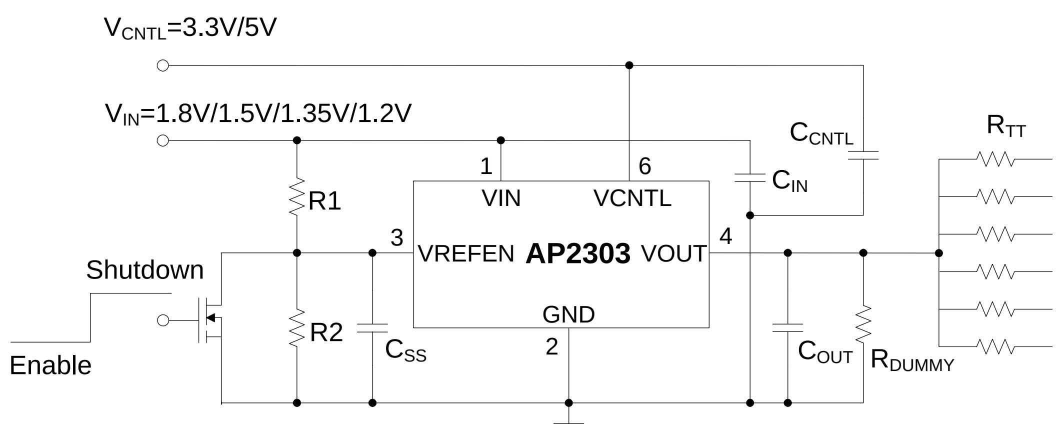
PSOP-8

Applications

- DDR-II/DDR-III/DDR-IIIL/DDR-IV Memory System
- Desktop PC, Notebook Mother Board
- Graphic Card
- STB, LCD-TV, Web-TV

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



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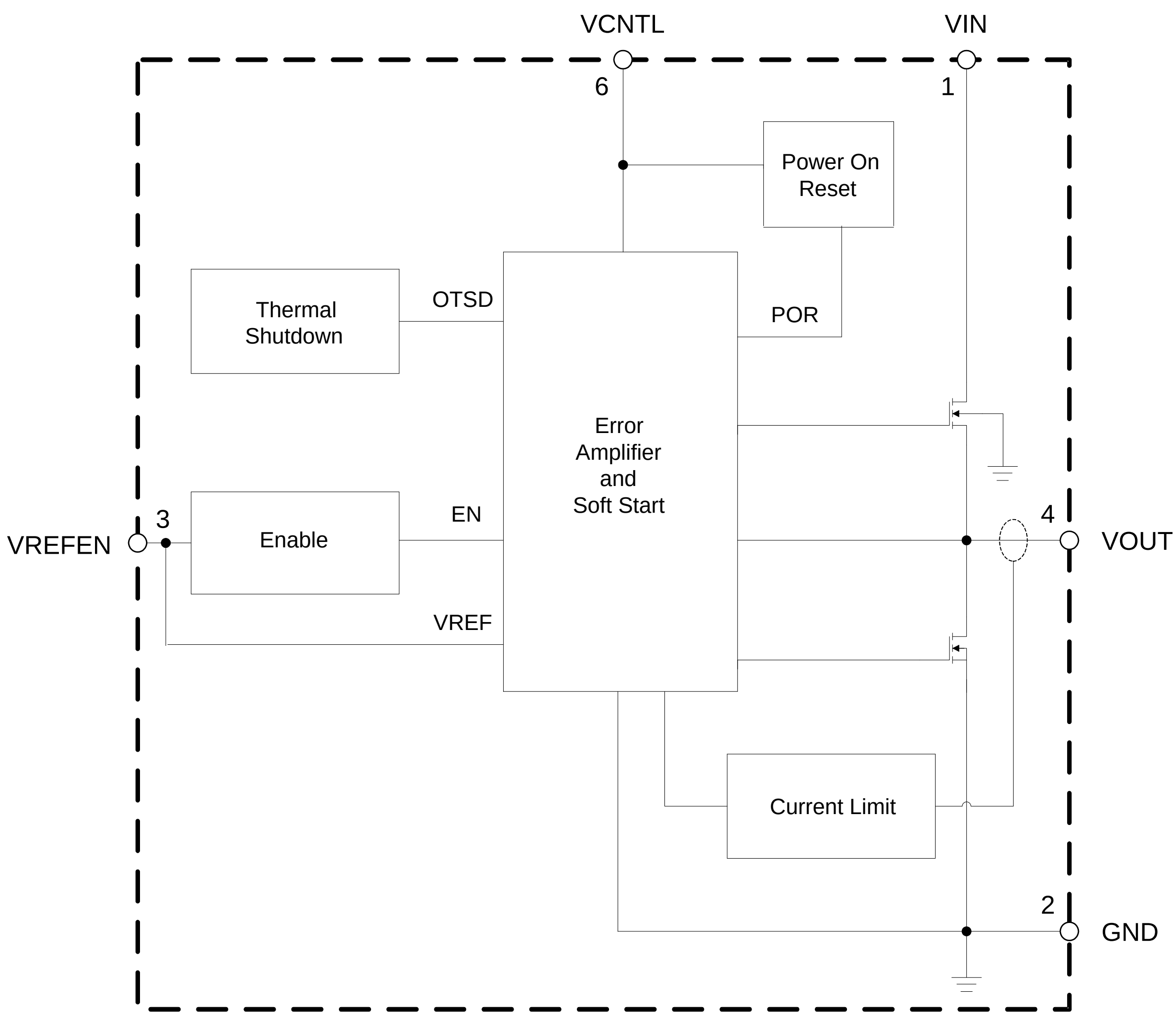
Pin Descriptions

Pin Number	Pin Name	Function
1	VIN	Unregulated input supply. A small 10µF MLCC should be connected from this pin to GND.
2	GND	Ground
3	VREFEN	Reference voltage input and active low shutdown control pin. Pulling the pin to ground turns off device by BJT or FET. When it is released, a soft-start will take for about 0.1ms.
4	VOUT	Regulated voltage output. A minimum of 10µF ceramic capacitor to ground is required to assure stability.
5, 7, 8	NC	No Connection
6	VCNTL	VCNTL supplies the internal control circuitry and provides the drive voltage.
–	Exposed Pad	The exposed pad should be connected to ground copper for better heat dissipation performance.

Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{IN}	Power Input Voltage	-0.3 to 6		V
V_{CNTL}	Control Input Voltage	-0.3 to 6		V
V_{REFEN}	Reference Input Voltage	-0.3 to 6		V
T_{STG}	Storage Temperature	+150		°C
T_J	Junction Temperature	+150		°C
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260		°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	PSOP-8	80	°C/W
		SOIC-8	110	
θ_{JC}	Thermal Resistance (Junction to Case)	PSOP-8	38	°C/W
		SOIC-8	50	
ESD	ESD (Human Body Model)	2000		V
ESD	ESD (Machine Model)	200		V

Notes: 4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

5. θ_{JA} is measured with the component mounted on a 2-Layer FR-4 board with 2.54cm*2.54cm thermal sink pad in free air.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CNTL}	Control Input Voltage (Note 6)	3.0	5.5	V
V_{IN}	Power Input Voltage	1.2	5.5	V
V_{REFEN}	Reference Input Voltage	0.6	V_{CNTL}-2.2	V
T_J	Operating Junction Temperature Range	-40	+125	°C
T_A	Operating Ambient Temperature Range	-40	+85	°C

Note 6: Keep $V_{CNTL} \geq V_{IN}$ in operation power on and power off sequences.

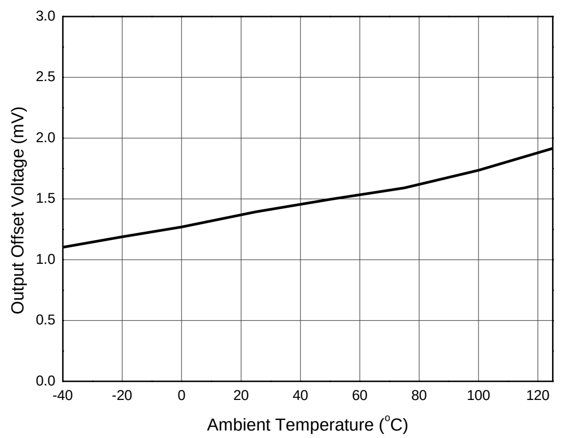
Electrical Characteristics (@T_A = +25°C, V_{IN} = 1.8V/1.5V/1.35V/1.2V, V_{CNTL} = 3.3V, V_{REFEN} = 0.9V/0.75V/0.675V/0.6V, C_{IN} = 10µF (Ceramic), C_{OUT} = 10µF (Ceramic), unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input						
I_{VCNTL}	VCNTL Operating Current	No Load	–	0.5	1.5	mA
$I_{SD-VCNTL}$	VCNTL Input Current in Shutdown Mode	V_{REFEN} < 0.15V	–	30	50	µA
I_{SD-VIN}	VIN Input Current in Shutdown Mode	V_{REFEN} < 0.15V	-1	–	1	µA
I_{VREFEN}	VREFEN Leakage Current	V_{REFEN} = 0.75V	-1	–	1	µA
Output						
V_{OS}	Output Offset Voltage (Note 7)	No Load	-10	0	10	mV
$V_{DROPOUT}$	Dropout Voltage	V_{CNTL} = 3.3V, I_{OUT} = 1A	–	220	–	mV
		V_{CNTL} = 3.3V, I_{OUT} = 1.5A	–	400	–	
		V_{CNTL} = 3.3V, I_{OUT} = 1.75A	–	520	–	
V_{LOAD}	Load Regulation	I_{OUT} = 0A to 1.75A	-20	–	20	mV
		I_{OUT} = 0A to -1.75A	-20	–	20	
Protection						
I_{LIMIT}	Current Limit	Source	1.75	–	–	A
		Sink	–	–	-1.75	
I_{SHORT}	Short Current	V_{OUT} = 0V	–	2	–	A
		V_{OUT} = V_{IN}	–	-2	–	
T_{SHDN}	Thermal Shutdown Temperature	3.3V ≤ V_{CNTL} ≤ 5V	–	+160	–	°C
–	Thermal Shutdown Hysteresis	–	–	+30	–	°C
Start-up & Shutdown Function						
V_{IH}	VREFEN Shutdown Threshold Voltage	Output = High	0.4	–	–	V
V_{IL}		Output = Low	–	–	0.15	
$V_{CNTL-ON}$	VCNTL Shutdown Threshold Voltage	Output = High	2.9	–	–	V
$V_{CNTL-OFF}$		Output = Low	–	–	2.2	
V_{IN-ON}	VIN Shutdown Threshold Voltage	Output = High	1.1	–	–	V
V_{IN-OFF}		Output = Low	–	–	0.4	

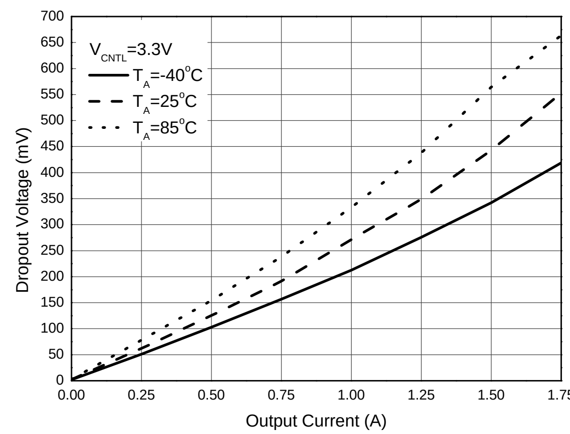
Note 7: V_{OS} is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Performance Characteristics

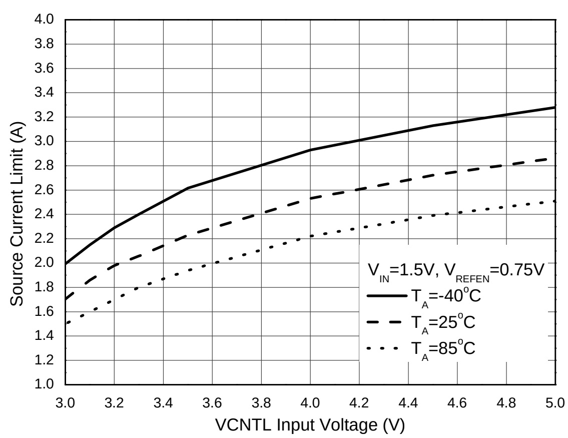
Output Offset Voltage vs. Ambient Temperature



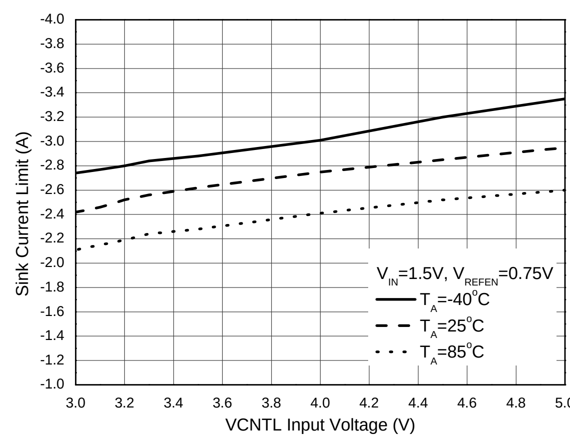
Dropout Voltage vs. Output Current



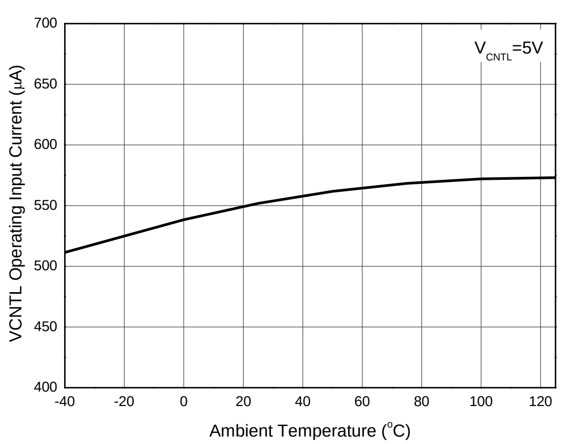
Source Current Limit vs. VCNTL Input Voltage



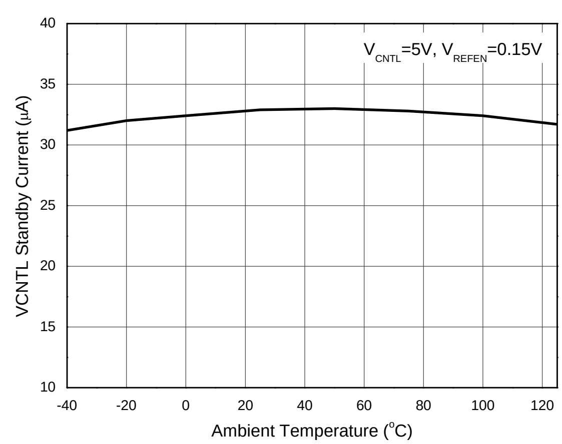
Sink Current Limit vs. VCNTL Input Voltage



VCNTL Operating Input Current vs. Ambient Temperature

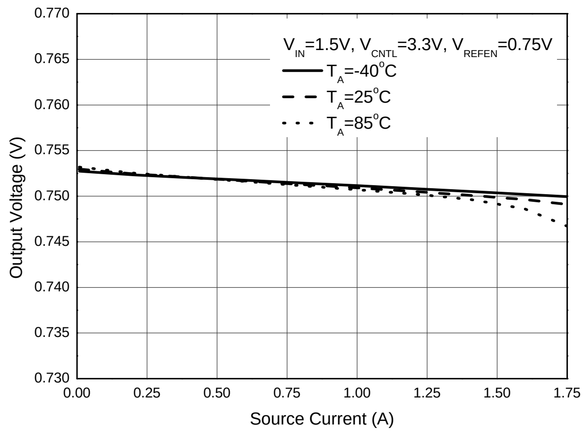


VCNTL Standby Current vs. Ambient Temperature

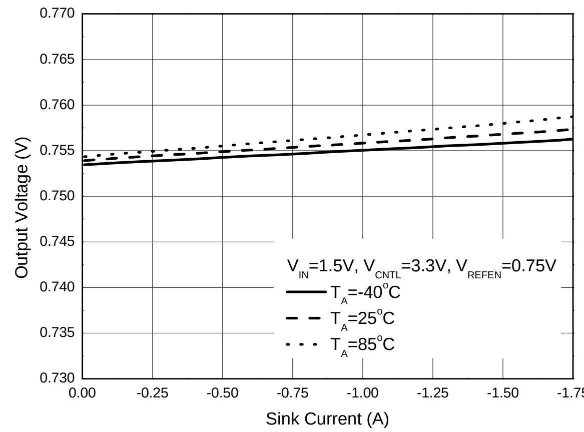


Performance Characteristics (Cont.)

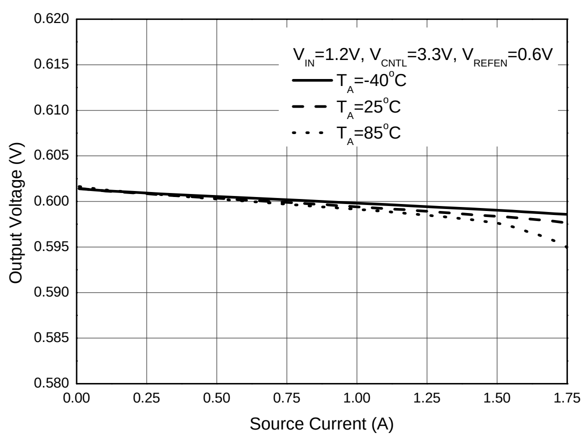
Output Voltage vs. Source Current (DDR-III)



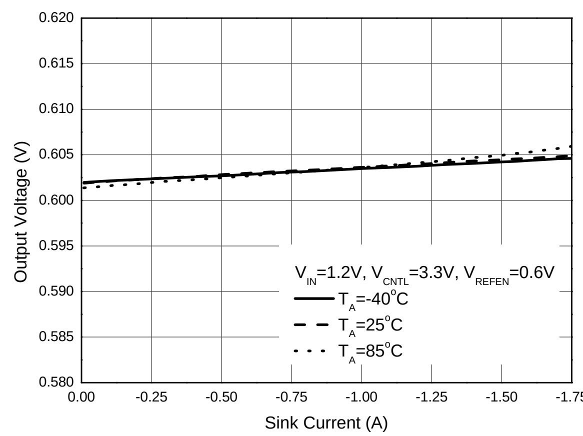
Output Voltage vs. Sink Current (DDR-III)



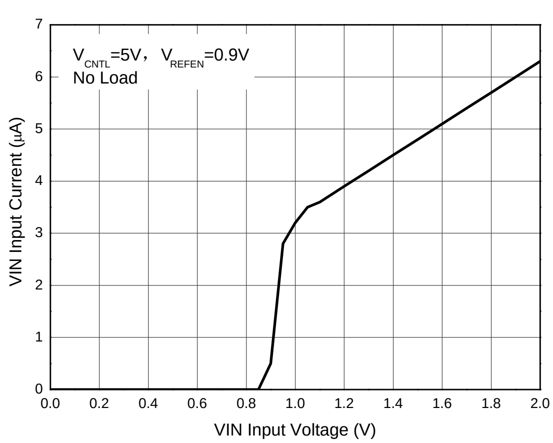
Output Voltage vs. Source Current (DDR-IV)



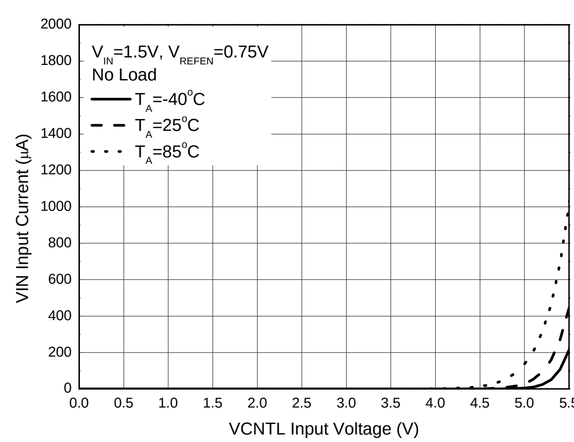
Output Voltage vs. Sink Current (DDR-IV)



VIN Input Current vs. VIN Input Voltage



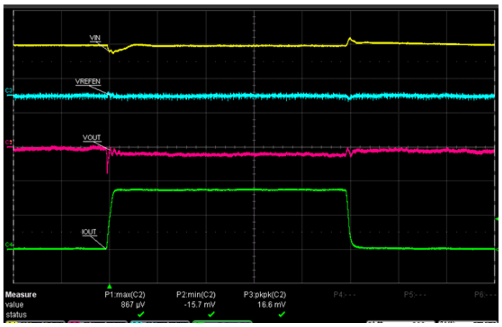
VIN Input Current vs. VCNTL Input Voltage



Performance Characteristics (Cont.)

Source Load Transient (DDR-III)
(C_{IN}=C_{OUT}=10μF, I_{OUT}=0A to 1.75A, V_{IN}=1.5V, V_{REFEN}=0.75V, V_{CNTL}=3.3V)

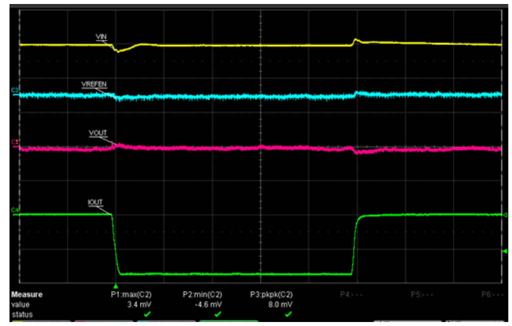
V_{IN} 500mV/div
V_{REFEN} 50mV/div
V_{OUT} 20mV/div
I_{OUT} 1A/div



Time 100 µs/div

Sink Load Transient (DDR-III)
(C_{IN}=C_{OUT}=10μF, I_{OUT}=0A to -1.75A, V_{IN}=1.5V, V_{REFEN}=0.75V, V_{CNTL}=3.3V)

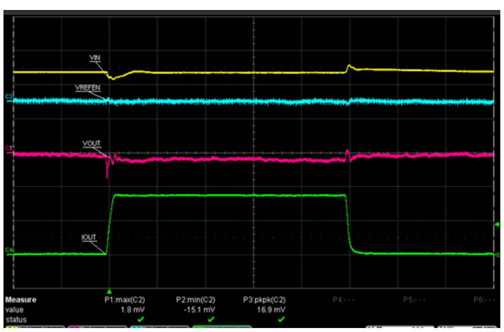
V_{IN} 500mV/div
V_{REFEN} 50mV/div
V_{OUT} 20mV/div
I_{OUT} 1A/div



Time 100 µs/div

Source Load Transient (DDR-IV)
(C_{IN}=C_{OUT}=10μF, I_{OUT}=0A to 1.75A, V_{IN}=1.2V, V_{REFEN}=0.6V, V_{CNTL}=3.3V)

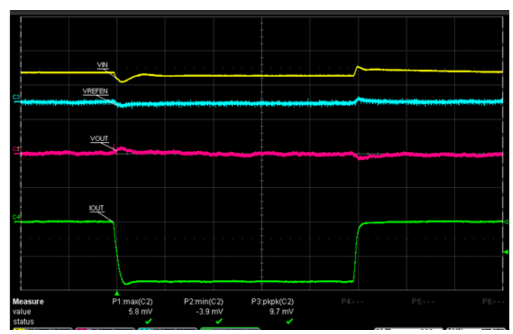
V_{IN} 500mV/div
V_{REFEN} 50mV/div
V_{OUT} 20mV/div
I_{OUT} 1A/div



Time 100 µs/div

Sink Load Transient (DDR-IV)
(C_{IN}=C_{OUT}=10μF, I_{OUT}=0A to -1.75A, V_{IN}=1.2V, V_{REFEN}=0.6V, V_{CNTL}=3.3V)

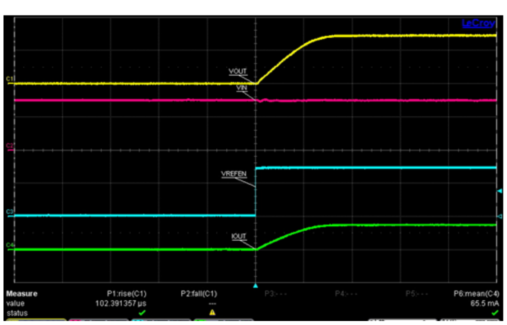
V_{IN} 500mV/div
V_{REFEN} 50mV/div
V_{OUT} 20mV/div
I_{OUT} 1A/div



Time 100 µs/div

VREFEN Power On
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω, V_{CNTL}=5V)

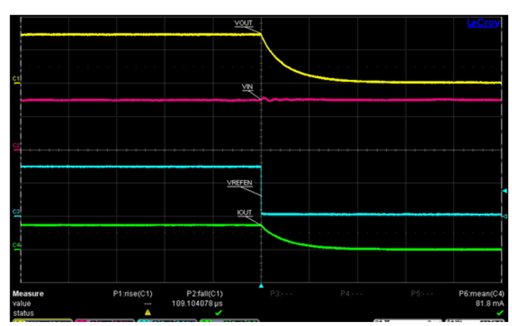
V_{OUT} 500mV/div
V_{IN} 1V/div
V_{REFEN} 500mV/div
I_{OUT} 200mA/div



Time 100 µs/div

VREFEN Power Off
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω, V_{CNTL}=5V)

V_{OUT} 500mV/div
V_{IN} 1V/div
V_{REFEN} 500mV/div
I_{OUT} 200mA/div



Time 100 µs/div

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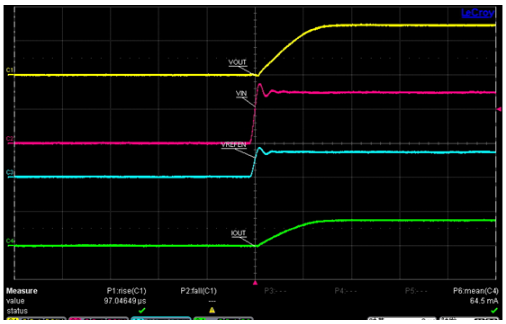
Performance Characteristics (Cont.)

VIN Power On
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω, V_{CNTL}=5V)

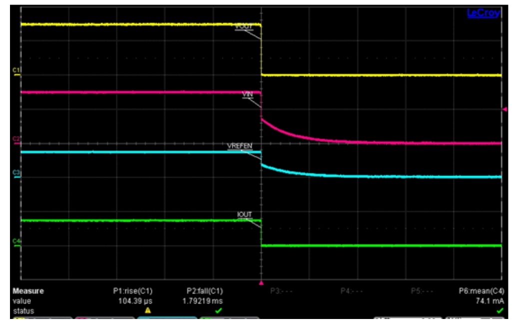
V_{OUT} 500mV/div
V_{IN} 1V/div
V_{REFEN} 1V/div
I_{OUT} 200mA/div



Time 100 μs/div

VIN Power Off
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω, V_{CNTL}=5V)

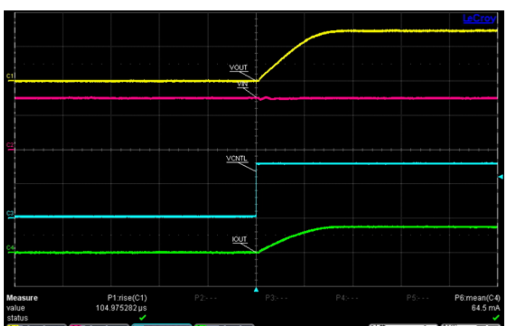
V_{OUT} 500mV/div
V_{IN} 1V/div
V_{REFEN} 1V/div
I_{OUT} 200mA/div



Time 500ms/div

VCNTL Power On
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω)

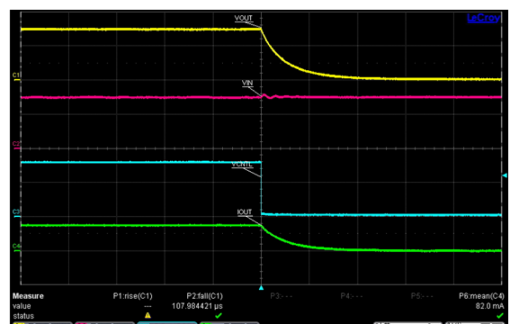
V_{OUT} 500mV/div
V_{IN} 1V/div
V_{CNTL} 2V/div
I_{OUT} 200mA/div



Time 100 μs/div

VCNTL Power Off
(C_{IN}=C_{OUT}=10μF, R_{LOAD}=5Ω)

V_{OUT} 500mV/div
V_{IN} 1V/div
V_{CNTL} 2V/div
I_{OUT} 200mA/div



Time 100 μs/div

NEW PRODUCT

Application Information

1. Input Capacitor

The input capacitor of VIN should be placed to VIN pin as close as possible. Use a low ESR, 10µF or larger MLCC capacitor to provide surge current during load transient.

The input capacitor for VCNTL is recommended to be 0.47µF or larger to decouple the supply voltage of AP2303's control circuitry.

2. Output Capacitor

The output capacitor is recommended with a 10µF or higher MLCC capacitor which will be sufficient at full temperature range. An aluminum electrolytic capacitor with low ESR also should be larger than 10µF. The output capacitor should be placed to VOUT pin as close as possible.

3. Reference Voltage

A reference voltage is applied to the VREFEN pin by a resistor divider between VIN and GND pins. And a 0.1µF to 1µF bypass capacitor is preferred to form a low-pass filter to reduce the noise from VIN. More capacitance and large resistance will increase the start-up time after VIN power-up.

4. Thermal Consideration

There's an internal thermal protection circuitry of AP2303 to protect device during overload conditions. For continuous operation, make sure not to exceed the operating junction temperature range of +125°C. The power dissipation definition in device is:

$P_D=(V_{IN} - V_{OUT})xI_{OUT}+V_{IN}xI_Q$

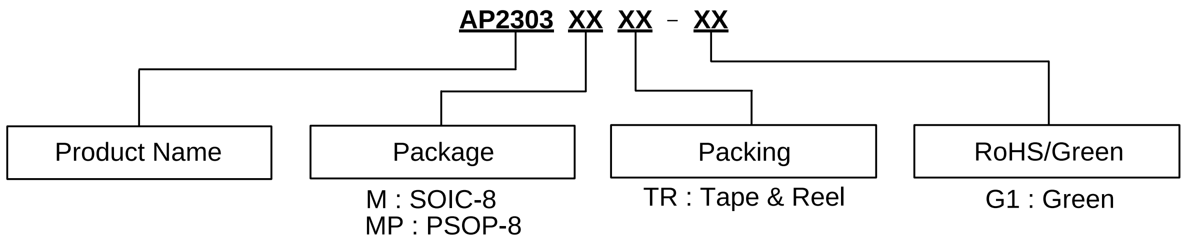
The maximum power dissipation depends on the thermal resistance of IC package, PCB layout and the surrounding airflow. The maximum power dissipation can also be calculated as:

$P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$

The maximum power dissipation for PSOP-8 package at T_A = +25°C can be calculated as:

$P_{D(MAX)}$ = (125°C-25°C) / (80°C/W) = 1.25W

Ordering Information

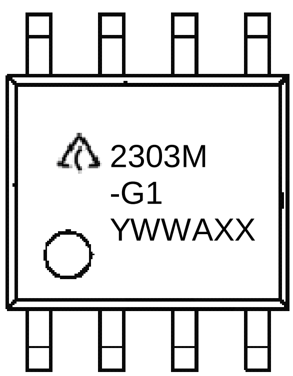


Package	Temperature Range	Part Number	Marking ID	Packing
SOIC-8	-40 to +85°C	AP2303MTR-G1	2303M-G1	4000/Tape & Reel
PSOP-8		AP2303MPTR-G1	2303MP-G1	4000/Tape & Reel

Marking Information

(1) SOIC-8

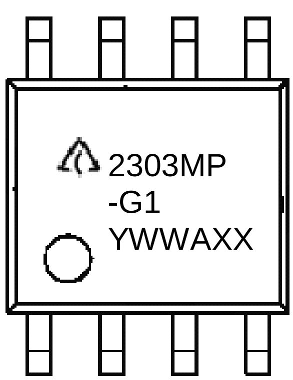
(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and8th Digits of Batch No.

(2) PSOP-8

(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

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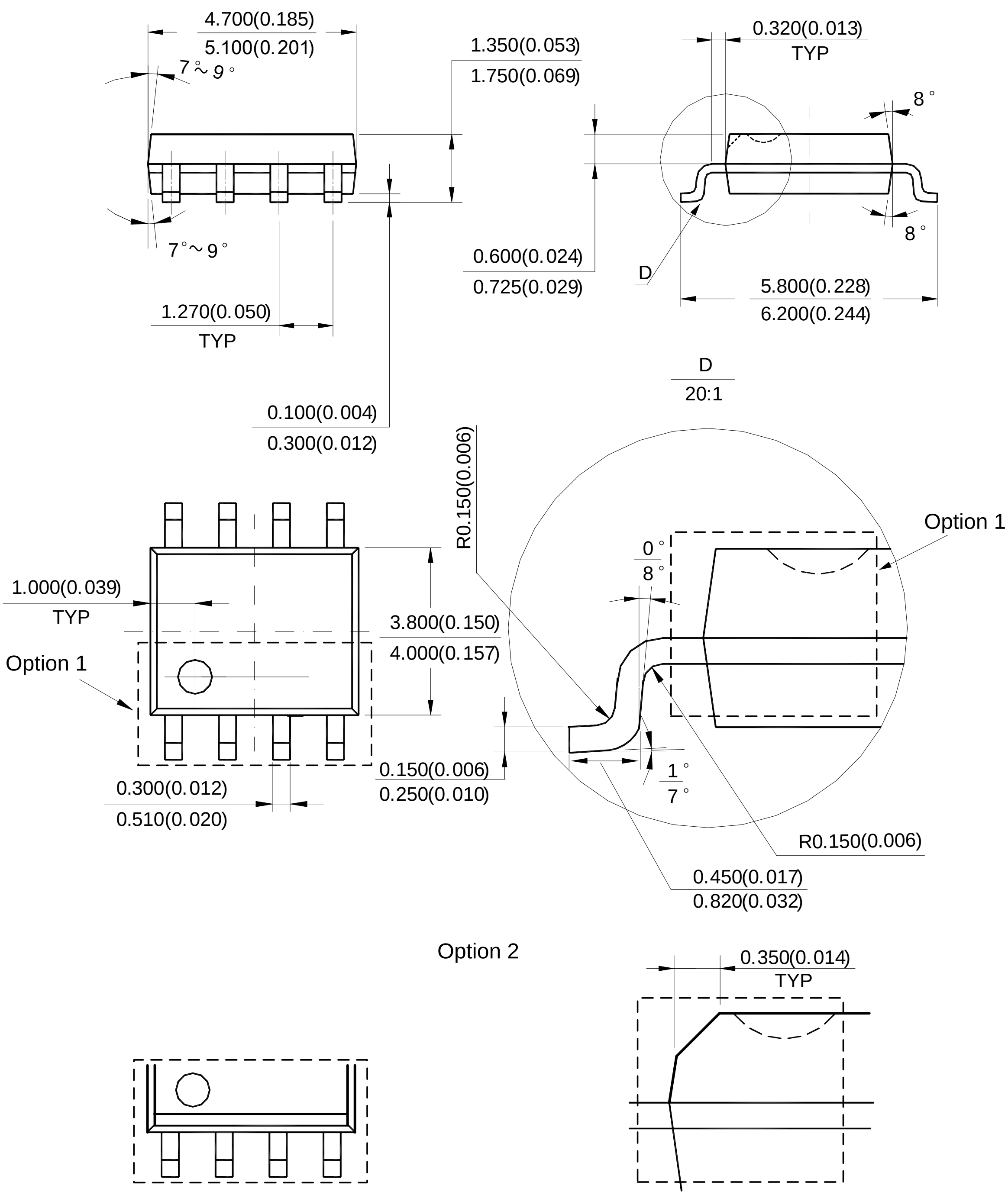
Package Outline Dimensions (All dimensions in mm(inch).)

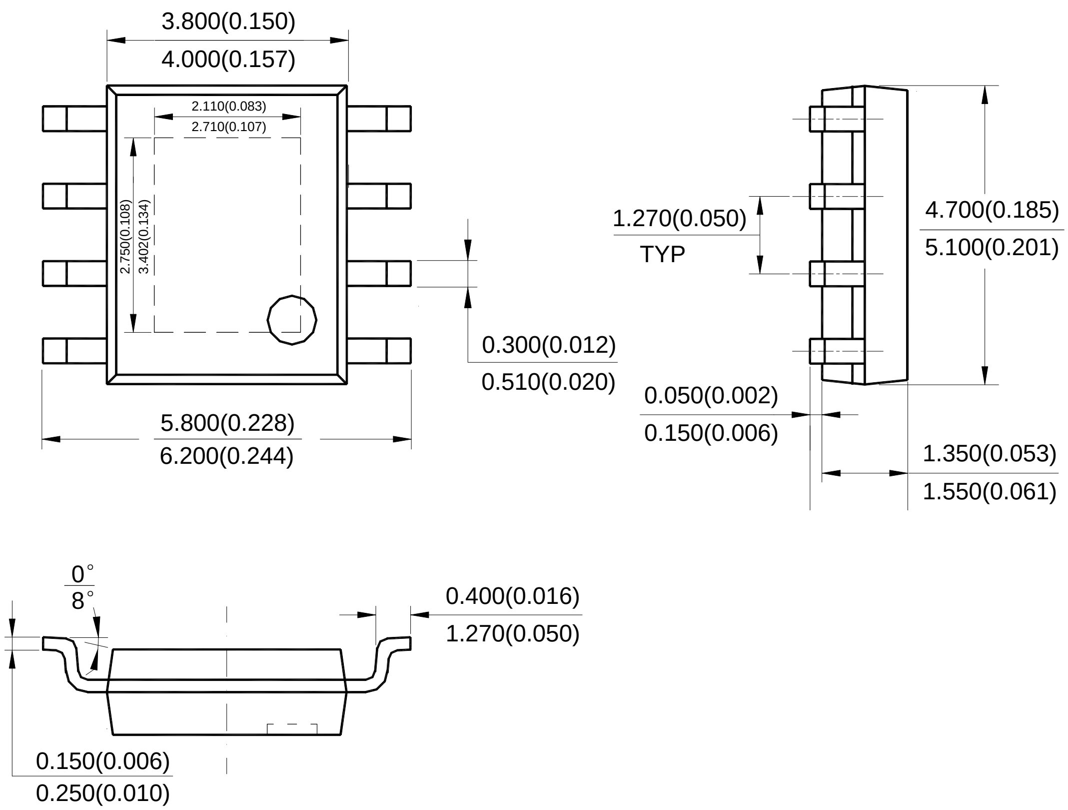
(1) Package Type: SOIC-8



Note: Eject hole, oriented hole and mold mark is optional.

Package Outline Dimensions (Cont. All dimensions in mm(inch).)

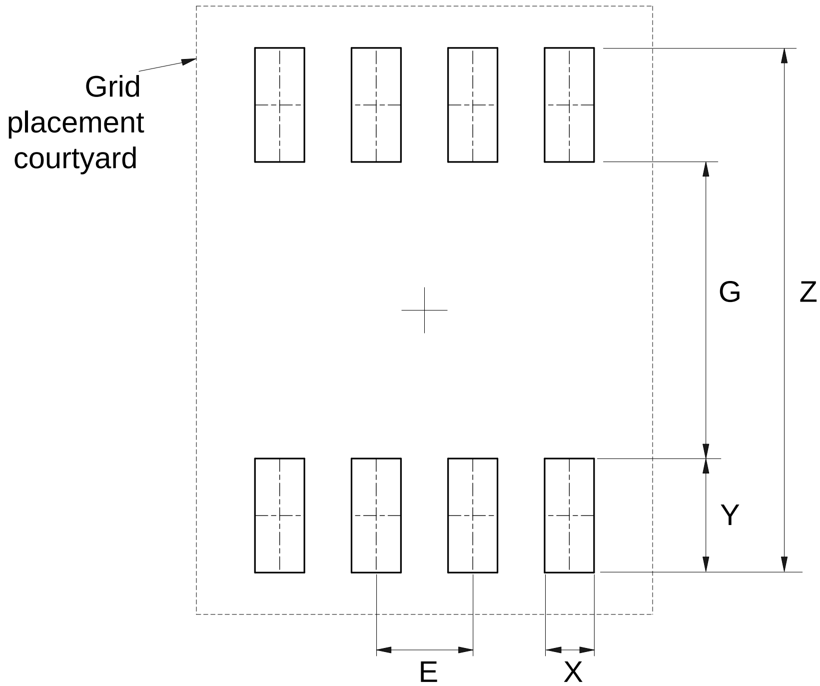
(2) Package Type: PSOP-8



Note: Eject hole, oriented hole and mold mark is optional.

Suggested Pad Layout

(1) Package Type: SOIC-8



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050

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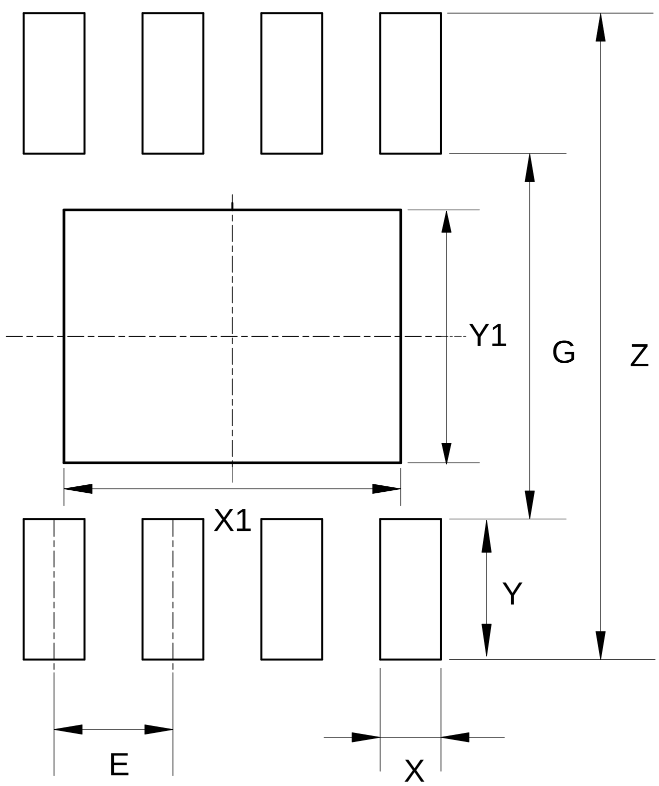
Suggested Pad Layout (Cont.)

(2) Package Type: PSOP-8



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	3.600/0.142	2.700/0.106	1.270/0.050