DS1886

SFP and PON ONU Controller with Digital LDD Interface

General Description

The DS1886 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality for GPON/EPON and 10G PON ONU applications. The combination of the DS1886 with the MAX3710 supports all transmitter and receiver functionality. The DS1886 includes modulation current control and APC setpoint control with tracking error adjustment. It continually monitors RSSI for LOS generation. A 13-bit analog-to-digital converter (ADC) monitors V_{CC}, temperature, laser bias, laser modulation, and receive power to meet all monitoring requirements. Receive power measurement is differential with support for common mode to V_{CC}. A 9-bit digital-to-analog converter (DAC) is included with temperature compensation for APD bias control.

Applications

SFF, SFP, and PON ONU Modules

Ordering Information appears at end of data sheet.

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Companion Controller for the MAX3710 Laser Driver/Limiting Amplifier and MAX3945 Limiting Amplifier**
- **MAX3710/DS1886 Combination Supports Broad Spectrum of Continuous Mode and PON Applications Up to 2.5GHz**
- **Temperature Lookup Table (LUT) to Compensate for APC Tracking Error and Dual Closed-Loop Variables**
- **Three Laser Control Modes**
  - **Dual Closed Loop: Laser Bias and Laser Modulation Are Automatically Controlled with Multiple LUTs to Compensate Dual Closed-Loop Calibration Points**
  - **APC Loop: Laser Bias Automatically Controlled, Laser Modulation Controlled by Temperature LUT**
  - **Open Loop: Laser Bias and Laser Modulation Are Controlled by Temperature LUTs**
- **13-Bit ADC**
  - **Laser Bias, Laser Power, and Receive Power Support Internal and External Calibration**
  - **Differential Receive Power Input**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **10-Bit DAC with Temperature Compensation for APD Bias**
- **Digital I/O Pins: Transmit Disable Input/Output, Rate Select Input, LOS Input/Output, Transmit Fault Input/Output, and IN1 Status Monitor and Fault input**
- **Comprehensive Fault Measurement System with Maskable Alarm/Warnings**
- **Flexible Password Scheme Provides Three Levels of Security**
- **256-Byte A0h and 128-Byte Upper A2h EEPROM**
- **I^2C-Compatible Interface**
- **3-Wire Master to Communicate with the MAX3710/MAX3711 Laser Driver/Limiting Amplifier and MAX3945 Limiting Amplifier**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6259; Rev 1; 8/12

DS1886

SFP and PON ONU Controller with Digital LDD Interface

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ABSOLUTE MAXIMUM RATINGS

(All voltages relative to ground.)
Voltage Range on IN1, DAC, LOS, RSSIP, RSSIN, REFIN, RSEL, TXF, TXMON, TXD..... -0.5V to (V_{CC} + 0.5V) (subject to not exceeding +6V)
Voltage Range on V_{CC}, SDA, SCL, TXFOUT and LOSOUT .....-0.5V to +6V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C).....2285.7mW
Operating Temperature Range ..... -40°C to +95°C
Programming Temperature Range ..... 0°C to +95°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 2)	2.97		3.63	V
High-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IL:1}$		-0.3		+0.3 x V_{CC}	V
High-Level Input Voltage (IN1, LOS, RSEL, TXD, TXF)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (IN1, LOS, RSEL, TXD, TXF)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 2, 3)		0.7	2	mA
Output Leakage (LOSOUT, SDA, SDAOUT, TXFOUT)	I_{LO}				1	µA
Low-Level Output Voltage (CSEL1OUT, CSEL2OUT, LOSOUT, SDA, SDAOUT, SCLOUT, TXDOUT, TXFOUT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (CSEL1OUT, CSEL2OUT, SCLOUT, SDAOUT, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
Input Leakage Current (IN1, LOS, RSEL, SCL, TXD, TXF)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.6		2.6	V
Analog Power-On Reset	POA	POA > POD by design	2.2		2.8	V

DAC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delta-Sigma Input Clock Frequency	f_{DS}			2.1		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Output and Reference* section for details (DAC FS[9:2] = FFh)			10	Bits
Output Impedance	R_{DS}	V_{REFIN} = 2.5V		45	100	Ω
Recovery After Power-Up	t_{INIT_DAC}	From V_{CC} > VCC LO alarm or warning	See the *Startup Timing Characteristics* table			ms

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution		(Note 4)		13		Bits
INL		T_A = +25°C	-3		+3	LSB
DNL			-1		+1	LSB
Update Rate for Temperature, TXMON (TXB/TXP), RSSIP-RSSIN, V_{CC}	t_{RR}	RSSIP-RSSIN requires only a coarse conversion (Note 5)		30		ms
Update Rate for RSSIP-RSSIN	$t_{R/R2}$	RSSIP-RSSIN requires a fine conversion		36		ms
Input/Supply Offset (TXMON, RSSIP, RSSIN, V_{CC})	V_{OS}	(Notes 5, 6)	-1	0	+1	LSB
Factory Setting Full Scale		TXMON and RSSIP-RSSIN coarse (Notes 6, 7)		2.5		V
		V_{CC} (Note 7)		6.5536		
		RSSIP-RSSIN fine (Note 7)		312.5		µV
Temperature LSB Weighting				1/256		°C

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C, guaranteed by design	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Rising Edge to Fault Clear	t_{OFF}	From ↑ TXD (Notes 8, 9)			5	µs
TXD Falling Edge to TXDOUT Falling	t_{ON}	From ↓ TXD (Note 10)			5	µs
Recovery After Power-Up: MAX3710	t_{INIT_3710}	From ↑ V_{CC} > POA (Note 11)		1		ms
Recovery After Power-Up: MAX3710 and MAX3945	t_{INIT_3945}	From ↑ V_{CC} > VCC LO alarm or warning (Note 12)		1		ms
Fault Assert Time (to TXFOUT = 1)	t_{INITR1}	From ↓ TXD		30		ms
Fault Reset Time at Power-On (to TXFOUT = 0)	t_{INITR2}	From ↑ V_{CC} > POA, Figure 12c (Note 13)		12.5		ms

STARTUP TIMING CHARACTERISTICS

(V_{CC}= +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Enable Time Following POA	t_{INIT}	(Notes 13, 14)		13		ms

3-WIRE DIGITAL INTERFACE SPECIFICATION

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Note 1) (See Figure 13.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLOUT Clock Frequency	f_{SCLOUT}			1.05		MHz
SCLOUT Duty Cycle	t_{3WDC}			50		%
SDAOUT Setup Time	t_{DS}			500		ns
SDAOUT Hold Time	t_{DH}		100			ns
CSEL1OUT, CSEL2OUT Pulse-Width Low	t_{CSW}		1			µs
CSEL1OUT, CSEL2OUT Leading Time Before the First SCLOUT Edge	t_L			1		µs
CSEL1OUT, CSEL2OUT Trailing Time After the Last SCLOUT Edge	t_T			1		µs
SDAOUT, SCLOUT Load	C_{B3W}	Total bus capacitance on one line			10	pF

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Note 1) (See Figure 19.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 15)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data in Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data in Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 16)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 16)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_W	(Note 17)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, unless otherwise noted.) (Note 1)

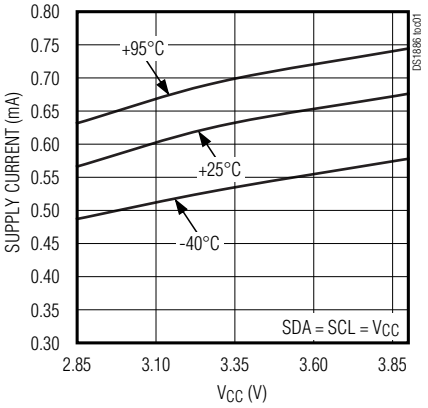
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At T_A = +25°C	50,000			—
		At T_A = +85°C	10,000			

Note 1: Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 2: All voltages are referenced to ground. Current entering the IC is considered positive, and current exiting the IC is considered negative.
Note 3: Inputs are at supply rail. Outputs are not loaded. Does not include REFIN current. Measured using the *Typical Operating Circuit—GPON ONU*.
Note 4: The ADC output is available internally as a 16-bit value. The 16 bits are derived by left-shifting the 13-bit ADC output by 3.
Note 5: Guaranteed by design.
Note 6: TXB (transmit bias) and TXP (transmit power) are separate ADC conversions that are performed on the same input pin, TXMON.
Note 7: Full scale is user-programmable.
Note 8: Time until faults are cleared (falling edge of TXFOUT).
Note 9: Time until rising edge of TXDOUT.
Note 10: Time until falling edge of TXDOUT.
Note 11: Time until completion of initial MAX3710 control registers configuration.
Note 12: Time until completion of initial MAX3945 and MAX3710 control registers configuration.
Note 13: VCC LO alarm or warning is enabled, a V_{CC} conversion is completed, and V_{CC} is above VCC LO alarm or warning. See Figure 12c.
Note 14: DAC output valid, 3-wire writes from LUTs complete, and digital outputs valid.
Note 15: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard mode.
Note 16: C_B = Total capacitance of one bus line in pF.
Note 17: EEPROM write begins after a STOP condition occurs.

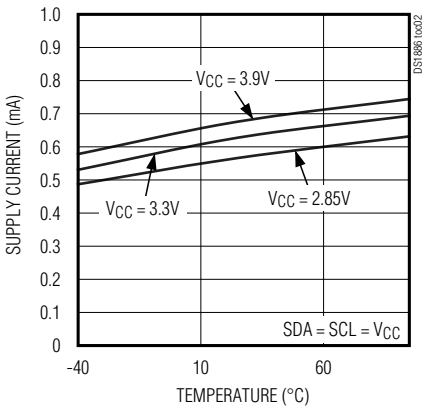
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

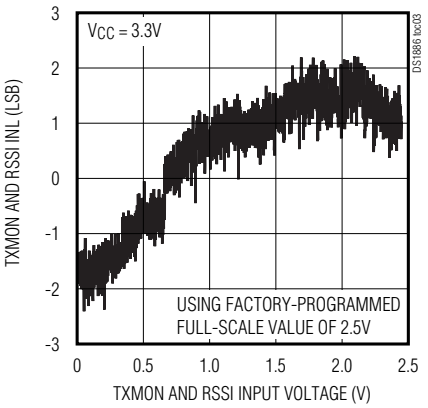
SUPPLY CURRENT vs. SUPPLY VOLTAGE



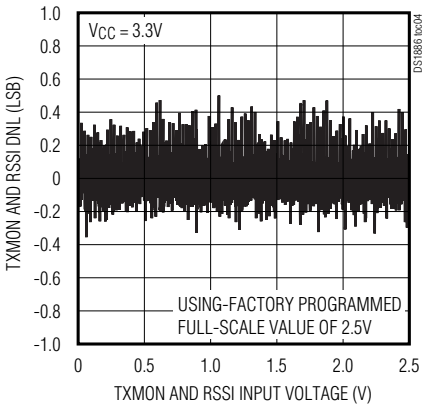
SUPPLY CURRENT vs. TEMPERATURE



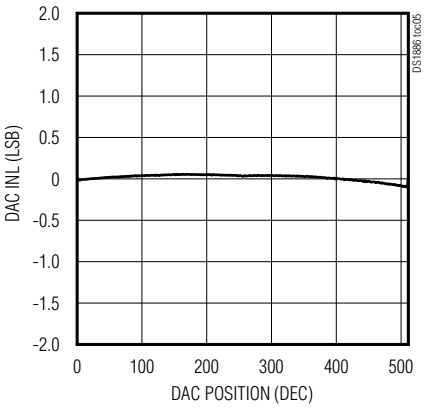
TXMON AND RSSI INL



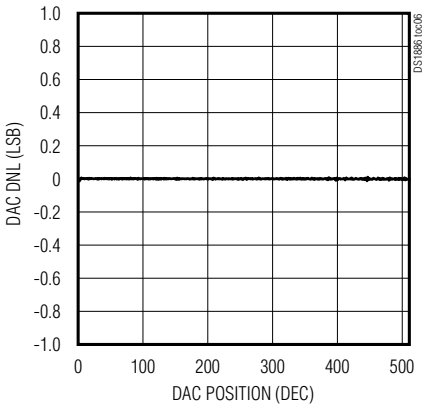
TXMON AND RSSI DNL



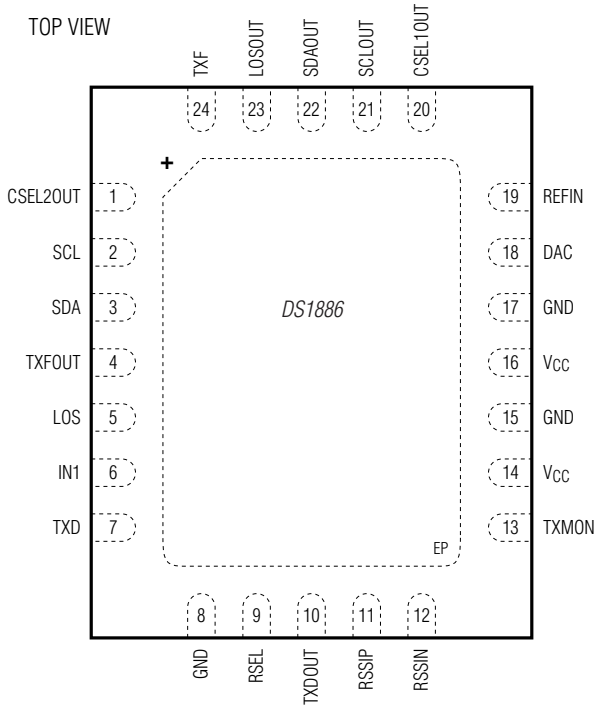
DAC INL



DAC DNL



Pin Configuration

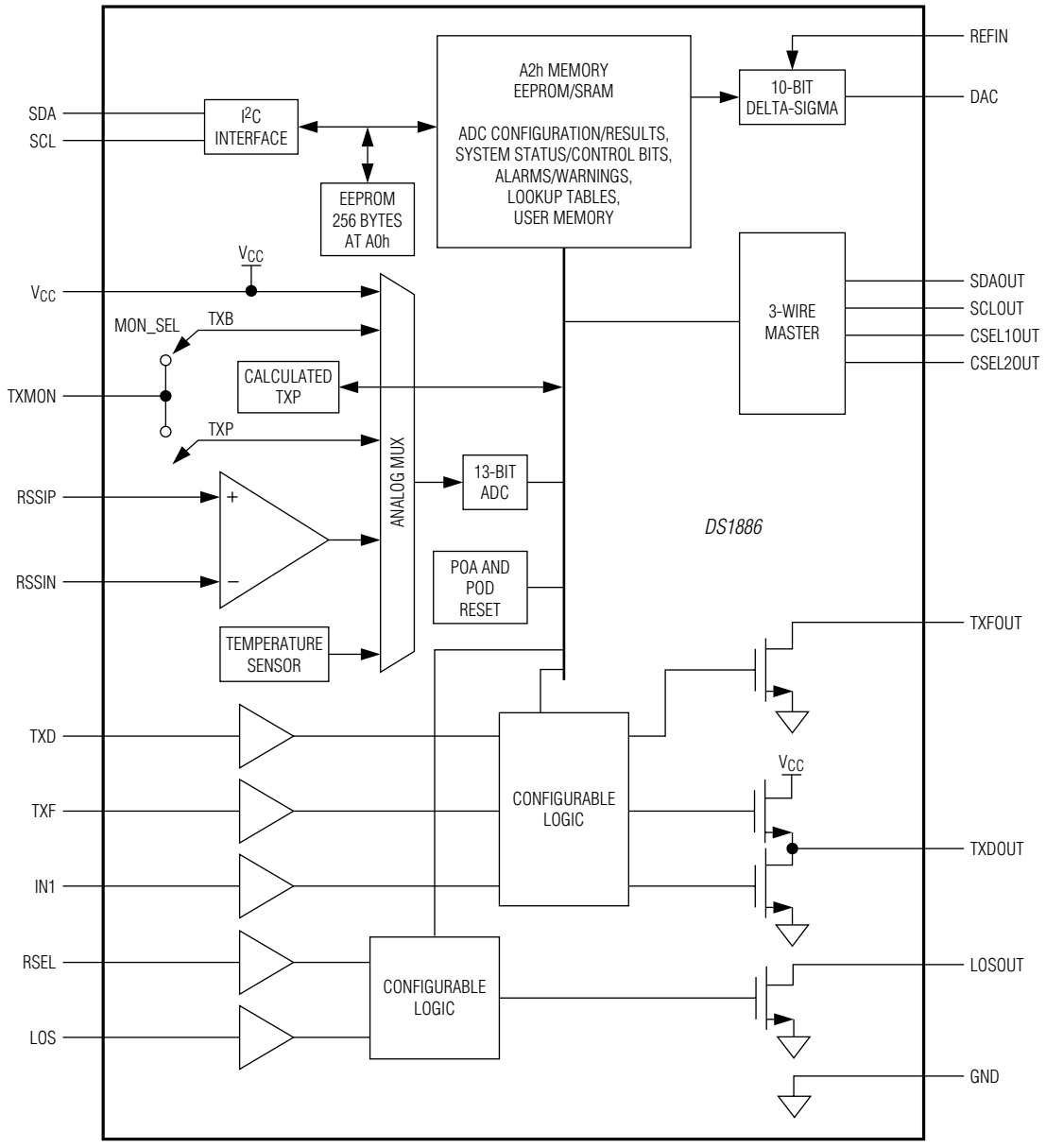


TQFN
(4mm × 5mm × 0.75mm)

Pin Description

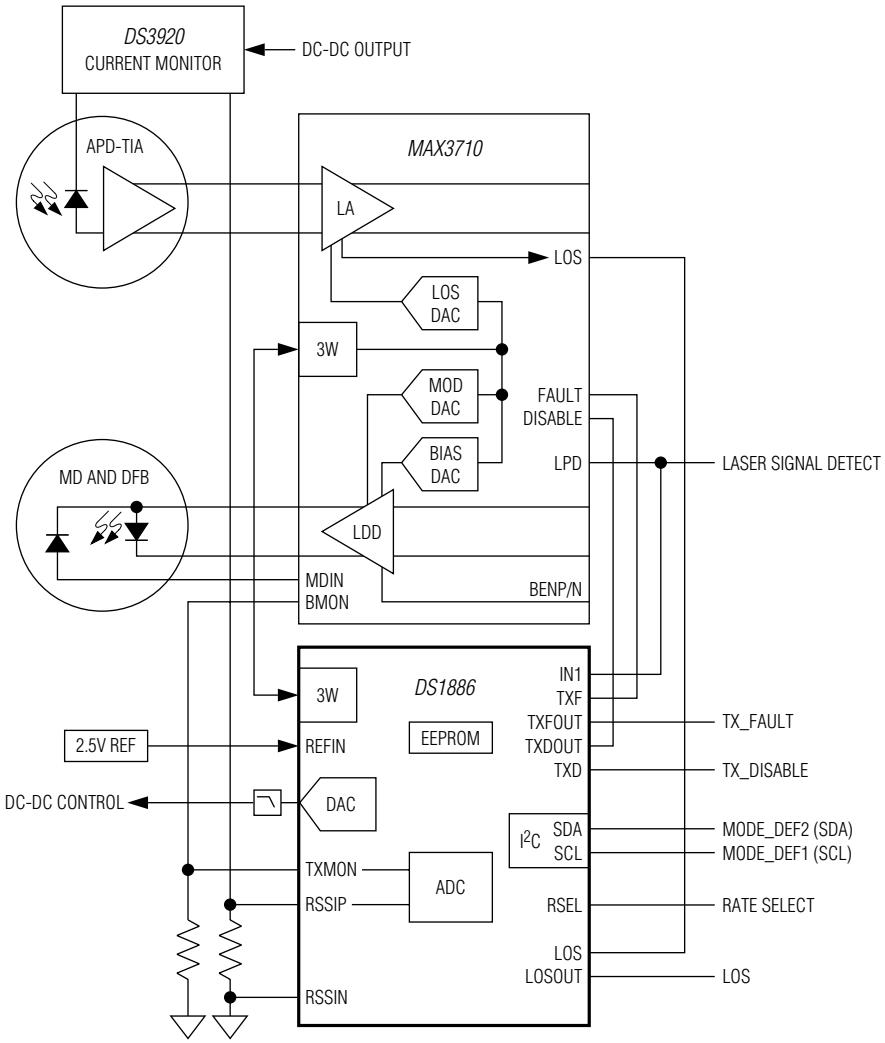
PIN	NAME	FUNCTION
1	CSEL2OUT	Chip-Select Output. Part of the 3-wire interface to the MAX3945.
2	SCL	I^2C Serial-Clock Input
3	SDA	Open-Drain I^2C Serial-Data Input/ Output
4	TXFOUT	Open-Drain Transmit Fault Output
5	LOS	Loss-of-Signal Input
6	IN1	Digital Maskable Fault Input
7	TXD	Transmit Disable Input
8, 15, 17	GND	Ground
9	RSEL	Rate Select Input
10	TXDOUT	Transmit Disable Output
11, 12	RSSIP, RSSIN	Differential External Monitor Input
13	TXMON	External Monitor Input for Both Transmit Power (TXP) and Transmit Bias (TXB)
14, 16	V_{CC}	Power-Supply Input
18	DAC	DAC Output
19	REFIN	Reference Input for DAC Full Scale
20	CSEL1OUT	Chip-Select Output. Part of the 3-wire interface to the MAX3710.
21	SCLOUT	Serial-Clock Output. Part of the 3-wire interface to the MAX3710.
22	SDAOUT	Serial-Data Input/Output. Part of the 3-wire interface to the MAX3710.
23	LOSOUT	Open-Drain Receive Loss-of-Signal Output
24	TXF	Transmit Fault Input
—	EP	Exposed Pad. Connect to ground.

Block Diagram

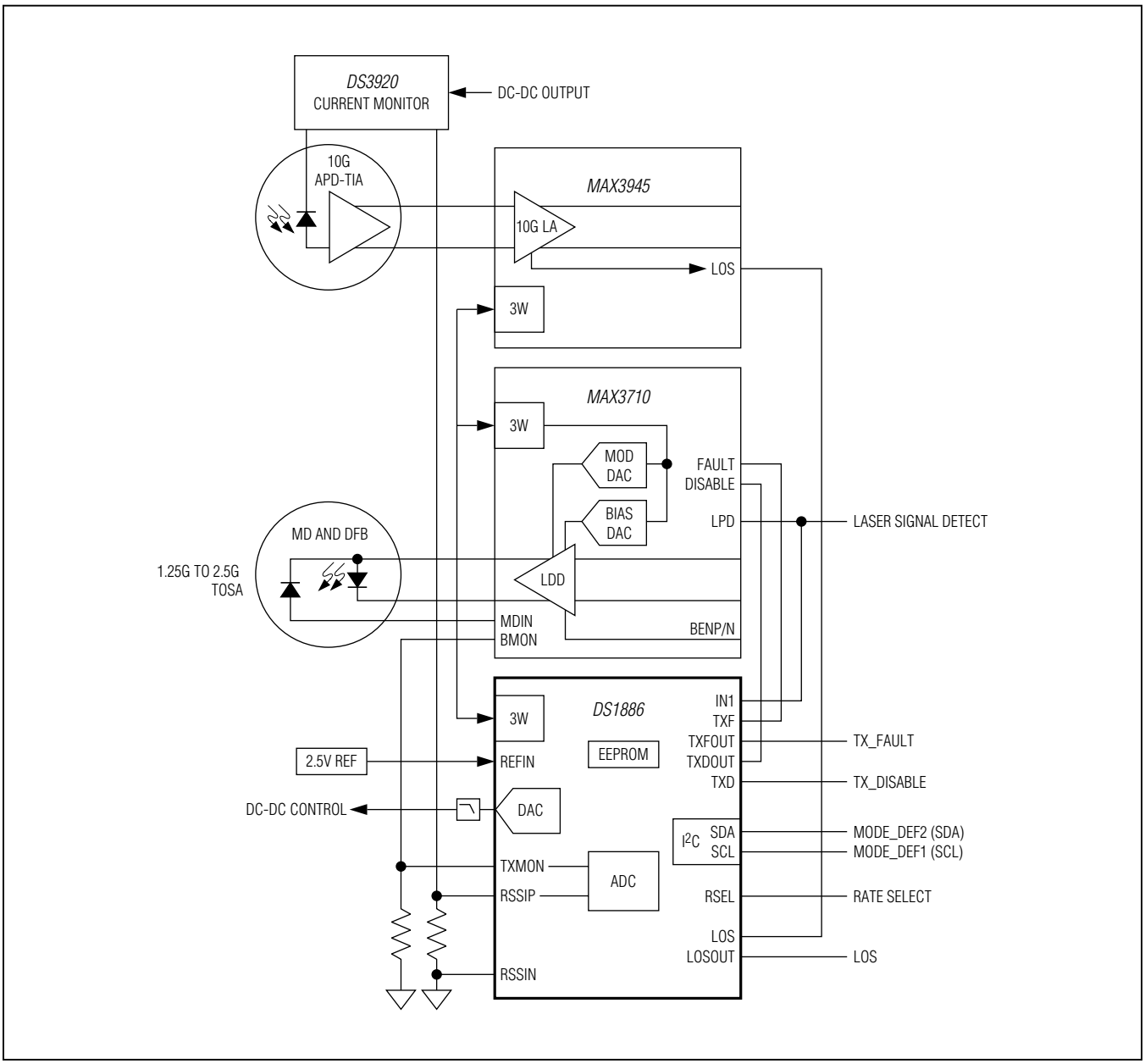


*See Figure 1a, 1b

Typical Operating Circuit—GPON ONU



Typical Operating Circuit—10G PON ONU



Detailed Description

The DS1886 integrates the control and monitoring functionality required to implement an SFP or PON ONU system using the Maxim MAX3710 or other compatible laser driver and limiting amplifier. Key components of the DS1886 are shown in the *Block Diagram* and described in subsequent sections.

Table 1. Acronyms

ACRONYM	DESCRIPTION
ADC	Analog-to-Digital Converter
APC	Automatic Power Control
APD	Avalanche Photodiode
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	LUT
NV	Nonvolatile
QT	Quick Trip
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM

ACRONYM	DESCRIPTION
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form-Factor Pluggable
SFP+	Enhanced SFP
TE	Tracking Error. Deviation from linear of the relationship between transmitted power and monitor diode current.
TIA	Transimpedance Amplifier
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

Monitors and Fault Detection

Monitors

The DS1886 monitors five ADC channels. This monitoring combined with the alarm enables (A2h Table 01h/05h) determines when/if the DS1886 turns off the MAX3710 DACs and triggers the TXFOUT and TXDOUT outputs. All the monitoring levels and interrupt masks are user-programmable. See Figure 1a.

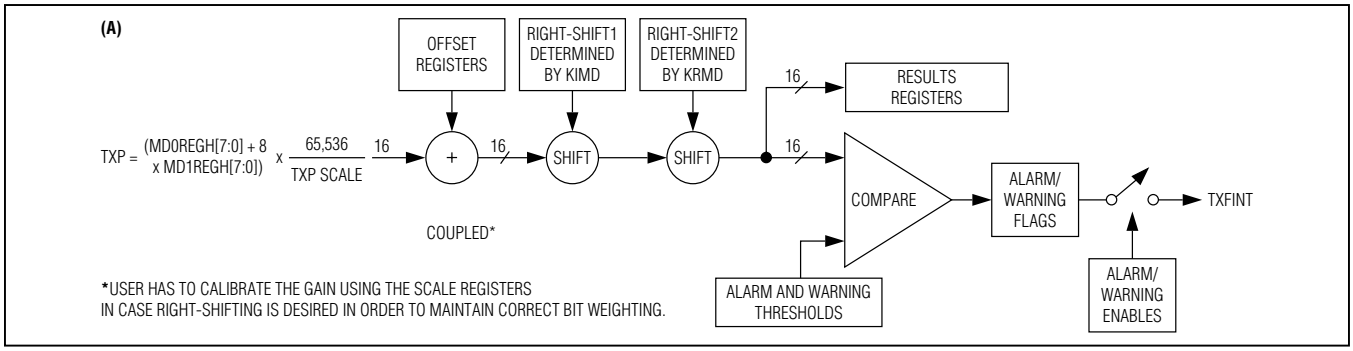


Figure 1a. ADC Channel Only for TXP when BURST_MODE = 1 in Table 02h, Register 89h

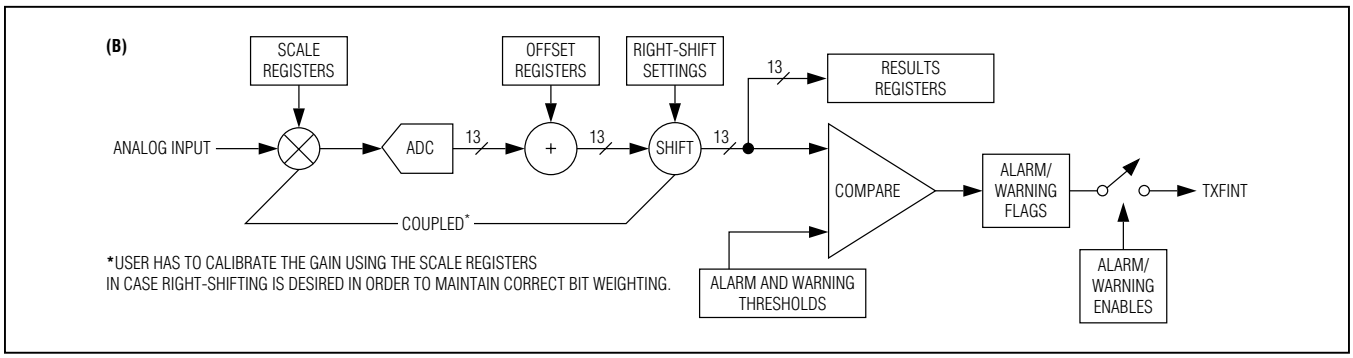


Figure 1b. ADC Channel

ADC Monitors and Alarms

The ADC monitors temperature (internal temp sensor), V_{CC}, laser bias (TXB), laser power (TXP), and receive power (RSSIC for coarse, RSSIF for fine) using an analog multiplexer to measure them using a round-robin scheme with a single ADC (see the *ADC Timing* section). The voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to a default value (Table 2). Additionally, TXB, TXP, RSSIC, and RSSIF can right-shift results as described in the *Right-Shifting ADC Result* section. This allows customers with specified ADC ranges to calibrate the ADC input gain by a factor of 2^n to measure small signals (thereby reducing the full scale by a factor of 2^n). The DS1886 can then right-shift the results by n bits (effectively multiplying by a factor of $1/2^n$) to maintain the bit weight of their specification. See the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual Range Functionality)* sections for more information.

Alarms and Warnings

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms and/or warnings are set, which can be programmed to create the internal signal TXFINT. The status of TXFINT can be read in A2h Lower Memory, Register 71h. TXFINT is one of the signals used to trigger TXFOUT. TXFOUT can be programmed to cause TXDOUT outputs. These ADC thresholds are user-programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXFOUT and TXDOUT outputs.

ADC Timing

Five analog channels are digitized in a round-robin fashion in the order as shown in Figure 2. RSSI is measured twice to obtain coarse and fine measurements (RSSIC and RSSIF, respectively). The total time required to convert all channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* table for details). After each TXMON conversion, a 3-wire communication is initiated to toggle the MON_SEL bit (bit 6 in the MAX3710's TXCTRL2 register, programmed through A2h Table 02h, Register E5h, bit 6). This causes the laser driver to alternate sending laser bias (TXB) and laser power (TXP) signals to the DS1886's TXMON input.

The DS1886 has a burst mode option to allow internal calculation of TXP using the MD0 and MD1 register values read from the MAX3710 over the 3-wire interface. In this option, the sampled TXP value is ignored.

The TXP value in this burst mode is calculated as follows:

$$TXP = \frac{(MD0\ REGH\ [7:0] + 8 \times MD1\ REGH\ [7:0])}{TXP\ Scale} \times 65536$$

TXP is then right-shifted (Figure 1a).

$RIGHT\text{-}SHIFT_1$ is determined by KIMD[1:0], TXCTRL3[4:3] as follows:

KIMD[1:0] TXCTRL3[4:3]	NO. OF RIGHT-SHIFTS
00	2
01	1
10	0
11	0

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFFh	-128	8000h
V_{CC} (V)	6.5528	FFF8h	0	0000h
TXB, TXP, RSSIC, RSSIF (V)	2.4997	FFF8h	0	0000h

RIGHT-SHIFT$_2$ is determined by KRMD[1:0], TXCTRL3[2:1] as follows:

KRMD[1:0] TXCTRL3[4:3]	NO. OF RIGHT-SHIFTS
00	2
01	1
10	0
11	0

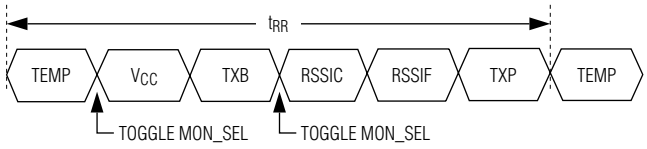
Right-Shifting ADC Result

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (A2h Table 02h, Register 8Eh and A2h Table 02h, Register 8Fh) in EEPROM. TXB, TXP, RSSIC, and RSSIF have 3 bits allocated to set the number of right-shifts. The user must calibrate the corresponding monitors to achieve the correct LSB weighting. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–69h). This is true during the setup of internal calibration as well as during subsequent data conversions.

In burst mode, right-shifting for TXP is determined by KIMD and KRMD.

Differential RSSI Input

The DS1886 offers a fully differential input for RSSI that enables high-side monitoring of RSSI, as shown in Figure 3. This reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.



NOTE: IF VCC LO ALARM OR WARNING IS ENABLED AT POWER-UP, THE ADC ROUND-ROBIN TIMING CYCLES BETWEEN TEMPERATURE AND V_{CC} ONLY UNTIL V_{CC} IS ABOVE THE VCC LO ALARM THRESHOLD.

Figure 2. ADC Round-Robin Timing

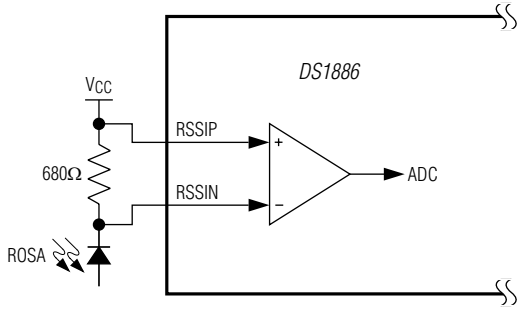


Figure 3. RSSI Differential Input for High-Side RSSI

Laser Bias and Laser Power Through TXMON

The DS1886 measures both laser bias (TXB) and laser power (TXP) through the same input pin, TXMON. The DS1886 commands the MAX3710 laser driver to output the correct monitor signal before each ADC conversions takes place. Figure 4 shows the two conversion paths. Each path has independent gain and offset calibration registers.

Enhanced RSSI Monitoring (Dual Range Functionality)

The DS1886 offers a feature to improve the accuracy and range of RSSI, which is most commonly used for monitoring RSSI. To achieve the SFF-8472 requirement of 0.1µW/LSB over -40 to 8.2dBm, the DS1886 makes two measurements to effectively achieve a 16-bit conversion with a 13-bit physical ADC. This “dual range” calibration can operate in two modes: APD mode and PIN mode.

APD Mode

For systems with a nonlinear relationship between the ADC input and desired ADC result, the mode should be set to APD mode (Figure 5). The RSSI measurement of an APD receiver is one such application. Using the APD mode allows a piece-wise linear approximation of the nonlinear response of the APD’s gain factor. The crossover point is the point between fine and coarse points. The ADC result transitions between the fine and coarse ranges with no hysteresis. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. Two registers, XOVER FINE and XOVER COARSE, determine the crossover point. The XOVER FINE register (A2h Table 02h, Register A0h–A1h) determines the maximum results returned by fine ADC conversions, before right-shifting. The XOVER COARSE register (A2h Table 02h, Register 90h–91h) determines the minimum results returned by coarse ADC conversions, before right-shifting.

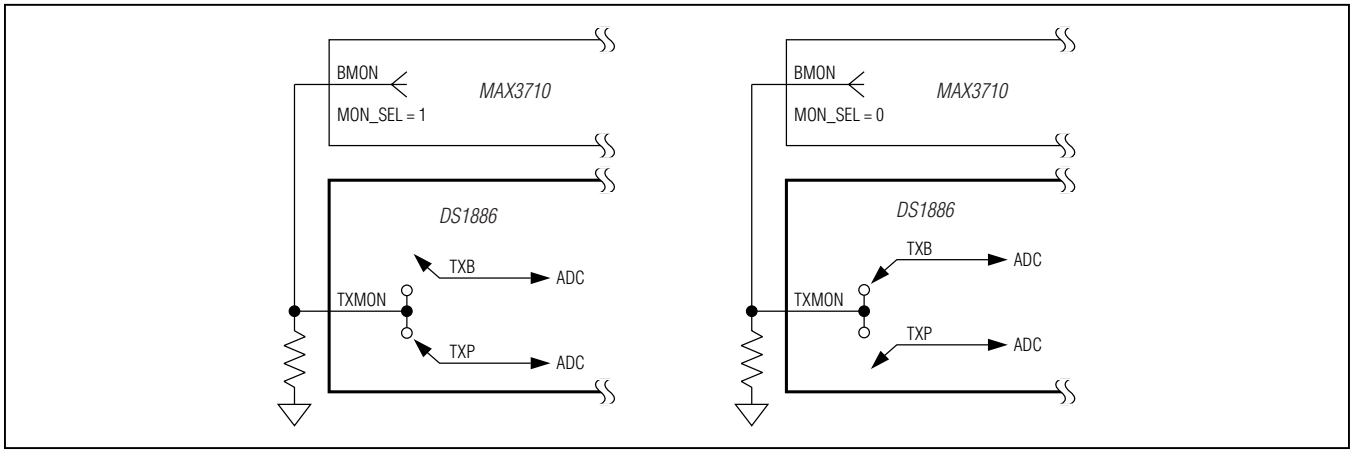


Figure 4. Laser Bias (TXB) and Laser Power (TXP) Monitoring Through TXMON

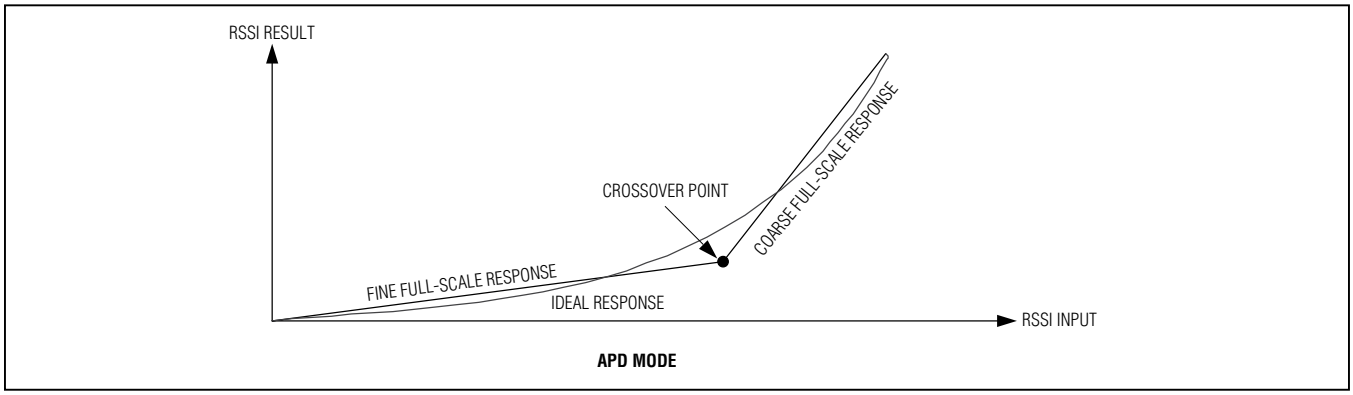


Figure 5. RSSI in APD Mode

PIN Mode

The PIN mode is intended for systems with a linear relationship between the RSSI input and desired ADC result. The ADC result transitions between the fine and coarse ranges with hysteresis, as shown in Figure 6.

In PIN mode, the thresholds between coarse and fine mode are a function of the number of right-shifts being used. With the use of right-shifting, the fine mode full scale is programmed to ($1/2^{nth}$) of the coarse mode full scale. The DS1886 now auto ranges to choose the range that gives the best resolution for the measurement. Table 3 shows the threshold values for each possible number of right-shifts.

Low-Voltage Operation

The DS1886 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM locations are zero, and all analog

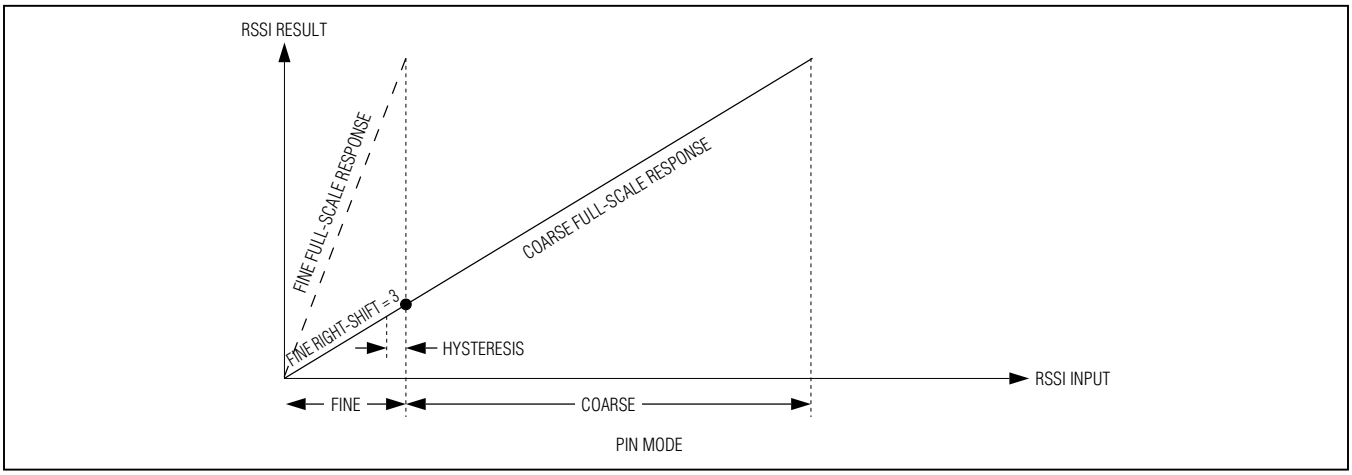


Figure 6. RSSI in PIN Mode

Table 3. RSSI Hysteresis Threshold Values

# OF RIGHT-SHIFTS	FINE MODE MAX (HEX)	COARSE MODE MIN* (HEX)
0	FFF8h	F000h
1	7FFCh	7800h
2	3FFEh	3C00h
3	1FFFh	1E00h
4	0FFFh	0F00h
5	07FFh	0780h
6	03FFh	03C0h
7	01FFh	01E0h

**This is the minimum reported coarse mode conversion.*

Table 4. RSSI Configuration Registers

REGISTER	FINE MODE	COARSE MODE
Gain Register (RSSI FINE/COARSE SCALE)	98h–99h, A2h Table 02h	9Ch–9Dh, A2h Table 02h
Offset Register (RSSI FINE/COARSE OFFEST)	A8h–A9h, A2h Table 02h	ACh–ADh, A2h Table 02h
$RIGHT\text{-}SHIFT_1$ Register	8Eh, A2h Table 02h	N/A
RSSIC and RSSIF Bits ($RIGHT\text{-}SHIFT_0$)	8Fh, A2h Table 02h	
RSSIR Bit (UPDATE)	6Fh, A2h Lower Memory	
RSSI Measurement (RSSI VALUE)	68h–69h, A2h Lower Memory	

circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs are disabled. If the supply voltage recovers back above POA, the device immediately resumes normal operation. If the supply voltage falls below POD, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} next exceeds POA. Figure 7 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS byte (A2h Lower Memory, Register 6Eh). RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (A2h Table 02h, Register 8Ch), the default DEVICE ADDRESS is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1886 in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} low ADC limit. This allows a programmable limit to ensure that the head room requirements of the transceiver are satisfied during a slow power-up. The TXFOUT output does not latch until there is a conversion above the V_{CC} low limit. The POA alarm is nonmaskable. See the *Low-Voltage Operation* section for more information.

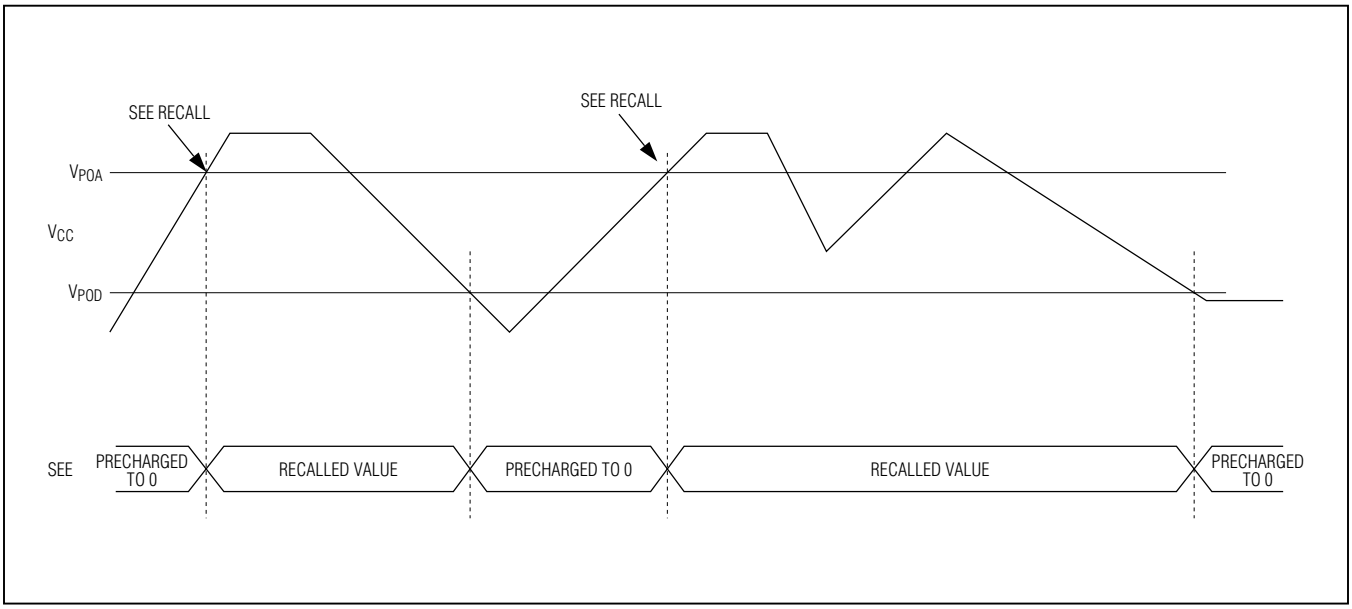


Figure 7. Low-Voltage Hysteresis Example

Delta-Sigma Output and Reference

One delta-sigma output (DAC) is provided. This provides a 10-bit resolution output. The maximum voltage output is set by the input REFIN. An inexpensive shunt reference is recommended to generate the voltage applied to REFIN, as shown in Figure 8. The output includes the ability to compensate the APD bias for temperature as given by the following formula:

DAC_INT = TINDEX[6:0] + DAC OFFSET

If INV_DAC = 0, then DAC[9:0] = DAC_INT/DACFS x V_{REFIN}.

If INV_DAC = 1, then DAC[9:0] = [3FF - (DAC_INT/DACFS)] x V_{REFIN}.

where:

1) INV_DAC is at A2h Table 02h, Register 8Dh, bit 7.
2) TINDEX is at A2h Table 02h, Register 81h.
3) DAC OFFSET is an 8-bit value, representing the 8 MSBs of a 10-bit value. The two LSBs are 0.
4) DACFS (A2h Table 02h, Register 88h) is an 8-bit value, representing the 8 MSBs of a 10-bit value. The two LSBs are 0.
5) DAC is a 10-bit value.
6) The DAC[9:0] is clamped at DACFS.
7) DAC_INT is an internal signal.

The delta-sigma output uses pulse-density modulation. It provides much lower output ripple than a standard digital PWM output given the same clock rate and filter components. An RC filter is required on the DAC output as suggested in Figure 8. The external RC filter components are chosen based on ripple requirements, output load, delta sigma frequency, and desired response time. Before t_{INIT}, the DAC output is high impedance.

The reference input, REFIN, is the supply voltage for the DAC's output buffer. The voltage source connected to REFIN must be able to support the edge rate requirements of the delta sigma outputs. In a typical application, a 0.1uF capacitor should be connected between REFIN and ground.

The DS1886's delta-sigma output is 10 bits. For illustrative purposes, a 3-bit example is provided in Figure 9.

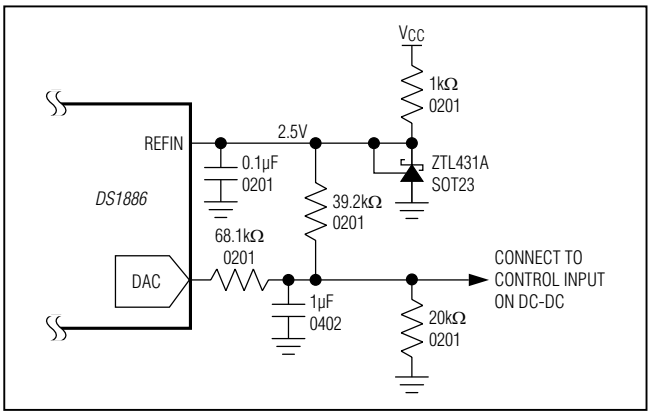


Figure 8. Recommended Shunt Reference and RC Filter for DAC Output

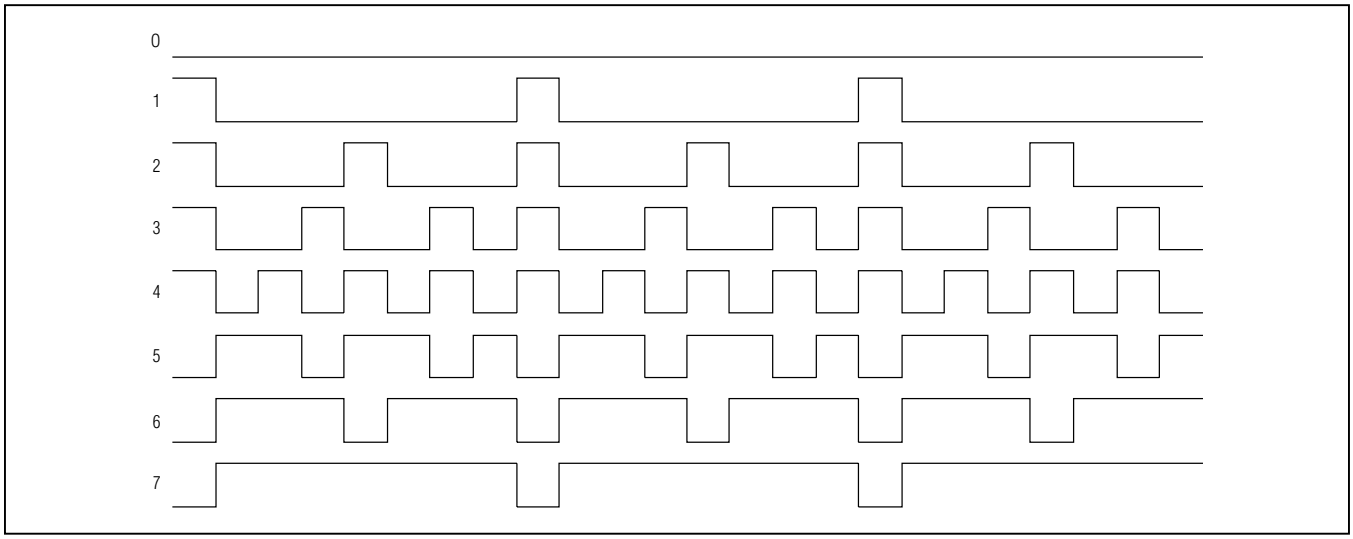


Figure 9. Delta-Sigma Output

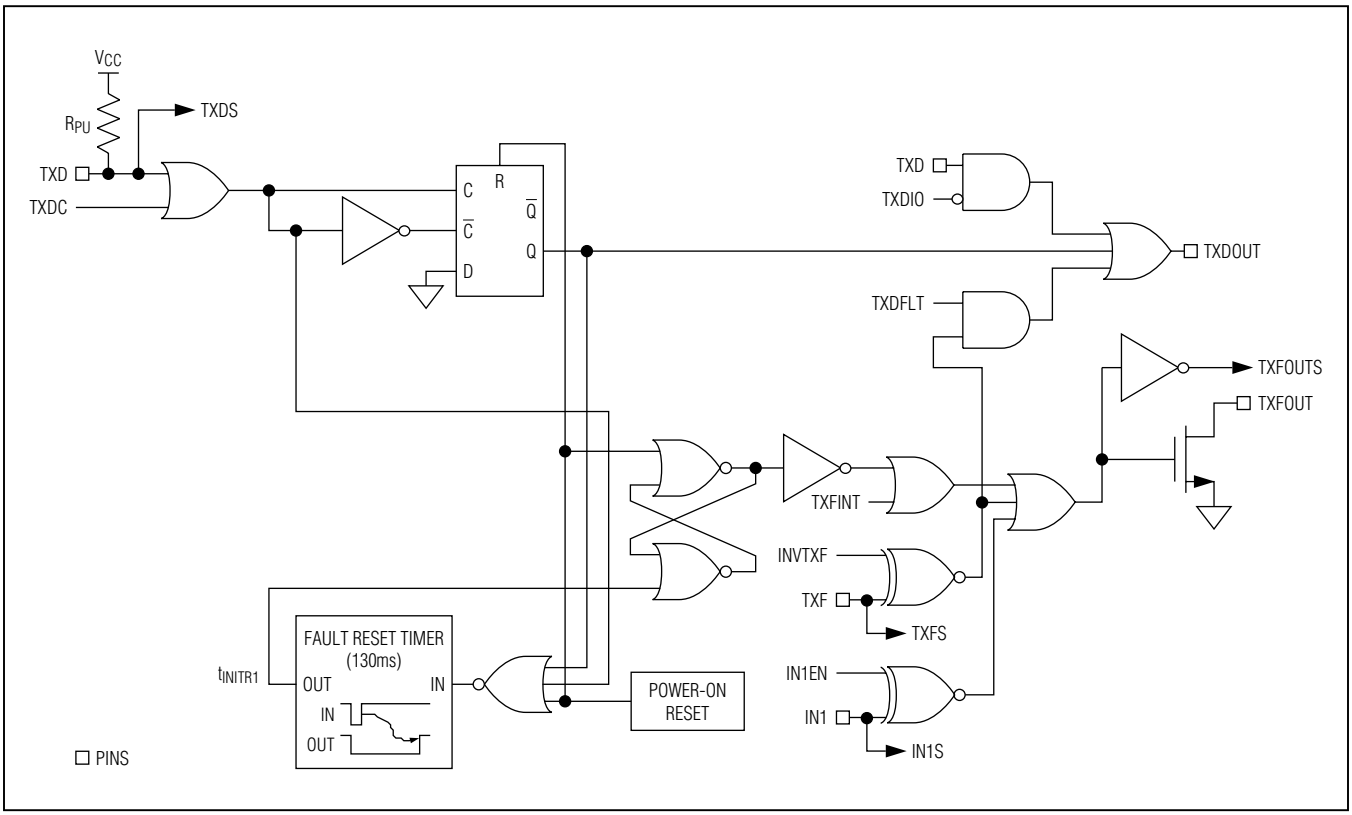


Figure 10. TXFOUT and TXDOUT Logic Diagram.

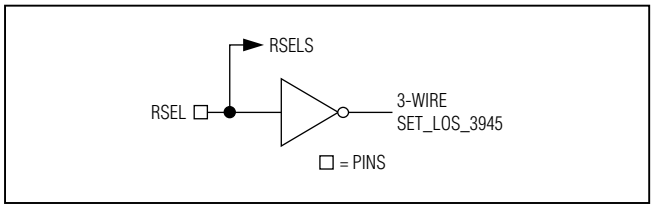


Figure 11. RSEL Logic Diagram

Digital I/O Pins

Five digital inputs and three digital output pins are provided for monitoring and control.

LOS, LOSOUT

By default, the LOS pin is used to convert a standard comparator output for loss of signal (LOS) to an open-collector output (LOSOUT). The status of LOS can be read in the STATUS byte (A2h Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INV LOS = 1) before driving the open drain output transistor.

RSEL

The level of RSEL can be read by reading the STATUS register (A2h Lower Memory, Register 6Eh). The status of RSEL determines whether SETLOSL or SETLOSH is written to the MAX3945 register SET_LOS.

TXD, TXDOUT

TXDOUT is generated from a combination of TXFOUT and TXD (see the CNFGC register A2h Table 02h, Register 8Bh for enabling these options). A software control identical to TXD is available (TXDC, A2h Lower Memory, Register 6Eh). A TXD pulse is internally extended (t_{INITR1}) to inhibit the latching of low alarms and warnings. The intended use is a direct connection to the MAX3710's DISABLE input if this is desired. When V_{CC} < POA, TXDOUT is high impedance.

IN1, TXF, Transmit Fault (TXFOUT) Output

TXFOUT can be triggered by all alarms and warnings and also the pins TXF and IN1 (Figure 10). The ADC alarms and warnings require enabling (A2h Table 01h/05h, Registers

F8h and FDh). See Figure 12a and Figure 12b for non-latched and latched operation. Figure 12c describes this TXFOUT behavior during power-on. Latching of the alarms is controlled by CNFGB and CNFGC Registers (A2h Table 02h, Register 8Ah and A2h Table 02h, Register 8Bh).

The DS1886 monitors the IMODOVFL and IBIASOVFL bits in the MAX3710 DPCSTAT register. If any of these bits is set, the user can optionally cause TXFOUT to be set. A mask bit, BIASMODOVFL_FLT in A2h Table 02h, Register 8Bh, must be set to enable this functionality.

Die Identification

The DS1886 has an ID hardcoded in its die. Two registers (DEVICE ID A2h Table 02h, Register CEh and DEVICE VER A2h Table 02h, Register CFh) are assigned for this feature. Register CEh reads 84h to identify with the device as the DS186, and Register CFh reads the present device version.

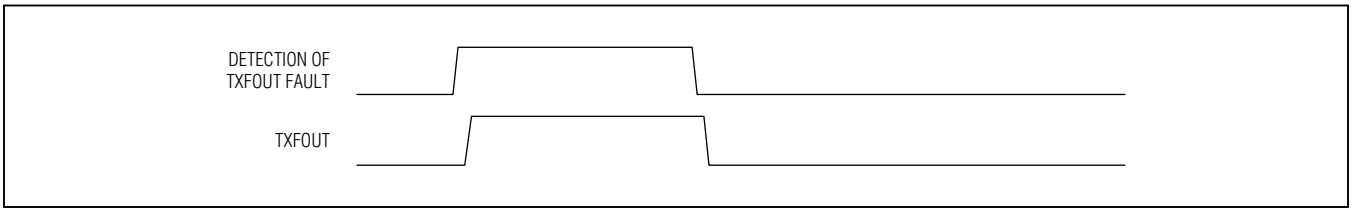


Figure 12a. TXFOUT Nonlatched Operation

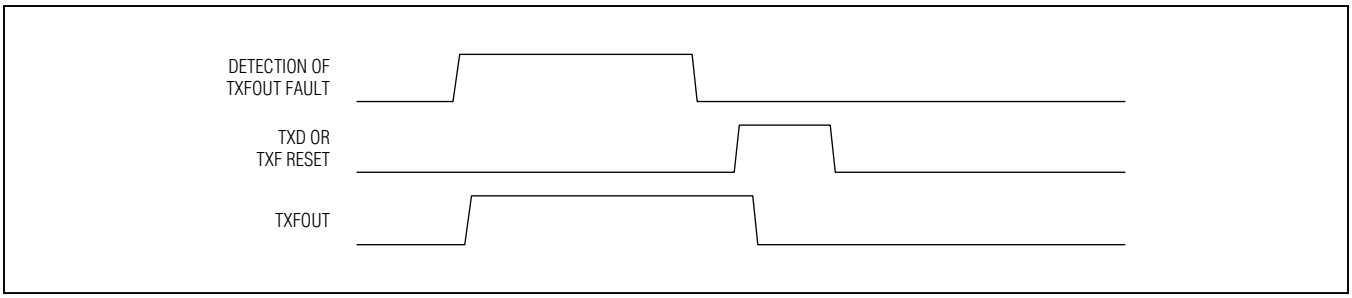


Figure 12b. TXFOUT Latched

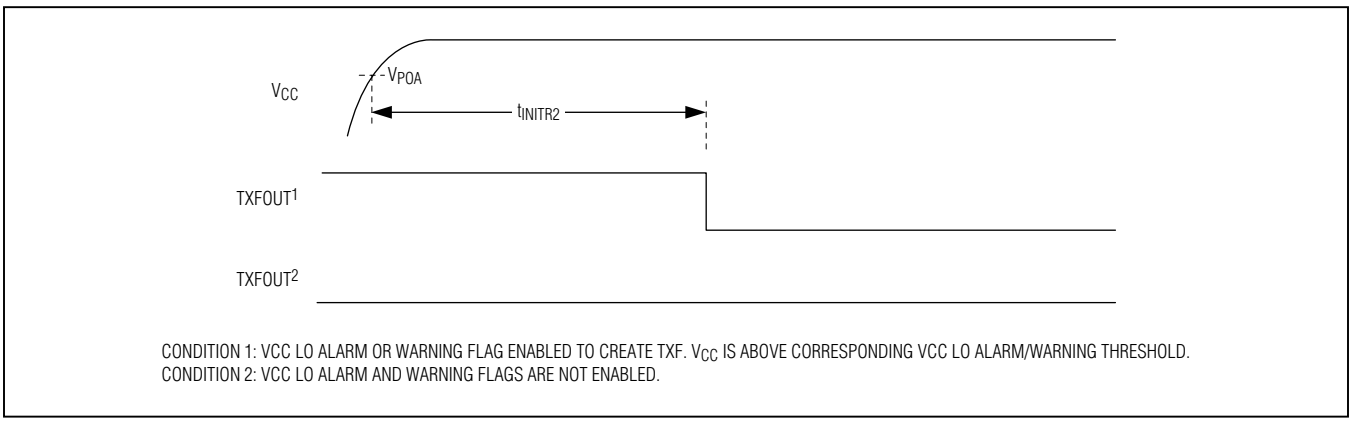


Figure 12c. TXFOUT During Power-On

DS1886 Master Communication Interface

The DS1886 controls the MAX3710 using a proprietary 3-wire interface. The DS1886 configures the MAX3710 on startup and then continuously updates the MAX3710 with new LUT values. The DS1886 operates in one of three modes: open loop, APC loop, and dual closed loop. The DS1886 can also configure the MAX3945 on startup. The communication between the DS1886 and the MAX3710 and MAX3945 is transparent to the end user. In addition, commands can be issued to the MAX3710 and MAX3945 using the DS1886's manual mode.

3-Wire Master Interface

The DS1886 acts as the master, initiating communication with and generating the clock for the Maxim slave device(s). It is a 3-pin interface consisting of SDAOUT, a bidirectional data line; clock signal SCLOUT; and CSEL1OUT chip-select output (active high). A second, independent chip select (CSEL2OUT) is provided for use with the MAX3945.

Protocol

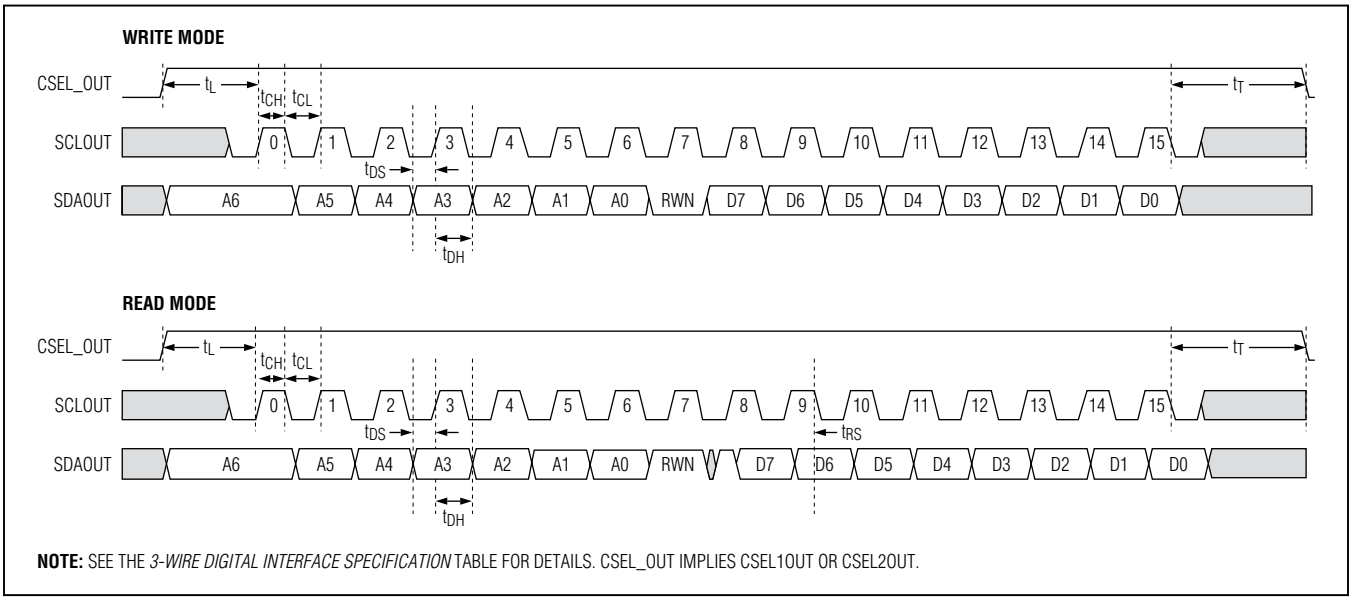
The DS1886 initiates a data transfer by asserting the CSEL1OUT or CSEL2OUT pin. It then starts to generate a clock signal after CSEL1OUT or CSEL2OUT has been set to 1. Each operation consists of 16 bit transfers (15-bit address/data, 1-bit RWN). All data transfers are MSB first.

Write Mode (RWN = 0): The master generates 16 clock cycles at SCLOUT in total. It outputs 16 bits (MSB first) to the SDAOUT line at the falling edge of the clock. The master closes the transmission by setting CSEL1OUT and CSEL2OUT to 0.

Read Mode (RWN = 1): The master generates 16 clock cycles at SCLOUT in total. It outputs 8 bits (MSB first) to the SDAOUT line at the falling edge of the clock. The SDAOUT line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at rising edge of the clock. The master samples SDAOUT at the falling edge of SCLOUT. The master closes the transmission by setting the CSEL1OUT and CSEL2OUT to 0.

Table 5. 3-Wire Transaction Detail

BIT	NAME	DESCRIPTION
15:9	Address	7-bit internal register address
8	RWN	0: write, 1: read
7:0	Data	8-bit read or write data



NOTE: SEE THE *3-WIRE DIGITAL INTERFACE SPECIFICATION* TABLE FOR DETAILS. CSEL_OUT IMPLIES CSEL1OUT OR CSEL2OUT.

Figure 13. 3-Wire Interface Timing Diagram

3-Wire Slave Register Map and DS1886 Corresponding Location

When the MAX3945 registers are written, the MAX3710 are also written simultaneously (Table 6).

3-Wire Master Flowchart

Figure 14 explains the working of the 3-wire master in the DS1886 in all three opreating modes. These modes are described in the *DS1886 with MAX3710 Operating Modes* section.

Table 6. 3-Wire Register Map and DS1886 Corresponding Location

DS1886 REGISTER (A2h TABLE 02h)	DS1886 REGISTER NAME	MAX3710 ADDRESS	MAX3710 REGISTER NAME	MAX3945 ADDRESS	MAX3945 REGISTER NAME
82h–83h	MODULATION VALUE	0Eh	SET_IMOD	N/A	N/A
85h	APC VALUE	11h	SET_2XAPC	N/A	N/A
86h–87h	SET_BIAS VALUE	0Dh	SET_IBIAS	N/A	N/A
CAh	INCBYTE[7:4]	0Fh	BIASINC	N/A	N/A
CAh	INCBYTE[3:0]	10h	MODINC	N/A	N/A
CBh	TXCTRL5 DPC	0Ah	TXCTRL5	N/A	N/A
CCh	IMODMAX	0Ch	IMODMAX	N/A	N/A
CDh	IBIASMAX	0Bh	IBIASMAX	N/A	N/A
E0h	RXCTRL1	01h	RXCTRL1	00h	RXCTRL1
E1h	RXCTRL2	02h	RXCTRL2	01h	RXCTRL2
E2h	SETCML	03h	SET_CML	03h	SET_CML
E3h	SETLOSH	04h	SET_LOS	N/A	N/A
E4h	TXCTRL1	06h	TXCTRL1	N/A	N/A
E5h	TXCTRL2	07h	TXCTRL2	N/A	N/A
E6h	TXCTRL3	08h	TXCTRL3	N/A	N/A
E7h	TXCTRL4	09h	TXCTRL4	N/A	N/A
E8h	TXCTRL5 APC OL	0Ah	TXCTRL5	N/A	N/A
E9h	TXCTRL6	13h	TXCTRL6	N/A	N/A
EAh	TXCTRL7	05h	TXCFG	N/A	N/A
ECh	SETLOSH_3945	N/A	N/A	04h	SET_LOS
EDh	SETLOSL_3945	N/A	N/A	04h	SET_LOS
EEh	SETLOSTIMER_3945	N/A	N/A	12h	SET_LOSTIMER
F0h	3WCTRL	Manual control of read/write from/to 3-wire slave devices; useful for determining correct settings for the slave devices and also for debugging.			
F1h	ADDRESS				
F2h	WRITE				
F3h	READ				
F4h	TXSTAT2	1Fh	TXSTAT2	N/A	N/A
F5h	TXSTAT1	1Eh	TXSTA1	N/A	N/A
F6h	DPCSTAT	1Dh	DPCSTAT	N/A	N/A
F7h	RXSTAT	1Ch	RXSTAT	N/A	N/A

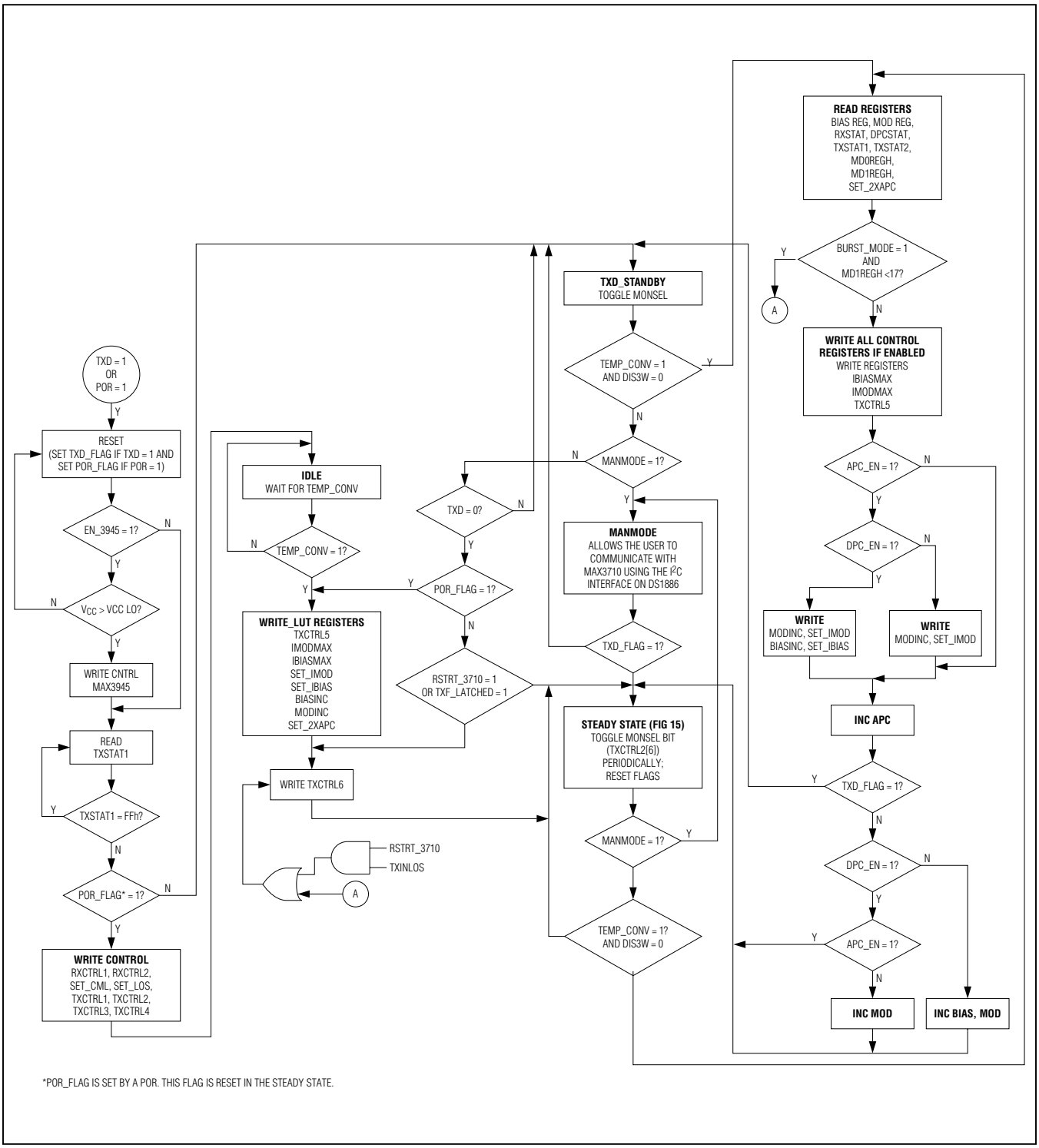
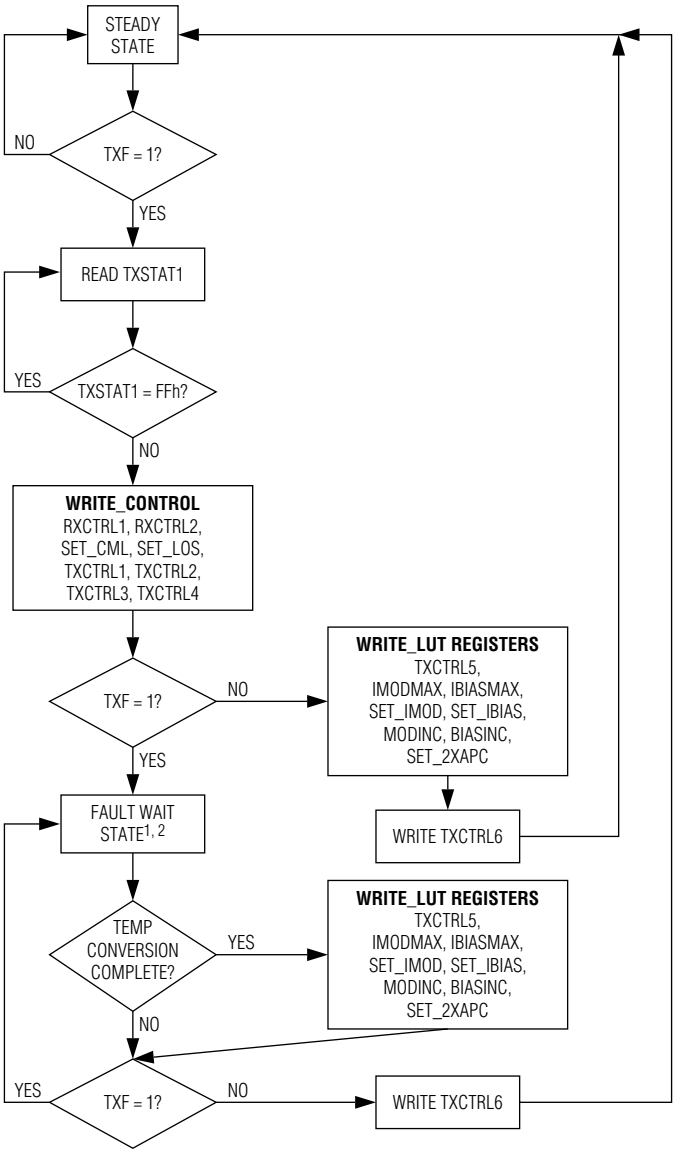


Figure 14. 3-Wire Flowchart



NOTE 1: FAULT WAIT STATE HAS ACCESS TO MAX3710 IN MANUAL MODE.
NOTE 2: MON_SEL BIT IS TOGGLED AS NEEDED TO KEEP THE TXP/TXB MONITORS CORRECT.

Figure 15. MAX3710 Brownout Detection Flowchart

3-Wire Power-On Reset

The DS1886 detects whether a power-on reset has occured on the slave 3-wire device. This is done using the flowchart shown in Figure 15.

DS1886 with MAX3710 Operating Modes

The user has the option of selecting among open loop, APC loop, and dual closed-loop operation modes. These can be programmed using the DPC_EN and APC_EN bits in the MAX3710 TXCTRL3 register (Address H0x08), programmed through A2h Table 02h, Register E6h. Table 7 indicates what the values in each LUT corresponds to in each of the modes. LUT values are not automatically updated when changing between operating modes.

Open Loop Mode, DPC_EN = 0, APC_EN = 0

In open loop mode, the laser bias and modulation are both controlled using LUTs. Each LUT consists of an 8-bit LUT with up to 2°C temperature resolution and an 8-bit offset LUT. This allows the DS1886 to fully support the 10-bit bias DAC and 9-bit modulation DAC inside the MAX3710.

APC Loop Mode, DPC_EN = 0, APC_EN = 1

In APC loop or single closed-loop mode, the laser bias is controlled by an APC loop, while the modulation is controlled using a temperature-indexed LUT. The APC setpoint is controlled using an LUT having up to 16°C resolution. The APC loop initial value (SET_IBIAS) is set using an LUT having up to 2°C resolution. The modulation LUT consists of an 8-bit LUT with up to 2°C temperature resolution and an 8-bit offset LUT. This allows the DS1886 to fully support the 10-bit bias DAC and 9-bit modulation DAC inside the MAX3710.

Dual Closed-Loop Mode, DPC_EN = 1, APC_EN = 1

In dual closed-loop mode, the laser bias is controlled by an APC loop, while the modulation is controlled with an extinction ratio loop. The APC setpoint and extinction ratio setpoints are controlled using 8-bit LUTs with up to 2°C temperature resolution and 8-bit offset LUTs. Each loop is initialized using 8-byte LUTs.

Table 7. DS1886 LUT Functions in Open Loop, APC Loop, and Dual Closed-Loop Modes

TABLE	REGISTER	OPEN LOOP	APC LOOP	DUAL CLOSED LOOP
04h	80h–A7h	8-Bit Modulation Value [7:0]	8-Bit Modulation Value [7:0]	8-Bit TXCTRL5[7:0]
	F0h–F7h	IMODMAX[8:1]	IMODMAX[8:1]	IMODMAX[8:1]
	F8h–FFh	Modulation Offset [9:2]	Modulation Offset [9:2]	SET_IMOD[8:1] (MOD Initial Value)
06h	80h–A7h	8-Bit BIAS Value [7:0]	8-Bit SET_IBIAS [9:2]	8-Bit SET_IBIAS [9:2]
	F0h–F7h	IBIASMAX[9:2]	IBIASMAX[9:2]	IBIASMAX[9:2]
	F8h–FFh	BIAS Offset [9:2]	8-Bit APC Value [7:0]	8-Bit APC Value [7:0]
08h	F8h–FFh	INCBYTE (set to all zeros)	INCBYTE 7:4 = BIASINC 3:0 = MODINC (set to all zeros)	INCBYTE 7:4 = BIASINC 3:0 = MODINC

BIAS, MODULATION, SET_2XAPC, TXCTRL5 LUTs

LUTs allow temperature indexing the BIAS and MODULATION values and their respective offsets. Depending on the operation mode (see the *DS1886 with MAX3710 Operating Modes* section), the LUTs function differently, as indicated in Table 7.

The LUTs have nonlinear temperature indexing. After every temperature conversion, based on the internal temperature read, a TINDEX value is calculated, which then indexes the LUT. The LUTs can index with a resolution as low as 2°C.

This is illustrated in Table 8 and Table 9. BIAS, MODULATION and TXCTRL5 are 5-row LUTs. Further details can be found in the LUT descriptions.

Table 8. DS1886 LUT Memory Map for 5-Row Table (Temperature Values Indicated in °C)

ROW	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
80h	-40	-32	-24	-16	-8	0	+8	+16
88h	+24	+28	+32	+36	+40	+44	+48	+52
90h	+56	+58	+60	+62	+64	+66	+68	+70
98h	+72	+74	+76	+78	+80	+82	+84	+86
A0h	+88	+90	+92	+94	+96	+98	+100	+102

Table 9. DS1886 LUT Memory Map for 5-Row Table (TINDEX Values Indicated in Hex)

ROW	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
80h	80	84	88	8C	90	94	98	9C
88h	A0	A2	A4	A6	A8	AA	AC	AE
90h	B0	B1	B2	B3	B4	B5	B6	B7
98h	B8	B9	BA	BB	BC	BD	BE	BF
A0h	C0	C1	C2	C3	C4	C5	C6	C7

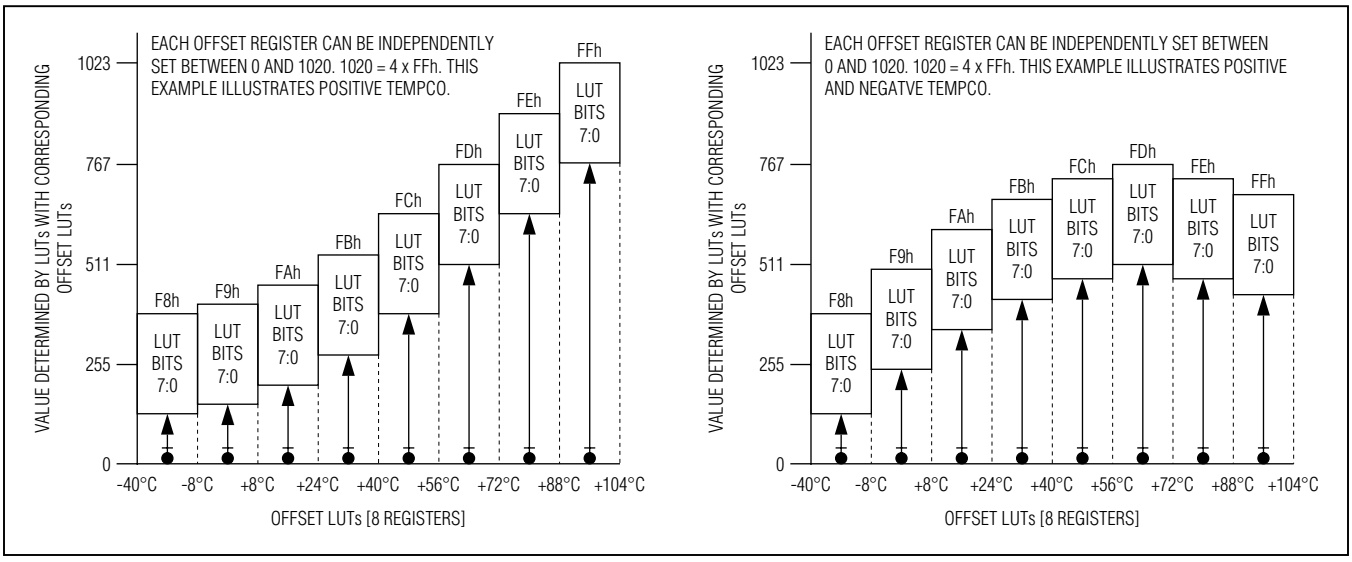
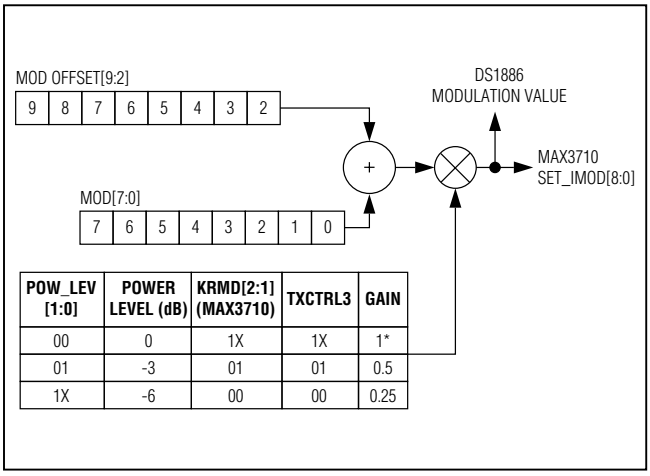


Figure 16. Offset LUT



POW_LEV [1:0]	POWER LEVEL (dB)	KRMD[2:1] (MAX3710)	TXCTRL3	GAIN
00	0	1X	1X	1*
01	-3	01	01	0.5
1X	-6	00	00	0.25

Figure 17. MODULATION LUT (Open Loop and APC Mode)

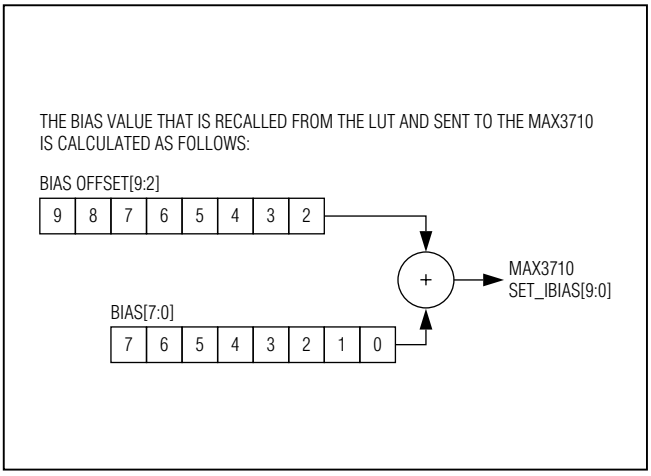


Figure 18. BIAS LUT (Open Loop)

Table 10. Temperature Resolution for Offsets

ROW	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
F8h	-40°C	-8°C	+8°C	+24°C	+40°C	+56°C	+72°C	+88°C

The offsets are also temperature indexed. Figure 16 illustrates how the offsets would affect the final output as the temperature varies.

Table 10 shows the temperature resolution for the offsets.

MODULATION Value

Figure 17 shows how to calculate the MODULATION value that is recalled from the LUT and sent to the MAX3710.

BIAS Value

Figure 18 shows how to calculate the BIAS value that is recalled from the LUT and sent to the MAX3710.

Table 11a. Power Leveling Details (when DS1863_MODE = 0, default)

POWER LEVEL (dB)	POW_LEV[1:0] (REGISTER 6Fh)	MODULATION CHANGE	KRMD[2:1] (MAX3710)	TXCTRL3 POW_LEV_INIT
0	00	None	1X	1X
-3	01	Right-shift SET_IMOD once	01	01
-6	1X	Right-shift SET_IMOD twice	00	00

Table 11b. Power Leveling Details (when DS1863_MODE = 1)

POWER LEVEL (dB)	POW_LEV_DS1863[2:0] (REGISTER 8Ch)	MODULATION CHANGE	KRMD[2:1] (MAX3710)
0	000–010	None	1X
-3	011–110	Right-shift SET_IMOD once	01
-6	111	Right-shift SET_IMOD twice	00

Power Leveling

The DS1886 supports power leveling as described in G.984.2. The POW_LEV[1:0] bits in UPDATE A2h Lower Memory, Register 6Fh allow for three power level settings: 0dB, -3dB, and -6dB. Depending on the operation mode, a combination of SET_IMOD and the KRMD bits (MAX3710 TXCTRL3 register) are adjusted to meet these power-level settings. The KRMD bits adjust the gain of the APC loop and extinction ratio loop. See Table 11a and Table 11b.

Manual MAX3710 Operations

The master interface is controllable using four registers in the DS1886: 3WCTRL, ADDRESS, WRITE, READ. Commands can be manually issued while the DS1886 is in normal operation mode. It is also possible to suspend normal 3-wire commands so that only manual operation commands are sent (3WCTRL, A2h Table 04h, Register F8h–FFh).

I²C Communication

I²C Definition

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 19 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 19 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 19 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 19). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during

a bit read (Figure 19). The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 19). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1886 responds to two slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. The Lower Memory and Tables 00h–08h respond to I²C slave addresses that can be configured to any value between 00h–FEh using the DEVICE ADDRESS byte (A2h Table 02h, Register 8Ch). The user also must set the ASEL bit (A2h Table 02h, Register 89h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates that it would write data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the device assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent. If the main device's slave address is programmed to be A0h, access to the auxiliary memory is disabled.

Memory Address: During an I²C write operation to the device, the master must transmit a memory address to identify the memory location where the slave is to store

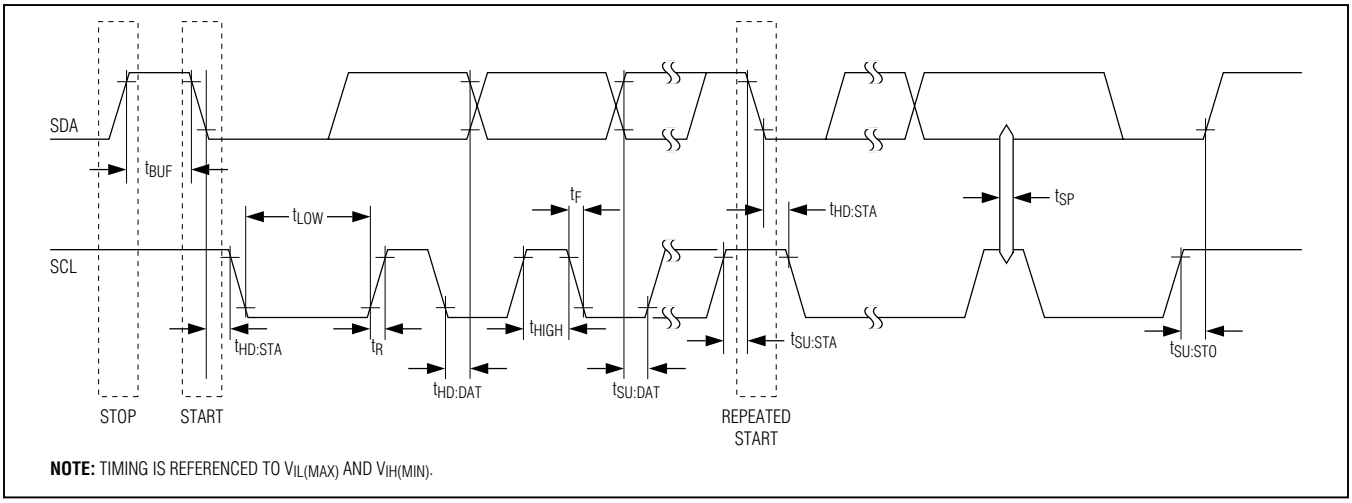


Figure 19. I²C Timing Diagram

the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

See Figure 20 for an example of I²C timing.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The device writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row.

For example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus free time or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

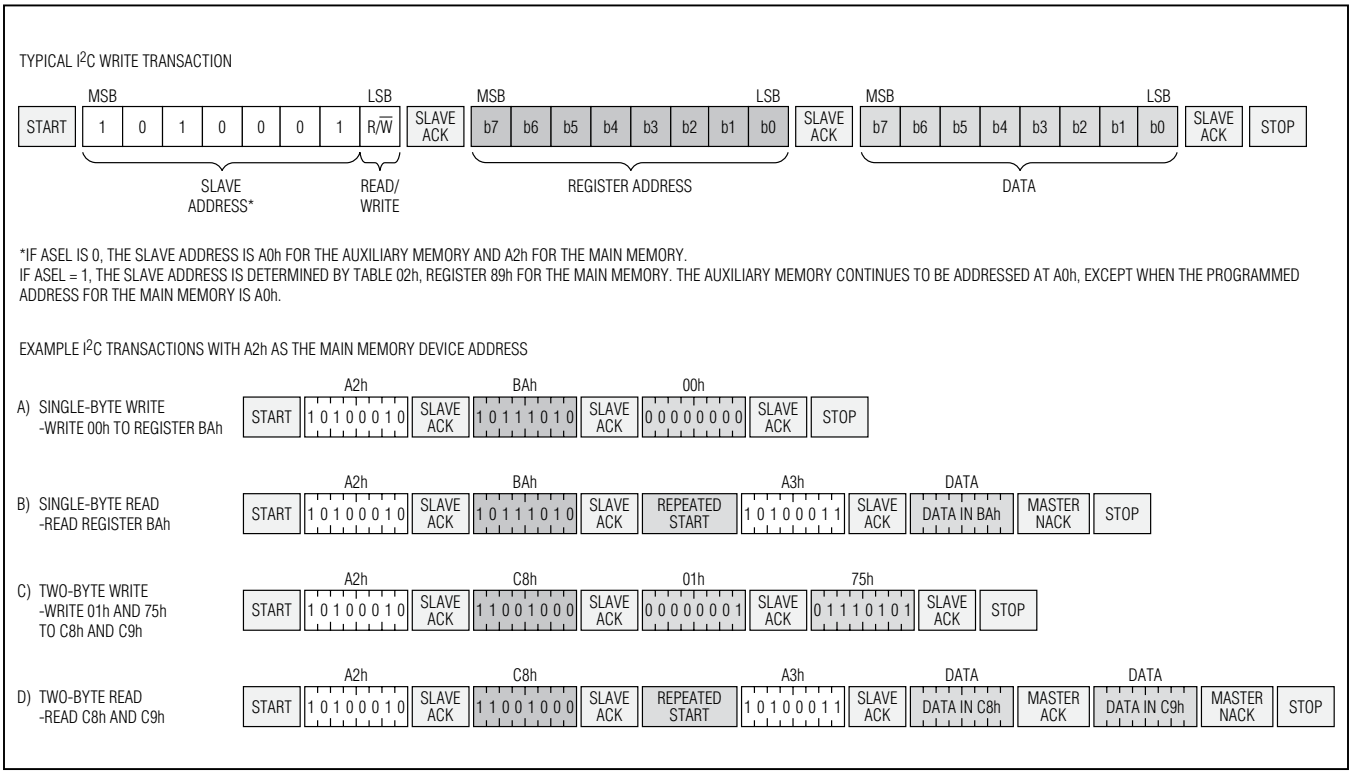


Figure 20. Example I²C Timing

Acknowledge Polling: Any time a EEPROM page is written, the device requires the EEPROM write time (t_W) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the device, which allows the next page to be written as soon as the device is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_W to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur, the device writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page 1 byte at a time wears the EEPROM out 8x faster than writing the entire page at once. The device's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10x that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as a EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Organization

The following sections provide the device's register definitions (see Figure 21 for the memory map). Each register or row of registers has an access descriptor that determines the password level required to read or write the memory. Level 2 password is intended for the module manufacture access only; level 1 password allows another level of protection for items the end consumer may wish to protect. Many registers are always readable, but require password access to write. There are a few registers that cannot be read without password access. The below access codes describe each mode used by the DS1886 with factory setting for the PW_ENA (A2h Table 02h, Register C0h) and PW_ENB (A2h Table 02h, Register C1h) values set to factory settings.

ACCESS CODE	READ ACCESS	WRITE ACCESS
<0>	At least 1 byte/bit in the row/byte is different than the rest of the row/byte, so look at each byte/bit separately for permissions.	
<1>	Read all	Write PW2
<2>	Read all	Write not applicable
<3>	Read all	Write all, but the device hardware also writes to these bytes/bits
<4>	Read PW2	Write PW2 + mode_bit
<5>	Read all	Write all
<6>	Read not applicable	Write all
<7>	Read PW1	Write PW1
<8>	Read PW2	Write PW2
<9>	Read not applicable	Write PW2
<10>	Read PW2	Write not applicable
<11>	Read all	Write PW1

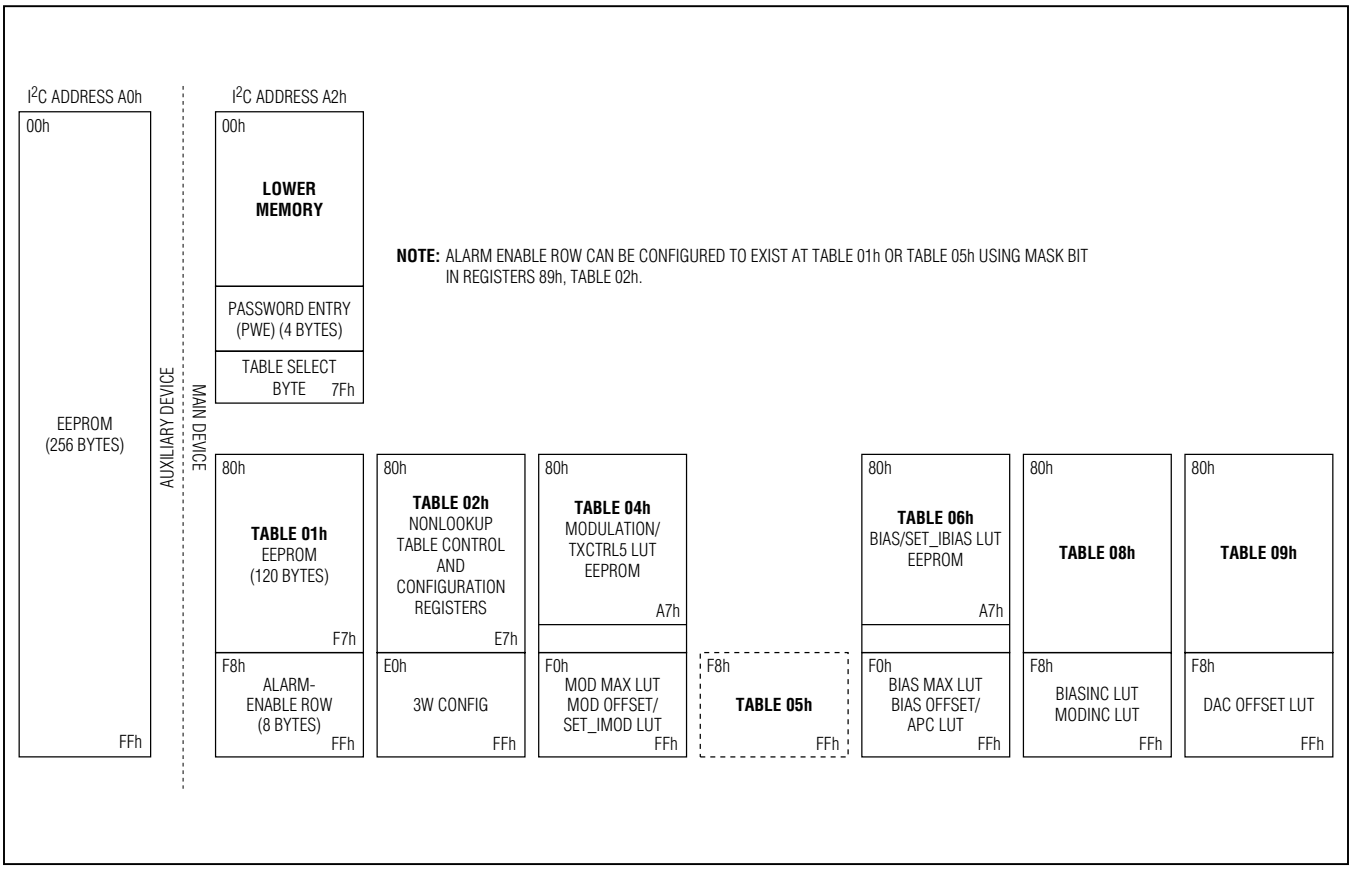


Figure 21. Memory Organization

Register Descriptions

The register maps show each byte/word (2 bytes) in terms of its row in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description.

A2h Lower Memory Register Map

LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1>THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1>THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1>THRESHOLD$_2$	TXB ALARM HI		TXB ALARM LO		TXB WARN HI		TXB WARN LO	
18	<1>THRESHOLD$_3$	TXP ALARM HI		TXP ALARM LO		TXP WARN HI		TXP WARN LO	
20	<1>THRESHOLD$_4$	RSSI ALARM HI		RSSI ALARM LO		RSSI WARN HI		RSSI WARN LO	
28–37	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
38–5F	<1>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
60	<2>ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		TXB VALUE		TXP VALUE	
68	<0>ADC VALUES$_1$	<2>RSSI VALUE		<2>RESERVED		<2>RESERVED		<0>STATUS	<3>UPDATE
70	<5>ALARM/WARN	ALARM$_3$	ALARM$_2$	RESERVED	RESERVED	WARN$_3$	WARN$_2$	RESERVED	RESERVED
78	<0> TABLE SELECT	<5>RESERVED	<5>RESERVED	<5>RESERVED	<6>PWE MSW	<6>PWE MSW	<6>PWE LSW	<6>PWE LSW	<5>TBL SEL

A2h Table 01h Register Map

A2h TABLE 01h									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–BF	<7>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
C0–F7	<8>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
F8	<8>ALARM ENABLE	ALARM EN$_3$	ALARM EN$_2$	RESERVED	RESERVED	WARN EN$_3$	WARN EN$_2$	RESERVED	RESERVED

Note: *The ALARM ENABLE bytes (Registers F8h–FFh) can be configured to exist in A2h Table 05h instead of here at A2h Table 01h with the MASK bit (A2h Table 02h, Register 89h). If the row is configured to exist in A2h Table 05, then these locations are EE in A2h Table 01h.*

The access codes represent the factory default values of PW_ENA (A2h Table 02h, Register C0h) and PW_ENB (A2h Table 02h, Register C1h).

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and device hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

A2h Table 02h Register Map

A2h TABLE 02h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<0>CONFIG$_0$	<8>MODE	<4>TINDEX	<4>MODULATION VALUE		RESERVED	<4>APC VALUE	<4>SET_IBIAS VALUE	
88	<8>CONFIG$_1$	DACFS	CNFGA	CNFGB	CNFGC	RESERVED	CNFGD	RSHIFT$_1$	RSHIFT$_0$
90	<8>SCALE$_0$	XOVER COARSE		V_{CC} SCALE		TXB SCALE		TXP SCALE	
98	<8>SCALE$_1$	RSSI FINE SCALE		RESERVED		RSSI COARSE SCALE		RESERVED	
A0	<8>OFFSET$_0$	XOVER FINE		V_{CC} OFFSET		TXB OFFSET		TXP OFFSET	
A8	<8>OFFSET$_1$	RSSI FINE OFFSET		RESERVED		RSSI COARSE OFFSET		INTERNAL TEMP OFFSET*	
B0	<9>PWD VALUE	PW1 MSW		PW1 LSW		PW2 MSW		PW2 LSW	
B8	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
C0	<8>PWD ENABLE	PW_ENA	PW_ENB	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TBLSELPON
C8	<0>MAXROW	<4>DAC VALUE	<4>DAC VALUE	<4>INCBYTE	<4>TXCTRL5 DPC	<4>IMODMAX	<4>IBIASMAX	<10>DEVICE ID	<10>DEVICE VER
D0–DF	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
E0	<8>3W CONFIG$_0$	RXCTRL1	RXCTRL2	SETCML	SETLOSH	TXCTRL1	TXCTRL2	TXCTRL3	TXCTRL4
E8	<8>3W CONFIG$_1$	TXCTRL5 APC OL	TXCTRL6	TXCTRL7	RESERVED	SETLOSH_3945	SETLOSL_3945	SET_LOS TIMER_3945	3WSET
F0	<0>3W CONFIG$_2$	<8>3WCTRL	<8>ADDRESS	<8>WRITE	<10>READ	<10>TXSTAT2	<10>TXSTAT1	<10>DPCSTAT	<10>RXSTAT
F8	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

**The final result must be XORed with BB40h before writing to this register.*

***Do not write to this register.*

The access codes represent the factory default values of PW_ENA (A2h Table 02h, Register C0h) and PW_ENB (A2h Table 02h, Register C1h).

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and device hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

A2h Table 04h Register Map

A2h TABLE 04h (MODULATION OR TXCTRL5 LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–A7	<8>MODULATION/ TXCTRL5	SEE TABLE DESCRIPTION							
A8–EF	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F0	<8>IMODMAX	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT	MOD MAX LUT
F8	<8>MOD OFFSET/ SET_IMOD LUT	SEE TABLE DESCRIPTION							

A2h Table 05h Register Map

A2h TABLE 05h									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>ALARM ENABLE	ALARM EN_3	ALARM EN_2	RESERVED	RESERVED	WARN EN_3	WARN EN_2	RESERVED	RESERVED

Note: *A2h Table 05h is empty by default. It can be configured to contain the alarm and warning enable bytes from A2h Table 01h, Registers F8h-FFh with the MASK bit enabled (A2h Table 02h, Register 89h). In this case A2h Table 01h will be empty.*

A2h Table 06h Register Map

A2h TABLE 06h (BIAS OR APC LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–A7	<8>BIAS/APC LUT	SEE TABLE DESCRIPTION							
A8–EF	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F0	<8>IBIASMAX	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT	BIAS MAX LUT
F8	<8>BIAS/SET_IBIAS OFF	SEE TABLE DESCRIPTION							

The access codes represent the factory default values of PW_ENA (A2h Table 02h, Register C0h) and PW_ENB (A2h Table 02h, Register C1h).

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and device hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

A2h Table 08h Register Map

A2h TABLE 08h (INC LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8–FF	<8>INCROW	INCBYTE	INCBYTE	INCBYTE	INCBYTE	INCBYTE	INCBYTE	INCBYTE	INCBYTE

A2h Table 09h Register Map

A2h TABLE 09h (DAC OFFSET LUT)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8–FF	<8>DAC OFFSET	DACOFF	DACOFF	DACOFF	DACOFF	DACOFF	DACOFF	DACOFF	DACOFF

Auxiliary A0h Memory Register Map

AUXILIARY MEMORY (A0h)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00–7F	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
80–FF	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE

The access codes represent the factory default values of PW_ENA (A2h Table 02h, Register C0h) and PW_ENB (A2h Table 02h, Register C1h).

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and device hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

A2h Lower Memory Register Descriptions

A2h Lower Memory, Register 00h–01h: TEMP ALARM HI
A2h Lower Memory, Register 04h–05h: TEMP WARN HI

FACTORY DEFAULT	7FFFh
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

00h, 04h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
01h, 05h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates above this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or below this threshold clear its alarm or warning bit.

A2h Lower Memory, Register 02h–03h: TEMP ALARM LO
A2h Lower Memory, Register 06h–07h: TEMP WARN LO

FACTORY DEFAULT	8000h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

02h, 06h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h, 07h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates below this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or above this threshold clear its alarm or warning bit.

A2h Lower Memory, Register 08h–09h: V_{CC} ALARM HI
A2h Lower Memory, Register 0Ch–0Dh: V_{CC} WARN HI
A2h Lower Memory, Register 10h–11h: TXB ALARM HI
A2h Lower Memory, Register 14h–15h: TXB WARN HI
A2h Lower Memory, Register 18h–19h: TXP ALARM HI
A2h Lower Memory, Register 1Ch–1Dh: TXP WARN HI
A2h Lower Memory, Register 20h–21h: RSSI ALARM HI
A2h Lower Memory, Register 24h–25h: RSSI WARN HI

FACTORY DEFAULT	FFFFh
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
08h, 0Ch, 10h,14h, 18h, 1Ch, 20h, 24h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
09h, 0Dh, 11h, 15h, 19h, 1Dh, 21h, 25h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Voltage measurement updates above this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or below this threshold clear its alarm or warning bit.

A2h Lower Memory, Register 0Ah–0Bh: V_{CC} ALARM LO
A2h Lower Memory, Register 0Eh–0Fh: V_{CC} WARN LO
A2h Lower Memory, Register 12h–13h: TXB ALARM LO
A2h Lower Memory, Register 16h–17h: TXB WARN LO
A2h Lower Memory, Register 1Ah–1Bh: TXP ALARM LO
A2h Lower Memory, Register 1Eh–1Fh: TXP WARN LO
A2h Lower Memory, Register 22h–23h: RSSI ALARM LO
A2h Lower Memory, Register 26h–27h: RSSI WARN LO

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
0Ah, 0Eh, 12h, 16h, 1Ah, 1Eh, 22h, 26h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
0Bh, 0Fh, 13h, 17h, 1Bh, 1Fh, 23h, 27h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Voltage measurement updates below this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or above this threshold clear its alarm or warning bit.

A2h Lower Memory, Register 28h–37h: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Lower Memory, Register 38h–5Fh: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (EE)

38h–5Fh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

A2h Lower Memory, Register 60h–61h: TEMP VALUE

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

60h	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
61h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Signed two's complement direct-to-temperature measurement.

A2h Lower Memory, Register 62h–63h: V_{CC} VALUE
A2h Lower Memory, Register 64h–65h: TXB VALUE
A2h Lower Memory, Register 66h–67h: TXP VALUE
A2h Lower Memory, Register 68h–69h: RSSI VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

62h, 64h, 66h, 68h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
63h, 65h, 67h, 69h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Left-justified unsigned voltage measurement.

A2h Lower Memory, Register 6Ah–6Dh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are reserved.

A2h Lower Memory, Register 6Eh: STATUS

POWER-ON VALUE	X0XX 0XXXb
READ ACCESS	All
WRITE ACCESS	See below description
MEMORY TYPE	Volatile

Write Access	N/A	All	N/A	All	All	N/A	N/A	N/A
6Eh	TXDS	TXDC	TXFIS	RSELS	RESERVED	TXFOUTS	RXL	RDYB
	BIT 7							BIT 0

BIT 7	**TXDS:** TXD status bit. Reflects the logic state of the TXD pin (read-only). 0 = TXD pin is logic-low. 1 = TXD pin is logic-high.
BIT 6	**TXDC:** TXD software control bit. This bit allows for software control that is identical to the TXD pin. See the section on TXD for further information. Its value is wired-ORed with the logic value of the TXD pin (writable by all users). 0 = (Default) 1 = Forces the device into a TXD state regardless of the value of the TXD pin.
BIT 5	**TXFIS:** Reflects the status of the TXF pin. The status will also include any inversion caused by the INVTXFI bit (read-only). 0 = TXF pin is low (after any inversion caused by the INVTXFI bit). 1 = TXF pin is high (after any inversion caused by the INVTXFI bit).
BIT 4	**RSELS:** RSEL status bit. Reflects the logic state of the RSEL pin (read-only). 0 = RSEL pin is logic-low. 1 = RSEL pin is logic-high.
BIT 3	**RESERVED**
BIT 2	**TXFOUTS:** TXFOUT status. Indicates the state the open drain output is attempting to achieve. 0 = TXFOUT is pulling low. 1 = TXFOUT is high impedance.
BIT 1	**RXL:** Reflects the driven state of the LOS pin (read-only). 0 = LOS pin is driven low. 1 = LOS pin is pulled high.
BIT 0	**RDYB:** Ready bar. 0 = V_{CC} is above POA. 1 = V_{CC} is below POA and/or too low to communicate over the I^2C bus.

A2h Lower Memory, Register 6Fh: UPDATE

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	All and DS1886 Hardware
MEMORY TYPE	Volatile

6Fh	TEMP RDY	VCC RDY	TXB RDY	TXP RDY	RSSI RDY	RSSIR	POW_LEV1	POW_LEV0
	BIT 7							BIT 0

BITS 7:3	Update of completed conversions. At power-on, these bits are cleared and are set as each conversion is completed. These bits can be cleared so that a completion of a new conversion is verified.
BIT 2	**RSSIR:** RSSI range. Reports the range used for conversion update of RSSI. 0 = Fine range is the reported value. 1 = Coarse range is the reported value.
BITS 1:0	**POW_LEV[1:0]:** Power level. These bits are active only when the DS1863_MODE bit in A2h Table 02h, Register 8Dh (CNFGD) is 0. These bits change the MAX3710 bits KRMD[2:1] to adjust the MD input impedance. See the *Power Leveling* section for more details.

A2h Lower Memory, Register 70h: $ALARM_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

70h	TEMP HI	TEMP LO	VCC HI	VCC LO	TXB HI	TXB LO	TXP HI	TXP LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low Alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High alarm status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low alarm status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**TXB HI:** High alarm status for TXB measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**TXB LO:** Low alarm status for TXB measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**TXP HI:** High alarm status for TXP measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**TXP LO:** Low alarm status for TXP measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

A2h Lower Memory, Register 71h: $ALARM_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

71h	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	IN1S	RESERVED	TXFINT
	BIT 7							BIT 0

BIT 7	**RSSI HI:** High alarm status for RSSI measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**RSSI LO:** Low alarm status for RSSI measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 5:3	**RESERVED**
BIT 2	**IN1S:** IN1 status bit. Reflects the logic state of the IN1 pin (read-only). 0 = IN1 pin is logic-low. 1 = IN1 pin is logic-high.
BIT 1	**RESERVED**
BIT 0	**TXFINT:** TXFOUT interrupt. This bit is the wired-ORed logic of all alarms and warnings wired-ANDed with their corresponding enable bits. The enable bits are found in A2h Table 01h/05h, Registers F8–FFh.

A2h Lower Memory, Register 72h–73h: RESERVED

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are reserved.

A2h Lower Memory, Register 74h: $WARN_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

74h	TEMP HI	TEMP LO	VCC HI	VCC LO	TXB HI	TXB LO	TXP HI	TXP LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High warning status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low warning status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High warning status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low warning status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**TXB HI:** High warning status for TXB measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**TXB LO:** Low warning status for TXB measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**TXP HI:** High warning status for TXP measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**TXP LO:** Low warning status for TXP measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

A2h Lower Memory, Register 75h: $WARN_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

75h	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**RSSI HI:** High warning status for RSSI measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**RSSI LO:** Low warning status for RSSI measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 5:0	**RESERVED**

A2h Lower Memory, Register 76h–7Ah: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are reserved.

A2h Lower Memory, Register 7Bh–7Eh: PASSWORD ENTRY (PWE)

POWER-ON VALUE	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	ALL
MEMORY TYPE	Volatile

7Bh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
7Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7Dh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
7Eh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

There are two passwords for the DS1886. Each password is 4 bytes long. The lower level password (PW1) will have all the access of a normal user plus those made available with PW1. The higher level password (PW2) will have all of the access of PW1 plus those made available with PW2. The values of the passwords reside in EEPROM inside of PW2 memory. At power up, all PWE bits are set to 1. All reads at this location are 0.

A2h Lower Memory, Register 7Fh: TBL SEL

POWER-ON VALUE	TBLSELPON (A2h Table 02h, Register C7h).
READ ACCESS	All
WRITE ACCESS	All
MEMORY TYPE	Volatile

7Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The upper memory tables of the DS1886 are accessible by writing the desired table value in this register. The power-on value of this register is defined by the value written to TBLSELPON (A2h Table 02, Register C7h).

A2h Table 01h Register Descriptions

A2h Table 05h can be configured to contain the alarm and warning enable bytes from A2h Table 01h, Registers F8h–FFh with the MASK bit enabled (A2h Table 02h, Register 89h). In this case the corresponding bytes in A2h Table 01h are empty.

A2h Table 01h, Register 80h–BFh: EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1A) or (PW1 and RTBL1A)
WRITE ACCESS	PW2 or (PW1 and RWTBL1A)
MEMORY TYPE	Nonvolatile (EE)

80h–BFh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1 and/or PW2 level access.

A2h Table 01h, Register C0h–F7h: EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1B) or (PW1 and RTBL1B)
WRITE ACCESS	PW2 or (PW1 and RWTBL1B)
MEMORY TYPE	Nonvolatile (EE)

C0h–F7h	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1 and/or PW2 level access.

A2h Table 01h, Register F8h: ALARM EN_3

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

F8h	TEMP HI	TEMP LO	VCC HI	VCC LO	TXB HI	TXB LO	TXP HI	TXP LO
	BIT 7							BIT 0

Layout is identical to $ALARM_3$ in Lower Memory, Register 70h. Enables alarms to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (A2h Table 02h, Register 89h) determines whether this memory exists in A2h Table 01h or 05h. When in A2h Table 05h, this location at A2h Table 01h becomes EE.

BIT 7	**TEMP HI:** 0 = Disables interrupt from TEMP HI alarm. 1 = Enables interrupt from TEMP HI alarm.
BIT 6	**TEMP LO:** 0 = Disables interrupt from TEMP LO alarm. 1 = Enables interrupt from TEMP LO alarm.
BIT 5	**VCC HI:** 0 = Disables interrupt from VCC HI alarm. 1 = Enables interrupt from VCC HI alarm.
BIT 4	**VCC LO:** 0 = Disables interrupt from VCC LO alarm. 1 = Enables interrupt from VCC LO alarm.
BIT 3	**TXB HI:** 0 = Disables interrupt from TXB HI alarm. 1 = Enables interrupt from TXB HI alarm.
BIT 2	**TXB LO:** 0 = Disables interrupt from TXB LO alarm. 1 = Enables interrupt from TXB LO alarm.
BIT 1	**TXP HI:** 0 = Disables interrupt from TXP HI alarm. 1 = Enables interrupt from TXP HI alarm.
BIT 0	**TXP LO:** 0 = Disables interrupt from TXP LO alarm. 1 = Enables interrupt from TXP LO alarm.

A2h Table 01h, Register F9h: ALARM EN_2

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

F9h	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	IN1EN	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $ALARM_2$ in Lower Memory, Register 71h. Enables alarms to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (A2h Table 02h, Register 89h) determines whether this memory exists in A2h Table 01h or 05h. When in A2h Table 05h, this location at A2h Table 01h becomes EE.

BIT 7	**RSSI HI:** 0 = Disables interrupt from RSSI HI alarm. 1 = Enables interrupt from RSSI HI alarm.
BIT 6	**RSSI LO:** 0 = Disables interrupt from RSSI LO alarm. 1 = Enables interrupt from RSSI LO alarm.
BITS 5:3	**RESERVED**
BIT 2	**IN1EN** 0 = Disable interrupt due to IN1 input pin. 1 = Enable interrupt due to IN1 input pin.
BIT 0	**RESERVED**

A2h Table 01h, Register FAh–FBh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved. When in A2h Table 05h, this location at A2h Table 01h becomes EE.

A2h Table 01h, Register FCh: WARN EN_3

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FCh	TEMP HI	TEMP LO	VCC HI	VCC LO	TXB HI	TXB LO	TXP HI	TXP LO
	BIT 7							BIT 0

Layout is identical to $WARN_3$ in Lower Memory, Register 74h. Enables warnings to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (A2h Table 02h, Register 89h) determines whether this memory exists in A2h Table 01h or 05h. When in A2h Table 05h, this location at A2h Table 01h becomes EE.

BIT 7	**TEMP HI:** 0 = Disables interrupt from TEMP HI warning. 1 = Enables interrupt from TEMP HI warning.
BIT 6	**TEMP LO:** 0 = Disables interrupt from TEMP LO warning. 1 = Enables interrupt from TEMP LO warning.
BIT 5	**VCC HI:** 0 = Disables interrupt from VCC HI warning. 1 = Enables interrupt from VCC HI warning.
BIT 4	**VCC LO:** 0 = Disables interrupt from VCC LO warning. 1 = Enables interrupt from VCC LO warning.
BIT 3	**TXB HI:** 0 = Disables interrupt from TXB HI warning. 1 = Enables interrupt from TXB HI warning.
BIT 2	**TXB LO:** 0 = Disables interrupt from TXB LO warning. 1 = Enables interrupt from TXB LO warning.
BIT 1	**TXP HI:** 0 = Disables interrupt from TXP HI warning. 1 = Enables interrupt from TXP HI warning.
BIT 0	**TXP LO:** 0 = Disables interrupt from TXP LO warning. 1 = Enables interrupt from TXP LO warning.

A2h Table 01h, Register FDh: WARN EN_2

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FDh	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $WARN_2$ in Lower Memory, Register 75h. Enables warnings to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (A2h Table 02h, Register 89h) determines whether this memory exists in A2h Table 01h or 05h. When in A2h Table 05h, this location at A2h Table 01h becomes EE.

BIT 7	**RSSI HI:** 0 = Disables interrupt from RSSI HI warning. 1 = Enables interrupt from RSSI HI warning.
BIT 6	**RSSI LO:** 0 = Disables interrupt from RSSI LO warning. 1 = Enables interrupt from RSSI LO warning.
BITS 5:0	**RESERVED**

A2h Table 01h, Register FEh–FFh: RESERVED OR EE

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

A2h Table 02h Register Descriptions

A2h Table 02h, Register 80h: MODE

POWER-ON VALUE	7Fh
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Volatile

80h	SEEB	INCROW LUT EN	TXCTRL5 LUT EN	BIAS LUT EN	AEN	MOD LUT EN	APC LUT EN	DAC LUT EN
	BIT 7							BIT 0

BIT 7	**SEEB:** 0 = (Default) Enables EEPROM writes to SEE bytes. 1 = Disables EEPROM writes to SEE bytes during configuration, so that the configuration of the part is not delayed by the EE cycle time. Once the values are known, write this bit to a 0 and write the SEE locations again for data to be written to the EEPROM.
BIT 6	**INCROW LUT EN:** 0 = INCROW register is controlled by the user. The INCROW register value is written with the use of the 3-wire interface. This allows users to interactively test their modules by writing the INCROW register value. In APC loop mode, only BIASINC[3:0] is updated. In DPC loop mode, both BIASINC[3:0] and MODINC[3:0] are updated. 1 = (Default) Enables auto control for the INCROW register.
BIT 5	**TXCTRL5 LUT EN:** 0 = TXCTRL5 DPC register is writable by the user and the LUT recalls are disabled. 1 = (Default) Enables auto control of the LUT for TXCTRL5.
BIT 4	**BIAS LUT EN:** 0 = SET_IBIAS and IBIASMAX registers are controlled by the user. The SET_IBIAS and IBIASMAX value is written with the use of the 3-wire interface. This allows the user to interactively test their modules by directly controlling the SET_IBIAS and IBIASMAX. 1 = (Default) Enables LUT control of the SET_IBIAS and IBIASMAX.
BIT 3	**AEN:** 0 = The temperature-calculated index value TINDEX is writable by the user and the updates of calculated indexes are disabled. This allows users to interactively test their modules by controlling the indexing for the look up tables. The recalled values from the LUTs appear in the DAC registers after the next completion of a temperature conversion. 1 = (Default) The internal temperature sensor determines the value of TINDEX
BIT 2	**MOD LUT EN:** 0 = MODULATION VALUE and IMODMAX registers are controlled by the user. The MODULATION VALUE and IMODMAX values are written with the use of the 3-wire interface. This allows users to interactively test their modules by directly controlling the MODULATION VALUE and IMODMAX. 1 = (Default) Enables LUT control of MODULATION VALUE and IMODMAX.
BIT 1	**APC LUT EN:** 0 = APC VALUE register is controlled by the user. The APC VALUE value is written with the use of the 3-wire interface. This allows users to interactively test their modules by directly controlling the APC VALUE register. 1 = (Default) Enables LUT control of APC VALUE.
BIT 0	**DAC LUT EN:** See the *Delta-Sigma Output and Reference* section for details. 0 = DAC VALUE is writable by the user and the DAC formula calculation disabled. This allows users to interactively test their modules by writing the values for DAC. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for DAC VALUE.

A2h Table 02h, Register 81h: Temperature Index (TINDEX)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and AEN = 0) or (PW1 and RWTBL246 and AEN = 0)
MEMORY TYPE	Volatile

81h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Holds the calculated index based on the temperature measurement. This index is used for the address during lookup of Tables 04h, 06h, and 08h. Temperature measurements below -40°C or above +102°C are clamped to 80h and C7h, respectively. The calculation of TINDEX is as follows:

$$\text{TINDEX} = \frac{\text{Temp\_Value} + 40°\text{C}}{2°\text{C}} + 80\text{h}$$

For the temperature-indexed LUTs, the index used during the lookup function for each table is as follows:

A2h Table 04h (MOD)	1	TINDEX_6	TINDEX_5	TINDEX_4	TINDEX_3	TINDEX_2	TINDEX_1	TINDEX_0
A2h Table 06h (APC)	1	0	TINDEX_6	TINDEX_5	TINDEX_4	TINDEX_3	TINDEX_2	TINDEX_1

A2h Table 02h, Register 82h–83h: MODULATION VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and MOD LUT EN = 0) or (PW1 and RWTBL246 and MOD LUT EN = 0)
MEMORY TYPE	Volatile

82h	0	0	0	0	0	0	0	2^8
83h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for MOD and recalled from A2h Table 04h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

A2h Table 02h, Register 84h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

This register is reserved.

A2h Table 02h, Register 85h: APC VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and APC LUT EN = 0) or (PW1 and RWTBL246 and APC LUT EN = 0)
MEMORY TYPE	Volatile

85h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for APC and recalled from A2h Table 06h in the APC and dual-closed-loop mode at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

A2h Table 02h, Register 86h–87h: SET_IBIAS VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and APC LUT EN = 0) or (PW1 and RWTBL246 and APC LUT EN = 0)
MEMORY TYPE	Volatile

86h	0	0	0	0	0	0	2^9	2^8
87h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for BIAS and recalled from A2h Table 06h in the open-loop mode at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

A2h Table 02h, Register 88h: DACFS

FACTORY DEFAULT	FFh
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

88h	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

DACFS sets the slope of the DAC's temperature compensation. In conjunction with DAC OFFSET and TINDEX, this allows the DAC to create an output that is linearly dependent on temperature. For further details see the *Delta-Sigma Output and Reference* section.

A2h Table 02h, Register 89h: CNFGA

FACTORY DEFAULT	82h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

89h	LOSC	RESERVED	INV LOS	RESERVED	MASK	RESERVED	BURST_MODE	INVTXFI
	BIT 7							BIT 0

BIT 7	**LOSC:** Enables LOSOUT due to input pin LOS. 0 = LOSOUT is affected by the LOS input. 1 = LOSOUT is not affected by changed in the LOS input.
BIT 6	**RESERVED**
BIT 5	**INV LOS:** Inverts the buffered input pin LOS to output pin LOSOUT. 0 = Noninverted LOS to LOSOUT pin. 1 = Inverted LOS to LOSOUT pin.
BIT 4	**RESERVED**
BIT 3	**MASK:** 0 = Alarm enable row exists at A2h Table 01h, Registers F8h–FFh. A2h Table 05h, Registers F8h–FFh are empty. 1 = Alarm enable row exists at A2h Table 05h, Registers F8h–FFh. A2h Table 01h, Registers F8h–FFh are empty.
BIT 2	**RESERVED**
BIT 1	**BURST_MODE:** 0 = TXP is derived from the TXMON input. 1 = TXP is calculated from MD0 and MD1, which are read from the MAX3710 through the 3-wire interface.
BIT 0	**INVTXFI:** Allow for inversion of signal driven by TXF input pin. 0 = (Default) TXF signal is not inverted. 1 = TXF signal is inverted.

A2h Table 02h, Register 8Ah: CNFGB

FACTORY DEFAULT	40h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

8Ah	RESERVED	BIASMOD_RSTEN	RESERVED	RESERVED	RESERVED	ALATCH	RESERVED	WLATCH
	BIT 7							BIT 0

BIT 7	**RESERVED**
BIT 6	**BIASMOD_RSTEN:** 0 = BIASREG and MODREG when set to 0 do not cause a restart. 1 = (Default) When BIASREG = 0 or MODREG = 0 in the MAX3710, the TXCTRL6 restart and soft_ restart bits are set to 1.
BITS 5:3	**RESERVED**
BIT 2	**ALATCH:** ADC alarm's comparison LATCH. A2h Table 01h, Registers 70h–71h. 0 = ADC alarm and flags reflect the status of the last comparison. 1 = ADC alarm flags remain set.
BIT 1	**RESERVED**
BIT 0	**WLATCH:** ADC warning's comparison LATCH. A2h Table 01h, Registers 74h–75h. 0 = ADC warning flags reflect the status of the last comparison. 1 = ADC warning flags remain set.

A2h Table 02h, Register 8Bh: CNFGC

FACTORY DEFAULT	10h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

8Bh	XOVEREN	RESERVED	TXDM3	BIASMODOVFL_FLT	TXDFLT	TXDIO	RSSI_FC	RSSI_FF
	BIT 7							BIT 0

BIT 7	**XOVEREN:** Enables RSSI conversion to use the XOVER (A2h Table 02h, Register 90h–91h) value during RSSI conversions. 0 = Uses hysteresis for linear RSSI measurements. 1 = XOVER value is enabled for nonlinear RSSI measurements.
BIT 6	**RESERVED**
BIT 5	**TXDM3:** Enables TXD to reset alarms and warnings associated to RSSI during a TXD event. 0 = TXD event has no affect on the RSSI alarms and warnings. 1 = RSSI alarms and warnings are reset during a TXD event.
BIT 4	**BIASMODOVFL_FLT:** 0 = IBIASOVFL and IMODOVFL bits in the DPCSTAT register in the MAX3710 have no affect on TXFOUT. 1 = IBIASOVFL or IMODOVFL bits when set to 1 in the DPCSTAT register in the MAX3710 cause the TXFOUT pin to be set to 1.
BIT 3	**TXDFLT:** See Figure 10. 0 = TXF pin has no affect on TXDOUT. 1 = TXF pin is enabled and ORed with other possible signals to create TXDOUT.
BIT 2	**TXDIO:** See Figure 10. 0 = (Default) TXD input signal is enabled and ORed with other possible signals to create TXDOUT. 1 = TXD input signal has no affect on TXDOUT.
BITS 1:0	**RSSI_FC and RSSI_FF:** RSSI force coarse and RSSI force fine. Control bits for RSSI mode of operation on the RSSI conversion. 00b = (Default) Normal RSSI mode of operation. 01b = The fine settings of scale and offset are used for RSSI conversions. 10b = The coarse settings of scale and offset are used for RSSI conversions. 11b = Normal RSSI mode of operation.

A2h Table 02h, Register 8Ch: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

This register is reserved.

A2h Table 02h, Register 8Dh: CNFGD

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

8Dh	INV_DAC	RESERVED	RESERVED	RESERVED	DS1863_MODE	POW_LEV_DS1863	
	BIT 7						BIT 0

BIT 7	**INV_DAC:** 0 = DAC output is inverted. 1 = DAC output is not inverted.	
BITS 6:4	**RESERVED**	
BIT 3	**DS1863_MODE:** 0 = Normal operation. Power leveling defined in A2h Lower Memory, Register 6Fh. 1 = DS1863 mode. This mode is usually used for systems upgrading from the DS1863. In this mode, KRMD[2:0] in the MAX3710 is directly written to by the POW_LEV_DS1863 bits.	
BITS 2:0	**POW_LEV_DS1863[2:0]**	**POWER LEVEL (dB)**
	000	0
	001	0
	010	0
	011	-3
	100	-3
	101	-3
	110	-6
	111	-6

A2h Table 02h, Register 8Eh: RIGHT-SHIFT$_1$ (RSHIFT$_1$)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

8Eh	RESERVED	TXB_2	TXB_1	TXB_0	RESERVED	TXP_2	TXP_1	TXP_0
	BIT 7							BIT 0

Allows for right-shifting the final answer of TXB and TXP voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

A2h Table 02h, Register 8Fh: RIGHT-SHIFT$_0$ (RSHIFT$_0$)

FACTORY DEFAULT	30h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

8Fh	RESERVED	RSSIF$_2$	RSSIF$_1$	RSSIF$_0$	RESERVED	RSSIC$_2$	RSSIC$_1$	RSSIC$_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of RSSI fine and coarse voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

A2h Table 02h, Register 90h–91h: XOVER COARSE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

90h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
91h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	0
	BIT 7							BIT 0

Defines the crossover value for RSSI measurements of nonlinear inputs when XOVEREN is set to a 1 (A2h Table 02h, Register 8Bh). RSSI coarse conversion results (before right-shifting) less than this register are clamped to the value of this register.

A2h Table 02h, Register 92h–93h: V_{CC} SCALE
A2h Table 02h, Register 94h–95h: TXB SCALE
A2h Table 02h, Register 96h–97h: TXP SCALE
A2h Table 02h, Register 98h–99h: RSSI FINE SCALE
A2h Table 02h, Register 9Ah–9Bh: RESERVED
A2h Table 02h, Register 9Ch–9Dh: RSSI COARSE SCALE

FACTORY CALIBRATED	
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

92h, 94h, 96h, 98h, 9Ch	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
93h, 95h, 97h, 99h, 9Dh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Controls the scaling or gain of the full-scale voltage measurements. The factory-calibrated value produces a full-scale voltage of 6.5536V for V_{CC}; 2.5V for TXB, TXP, and MON4; and 0.3125V for RSSI fine.

A2h Table 02h, Register 9Eh–9Fh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

A2h Table 02h, Register A0h–A1h: XOVER FINE

FACTORY DEFAULT	FFFFh
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
A0h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
A1h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	0

Defines the crossover value for RSSI measurements of nonlinear inputs when XOVEREN is set to 1 (A2h Table 02h, Register 8Bh). RSSI fine conversion results (before right-shifting) greater than this register require a RSSI coarse conversion.

A2h Table 02h, Register A2h–A3h: V_{CC} OFFSET
A2h Table 02h, Register A4h–A5h: TXB OFFSET
A2h Table 02h, Register A6h–A7h: TXP OFFSET
A2h Table 02h, Register A8h–A9h: RSSI FINE OFFSET
A2h Table 02h, Register AAh–ABh: RESERVED
A2h Table 02h, Register ACh–ADh: RSSI COARSE OFFSET

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
A2h, A4h, A6h, A8h, ACh	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}
A3h, A5h, A7h, A9h, ADh	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}

Allows for offset control of these voltage measurements if desired. This number is two's complement.

A2h Table 02h, Register AEh–AFh: INTERNAL TEMP OFFSET

FACTORY CALIBRATED	
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

AEh	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2
AFh	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}
	BIT 7							BIT 0

Allows for offset control of temp measurement if desired. The final result must be XORed with BB40h before writing to this register. Factory calibration contains the desired value for a reading in degrees Celsius.

A2h Table 02h, Register B0h–B3h: PW1

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2 or (PW1 and WPW1)
MEMORY TYPE	Nonvolatile (SEE)

B0h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B1h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B2h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
B3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW1 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW1 access on power-on without writing the password entry. All reads of this register are 00h.

A2h Table 02h, Register B4h–B7h: PW2

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B4h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B5h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B6h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B7h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW2 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW2 access on power-on without writing the password entry. All reads of this register are 00h.

A2h Table 02h, Register B8h–BFh: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Table 02h, Register C0h: PW_ENA

FACTORY DEFAULT	10h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

C0h	RWTBL89	RWTBL1C	RWTBL2	RWTBL1A	RWTBL1B	WA2 LOWER	WAUXA	WAUXB
	BIT 7							BIT 0

BIT 7	**RWTBL89:** Tables 08h–09h. 0 = (Default) read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 6	**RWTBL1C:** A2h Table 01h or 05h bytes F8–FFh. Table address is dependent on MASK bit (A2h Table 02h, Register 89h). 0 = (Default) read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 5	**RWTBL2:** Table 02h except for PW1 value locations (A2h Table 02h, Registers B0h–B3h). 0 = (Default) read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 4	**RWTBL1A:** Read and write A2h Table 01h, Registers 80h–BFh. 0 = Read and write access for PW2 only. 1 = (Default) read and write access for both PW1 and PW2.
BIT 3	**RWTBL1B:** Read and write A2h Table 01h, Registers C0h–F7h. 0 = (Default) read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 2	**WA2 LOWER:** Write lower memory bytes 00h–5Fh in main memory. All users can read this area. 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 1	**WAUXA:** Write auxiliary memory, Registers 00h–7Fh. All users can read this area (see also A2h Table 02h, Register C1h, PW_ENB). 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 0	**WAUXB:** Write auxiliary memory, Registers 80h–FFh. All users can read this area (see also A2h Table 02h, Register C1h, PW_ENB). 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.

A2h Table 02h, Register C1h: PW_ENB

FACTORY DEFAULT	03h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

C1h	RWTBL46	RTBL1C	RTBL2	RTBL1A	RTBL1B	WPW1	WAUXAU	WAUXBU
	BIT 7							BIT 0

BIT 7	**RWTBL46:** Read and write Tables 04h and 06h. 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 6	**RTBL1C:** Read A2h Table 01h or A2h Table 05h, Registers F8h–FFh. Table address is dependent on the MASK bit (A2h Table 02h, Register 89h). 0 = (Default) Read access for PW2 only. 1 = Read access for both PW1 and PW2.
BIT 5	**RTBL2:** Read A2h Table 02h except for PW1 value locations (A2h Table 02h, Registers B0h–B3h). 0 = (Default) Read access for PW2 only. 1 = Read access for both PW1 and PW2.
BIT 4	**RTBL1A:** Read A2h Table 01h, Registers 80h–BFh. 0 = (Default) read access for PW2 only. 1 = Read access for both PW1 and PW2.
BIT 3	**RTBL1B:** Read A2h Table 01h, Registers C0h-F7h. 0 = (Default) read access for PW2 only. 1 = Read access for both PW1 and PW2.
BIT 2	**WPW1:** Write register PW1 (A2h Table 02h, Registers B0h–B3h). For security purposes these registers are not readable. 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 1	**WAUXAU:** Write auxiliary memory, Registers 00h–7Fh. All users can read this area (see also A2h Table 02h, Register C0h, PW_ENA). 0 = Write access for PW2 only. 1 = (Default) Write access for user, PW1, and PW2.
BIT 0	**WAUXBU:** Write auxiliary memory, Registers 80h–FFh. All users can read this area (see also A2h Table 02h, Register C0h, PW_ENA) 0 = Write access for PW2 only. 1 = (Default) Write access for user, PW1, and PW2.

A2h Table 02h, Register C2h–C6h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

A2h Table 02h, Register C7h: TBLSELPON

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Chooses the initial value for the TBL SEL byte (Lower Memory, Register 7Fh) at power-on.

A2h Table 02h, Register C8h–C9h: DAC VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and BIAS LUT EN = 0) or (PW1 and RWTBL246 and BIAS LUT EN = 0)
MEMORY TYPE	Volatile

C8h	0	0	0	0	0	0	2^9	2^8
C9h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Value written to DAC when DAC_EN = 0, or calculated using the formula stated in the *Delta-Sigma Output and Reference* section.

A2h Table 02h, Register CAh: INCBYTE

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and BIAS LUT EN = 0) or (PW1 and RWTBL246 and BIAS LUT EN = 0)
MEMORY TYPE	Volatile

CAh	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

7:4: Value written to MAX3710 BIASINC[3:0] from LUT. This must be set to 0 in open-loop mode.
3:0: Value written to MAX3710 MODINC[3:0] from LUT. This must be set to 0 in open-loop mode and APC mode.

A2h Table 02h, Register CBh: TXCTRL5 DPC

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	(PW2 and APC LUT EN = 0) or (PW1 and RWTBL246 and APC LUT EN = 0)
MEMORY TYPE	Volatile

CBh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Value written to MAX3710 TXCTRL5 from the TXCTRL5 LUT. The TXCTRL5 LUT is only active during the dual closed loop mode. For open loop and APC loop mode, see Register E8h.

A2h Table 02h, Register CCh: IMODMAX

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Volatile

CCh	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1
	BIT 7							BIT 0

Value written to MAX3710 IMODMAX from the MOD MAX LUT.

A2h Table 02h, Register CDh: IBIASMAX

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Volatile

CDh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

Value written to MAX3710 IBIASMAX from the BIAS MAX LUT.

A2h Table 02h, Register CEh: DEVICE ID

FACTORY DEFAULT	86h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

CEh	1	0	0	0	0	1	0	0
	BIT 7							BIT 0

Hardwired connections to show the device ID.

A2h Table 02h, Register CFh: DEVICE VER

FACTORY DEFAULT	DEVICE VERSION
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

CFh	DEVICE VERSION	
	BIT 7	BIT 0

Hardwired connections to show the device version.

A2h Table 02h, Register D0h–DFh: EMPTY

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	None

These registers do not exist.

A2h Table 02h, Register E0h: RXCTRL1

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
E0h	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E1h: RXCTRL2

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
E1h	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E2h: SETCML

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
E2h	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E3h: SETLOSH

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
E3h	BIT 7							BIT 0

A 3-wire slave register. Only written if SETLOSCTL is 1. If SETLOSCTL is 0, then SETLOSL register is used. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E4h: TXCTRL1

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
E4h	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E5h: TXCTRL2

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

E5h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E6h: TXCTRL3

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

E6h	2^7	2^6	2^5	2^4	2^3	POW_LEV_INIT	2^0
	BIT 7						BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface. For bits 2:1, see the POW_LEV[1:0] bits in A2h Lower Memory, Register 6Fh and Table 11a and Table 11b.

A2h Table 02h, Register E7h: TXCTRL4

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

E7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register E8h: TXCTRL5 APC OL

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

E8h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface. This register is active only during the open loop and APC loop modes. See Register CBh for TXCTRL5 access during the dual closed-loop mode.

A2h Table 02h, Register E9h: TXCTRL6

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

E9h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register EAh: TXCTRL7

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

EAh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register EBh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

This register is reserved.

A2h Table 02h, Register ECh: SETLOSH_3945

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

ECh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A2h Table 02h, Register EDh: SETLOSL_3945

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

EDh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. Only written if SETLOSCTL is 0. If SETLOSCTL is 1, then the SETLOSH register is used. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register EEh: SETLOSTIMER_3945

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

EEh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A 3-wire slave register. After either V_{CC} exceeds POA (after a POR event), a Maxim laser driver TX_POR bit is set high (visible in 3-wire TXSTAT1 bit 7), or on a rising edge of TXD, this value is written to a Maxim laser driver through the 3-wire interface.

A2h Table 02h, Register EFh: 3WSET

FACTORY DEFAULT	60h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

EFh	TEMP_UPD	EN_3945	RSTRT_3710	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**TEMP_UPD:** 0 = Default 3-wire operation. 1 = All the control registers (from Register 0Eh–E8h and Register EAh) are written every temperature conversion.
BIT 6	**EN_3945:** 0 = Bytes associated with the MAX3945 are not sent on the 3-wire bus. 1 = Bytes associated with the MAX3945 are transmitted on the 3-wire bus on power-up (after V_{CC} crosses the VCC LO alarm).
BIT 5	**RSTRT_3710:** 0 = TXINLOS (TXSTAT1 register) does not affect system restart. 1 = When TXINLOS (TXSTAT1 register) is set, Register E9h (TXCTRL6) is written to MAX3710 periodically every t_{RR}.
BITS 4:0	**RESERVED**

A2h Table 02h, Register F0h: 3WCTRL

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Volatile

F0h	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	3WMAN_3945	3WRW	3WDIS
	BIT 7							BIT 0

BITS 7:3	**RESERVED**
BIT 2	**3WMAN_3945:** When this bit is set when 3WRW is set, only the MAX3945 is written using CSELOUT2.
BIT 1	**3WRW:** Initiates a 3-wire read or write operation. The write command uses the memory address found in the 3-wire ADDRESS register (A2h Table 02h, Register F1h) and the data from the 3-wire WRITE register (A2h Table 02h, Register F2h). The read command uses the memory address found in the 3-wire ADDRESS register (A2h Table 02h, Register F1h). The address determines whether a read or write operation is to be performed. This bit clears itself at the completion of the operation. 0 = (Default) Reads back as 0 when the read or write operation is completed. 1 = Initiates a 3-wire read or write operation.
BIT 0	**3WDIS:** Disables all automatic communication across the 3-wire interface. This includes all updates from the LUTs, the APC loop, and status registers updates. The only 3-wire communication is with the manual mode of operation. 0 = (Default) Automatic communication is enabled. 1 = Disables automatic communication.

A2h Table 02h, Register F1h: ADDRESS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

F1h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

This byte is used during manual 3-wire communication. When a manual read or write is initiated, this register contains the address for the operation.

A2h Table 02h, Register F2h: WRITE

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F2h	BIT 7							BIT 0

This byte is used during manual 3-wire communication. When a manual write is initiated, this register contains the address for the operation.

A2h Table 02h, Register F3h: READ

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F3h	BIT 7							BIT 0

This byte is used during maunual 3-wire communication. When a manual read is initiated, the return data is stored in this register.

A2h Table 02h, Register F4h: TXSTAT2

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F4h	BIT 7							BIT 0

A 3-wire slave register. This value is read from a Maxim laser driver with the 3-wire interface every t_{RR} (see the *Analog Voltage Monitoring Characteristics* table).

A2h Table 02h, Register F5h: TXSTAT1

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F5h	BIT 7							BIT 0

A 3-wire slave register. This value is read from a Maxim laser driver with the 3-wire interface every t_{RR} (see the *Analog Voltage Monitoring Characteristics* table).

A2h Table 02h, Register F6h: DPCSTAT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F6h	BIT 7							BIT 0

A 3-wire slave register. This value is read from a Maxim laser driver with the 3-wire interface every t_{RR} (see the *Analog Voltage Monitoring Characteristics* table).

A2h Table 02h, Register F7h: RXSTAT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
F7h	BIT 7							BIT 0

A 3-wire slave register. This value is read from a Maxim laser driver with the 3-wire interface every t_{RR} (see the *Analog Voltage Monitoring Characteristics* table).

A2h Table 02h, Register F8h–FFh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

A2h Table 04h Register Descriptions

A2h Table 04h, Register 80h–A7h: MODULATION or TXCTRL5 LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

Open Loop and APC Loop (Modulation), Dual Closed Loop (TXCTRL5)

80h–A7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The digital value for the modulation DAC output or TXCTRL5 register in MAX3710. The MODULATION LUT is a set of registers assigned to hold the temperature profile for the MODULATION register. The temperature measurement is used to index the LUT (TINDEX, A2h Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at 80h. Values recalled from this EEPROM memory table are written into the MODULATION VALUE register (A2h Table 02h, Register 82h–83h) location, which holds the value until the next temperature conversion. The part can be placed into a manual mode (MOD LUT EN bit, A2h Table 02h, Register 80h), where MODULATION register is directly controlled for calibration. If the temperature compensation functionality is not required, then program the entire table to the desired modulation setting. See the *BIAS, MODULATION, SET_2XAPC, TXCTRL5 LUTs* section for more details. The MODULATION VALUE written to the register is determined as follows:

MODULATION VALUE = MODULATION LUT + 4 x MOD OFFSET LUT

A2h Table 04h, Register A8h–EFh: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Table 04h, Register F0h–F7h: MOD MAX LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

F0h–F7h	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1
	BIT 7							BIT 0

A2h Table 04h, Register F8h–FFh: MOD OFFSET or SET_IMOD LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

Open Loop, APC Loop, and Dual Closed Loop (SET_IMOD)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

A2h Table 06h, Register 80h–A7h: BIAS or SET_IBIAS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

Open Loop

80h–A7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

APC Loop and Dual Closed Loop

80h–A7h	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The BIAS LUT is a set of registers assigned to hold the temperature profile for the BIAS reference DAC. The temperature measurement is used to index the LUT (TINDEX, A2h Table 02h, Register 81h) in 2°C increments. Values recalled from this EEPROM memory table are written into the BIAS or SET_IBIAS location, which holds the value until the next temperature conversion. The part can be placed into a manual mode, where BIAS or SET_IBIAS can be directly controlled for calibration. If TE temperature compensation is not required by the application, program the entire LUT to the desired BIAS value.

A2h Table 06h, Register A8h–EFh: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Table 06h, Register F0h–F7h: BIAS MAX LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

F0h–F7h	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

A2h Table 06h, Register F8h–FFh: BIAS OFFSET or APC LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (EE)

Open Loop

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2

APC Loop and Dual Closed Loop (APC)

F8h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

A2h Table 08h Register Descriptions

A2h Table 08h, Register 80h–F7h: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Table 08h, Register F8h–FFh: INCBYTE

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Bits 7:4 update the upper nibble of the INCBYTE register (Table 02h, Register CAh). Bits 3:0 update the lower nibble of the INCBYTE register. See the INCBYTE register descriptions for more details.

A2h Table 09h Register Descriptions

A2h Table 09h, Register 80h–F7h: EMPTY

FACTORY DEFAULT	
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are empty.

A2h Table 09h, Register F8h–FFh: DAC OFFSET LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

Auxiliary Memory A0h Register Description

Auxiliary Memory A0h, Register 00h–FFh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWAUXA) or (PW1 and RWAUXAU)
WRITE ACCESS	PW2 or (PW1 and RWAUXA)
MEMORY TYPE	Nonvolatile (EE)

00h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Applications Information

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

Layout Considerations

Connect all GND pins to a common ground plane. Connect all V_{CC} pins together.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the device that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C AC Electrical Characteristics* are within specification.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1886T+	-40°C to +95°C	24 TQFN-EP*
DS1886T+T	-40°C to +95°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2445+1	**21-0201**	**90-0083**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/12	Initial release	—
1	8/12	Made numerous LUT addressing changes for TXINLOS	30, 32, 33, 39, 83, 87, 88, 89