

# 74VHC595FT

## 1. Functional Description

- 8-Bit Shift Register/Latch (3-state)

## 2. General

The 74VHC595FT is an advanced high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHC595FT contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input.

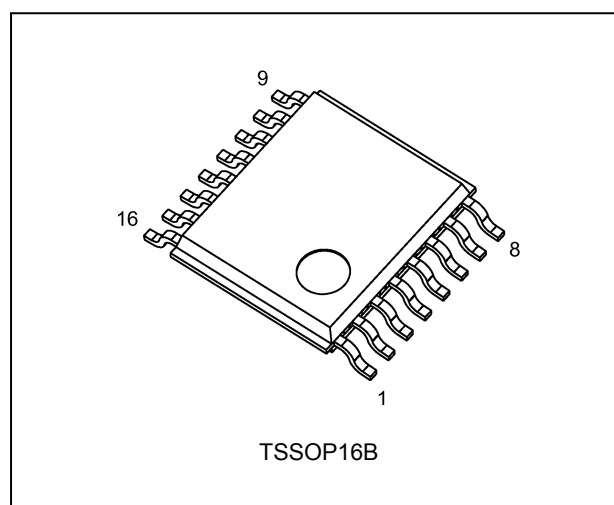
Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

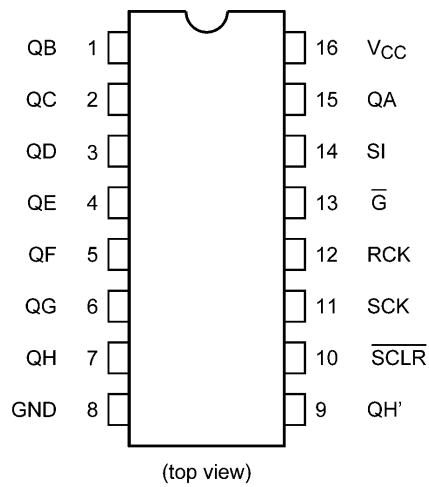
## 3. Features

- (1) High speed:  $f_{MAX} = 185$  MHz (typ.) at  $V_{CC} = 5$  V
- (2) Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ\text{C}$
- (3) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (4) Power-down protection is provided on all inputs.
- (5) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (6) Wide operating voltage range:  $V_{CC(opr)} = 2$  V to 5.5 V
- (7) Low noise:  $V_{OLP} = 1.0$  V (max)
- (8) Pin and function compatible with the 74 serie (74AC/HC/AHC/LV etc.) 595 type.

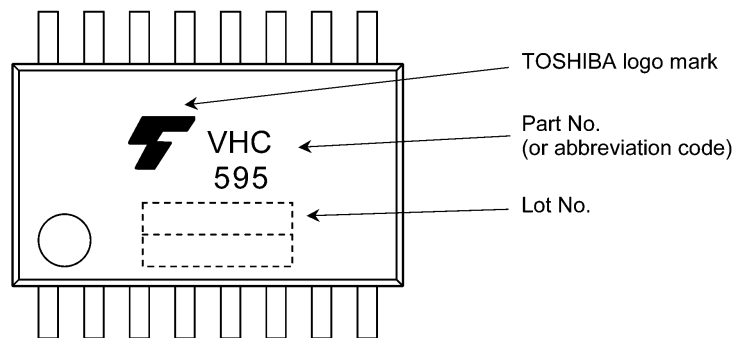
## 4. Packaging



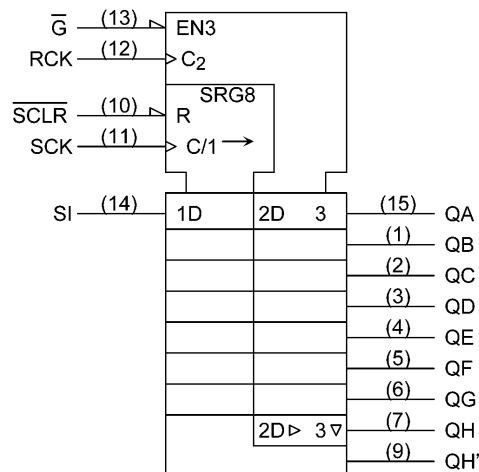
**5. Pin Assignment**








**6. Marking**



**7. IEC Logic Symbol**

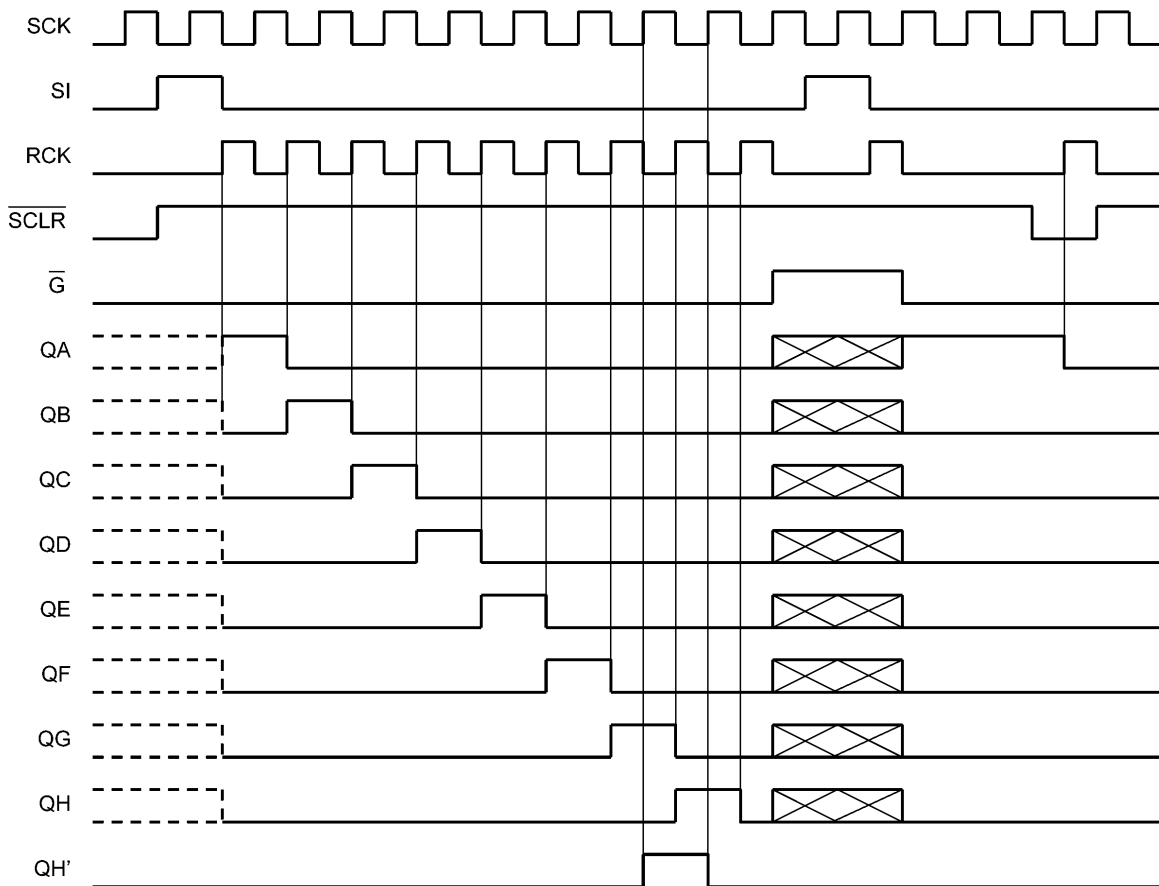


**8. Truth Table**

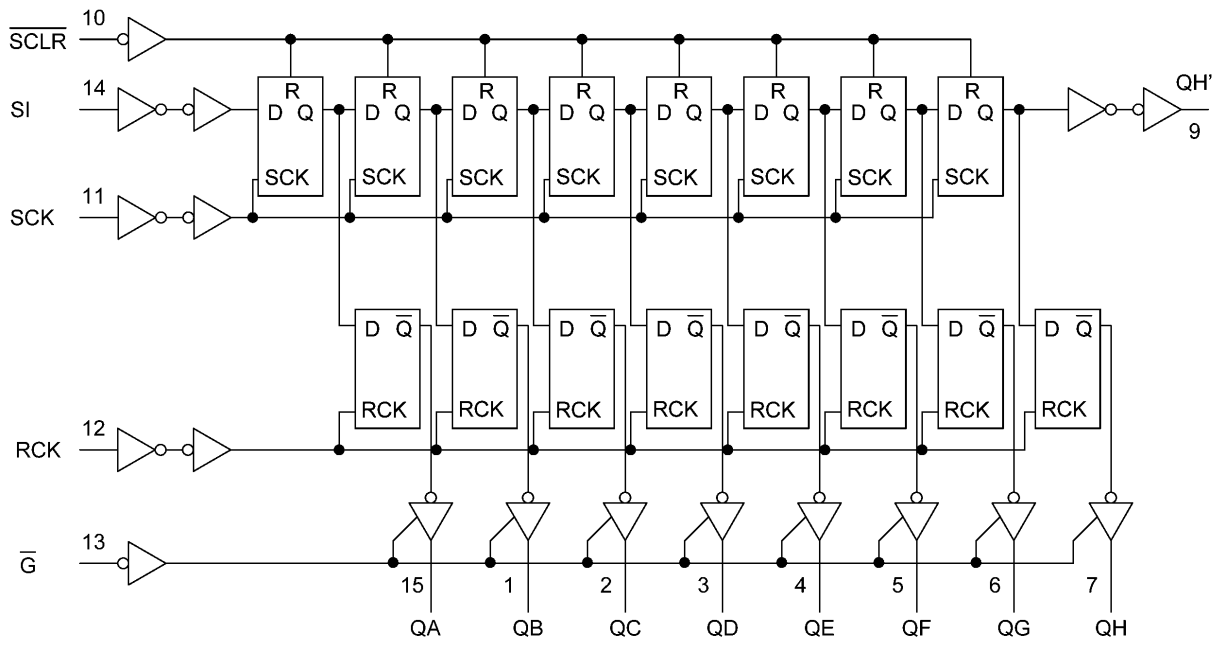
Inputs					Function
SI	SCK	$\overline{\text{SCLR}}$	RCK	$\overline{\text{G}}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L		H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X		H	X	X	State of S.R. is not changed.
X	X	X		X	S.R. data is stored into storage register.
X	X	X		X	Storage register stage is not changed.

X: Don't care

**9. Timing Chart**



**10. System Diagram**



**11. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to 7.0	V
Input voltage	$V_{IN}$	-0.5 to 7.0	V
Output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-6.5 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**12. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 85	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3 V$	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5 V$	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND.

**13. Electrical Characteristics**

**13.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
			4.5	4.4	4.5	—		
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	—	$\pm 0.25$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	—	$\pm 0.1$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	

**13.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OL} = -4\text{ mA}$	3.0	2.48	—	
			$I_{OL} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	$\pm 2.50$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	$\pm 1.0$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	

**13.3. Timing Requirements (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ , Input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	$V_{CC}$ (V)	Typ.	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}, t_{w(H)}$	$3.3 \pm 0.3$	—	5.0	ns
		$5.0 \pm 0.5$	—	5.0	
Minimum pulse width ( $\overline{\text{SCLR}}$ )	$t_{w(L)}$	$3.3 \pm 0.3$	—	5.0	ns
		$5.0 \pm 0.5$	—	5.0	
Minimum setup time (SI-SCK)	$t_s$	$3.3 \pm 0.3$	—	3.5	ns
		$5.0 \pm 0.5$	—	3.0	
Minimum setup time (SCK - RCK)	$t_s$	$3.3 \pm 0.3$	—	8.0	ns
		$5.0 \pm 0.5$	—	5.0	
Minimum setup time ( $\overline{\text{SCLR}}$ -RCK)	$t_s$	$3.3 \pm 0.3$	—	8.0	ns
		$5.0 \pm 0.5$	—	5.0	
Minimum hold time (SI-SCK)	$t_h$	$3.3 \pm 0.3$	—	1.5	ns
		$5.0 \pm 0.5$	—	2.0	
Minimum hold time (SCK-RCK)	$t_h$	$3.3 \pm 0.3$	—	0	ns
		$5.0 \pm 0.5$	—	0	
Minimum hold time ( $\overline{\text{SCLR}}$ -RCK)	$t_h$	$3.3 \pm 0.3$	—	0	ns
		$5.0 \pm 0.5$	—	0	
Minimum removal time ( $\overline{\text{SCLR}}$ )	$t_{rem}$	$3.3 \pm 0.3$	—	3.0	ns
		$5.0 \pm 0.5$	—	2.5	

**13.4. Timing Requirements (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ , Input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (SCK, RCK)	$t_{w(L)}, t_{w(H)}$	$3.3 \pm 0.3$	5.0	ns
		$5.0 \pm 0.5$	5.0	
Minimum pulse width ( $\overline{\text{SCLR}}$ )	$t_{w(L)}$	$3.3 \pm 0.3$	5.0	ns
		$5.0 \pm 0.5$	5.0	
Minimum setup time (SI-SCK)	$t_s$	$3.3 \pm 0.3$	3.5	ns
		$5.0 \pm 0.5$	3.0	
Minimum setup time (SCK - RCK)	$t_s$	$3.3 \pm 0.3$	8.5	ns
		$5.0 \pm 0.5$	5.0	
Minimum setup time ( $\overline{\text{SCLR}}$ -RCK)	$t_s$	$3.3 \pm 0.3$	9.0	ns
		$5.0 \pm 0.5$	5.0	
Minimum hold time (SI-SCK)	$t_h$	$3.3 \pm 0.3$	1.5	ns
		$5.0 \pm 0.5$	2.0	
Minimum hold time (SCK-RCK)	$t_h$	$3.3 \pm 0.3$	0	ns
		$5.0 \pm 0.5$	0	
Minimum hold time ( $\overline{\text{SCLR}}$ -RCK)	$t_h$	$3.3 \pm 0.3$	0	ns
		$5.0 \pm 0.5$	0	
Minimum removal time ( $\overline{\text{SCLR}}$ )	$t_{rem}$	$3.3 \pm 0.3$	3.0	ns
		$5.0 \pm 0.5$	2.5	

**13.5. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time (SCK-QH')	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	8.8	13.0	ns
					50	—	11.3	16.5	
				$5.0 \pm 0.5$	15	—	6.2	8.2	
					50	—	7.7	10.2	
Propagation delay time (SCLR-QH')	$t_{PHL}$		—	$3.3 \pm 0.3$	15	—	8.4	12.8	
					50	—	10.9	16.3	
				$5.0 \pm 0.5$	15	—	5.9	8.0	
					50	—	7.4	10.0	
Propagation delay time (RCK-Q <sub>n</sub> )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	7.7	11.9	
					50	—	10.2	15.4	
				$5.0 \pm 0.5$	15	—	5.4	7.4	
					50	—	6.9	9.4	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	—	7.5	11.5	
					50	—	9.0	15.0	
				$5.0 \pm 0.5$	15	—	4.8	8.6	
					50	—	8.3	10.6	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	—	12.1	15.7	
				$5.0 \pm 0.5$	50	—	7.6	10.3	
Maximum clock frequency	$f_{MAX}$		—	$3.3 \pm 0.3$	15	80	150	—	MHz
					50	55	130	—	
				$5.0 \pm 0.5$	15	135	185	—	
					50	95	155	—	
Input capacitance	$C_{IN}$		—			—	4	10	pF
Output capacitance	$C_{OUT}$		—			—	6	—	
Power dissipation capacitance	$C_{PD}$	(Note 1)	—				—	87	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$



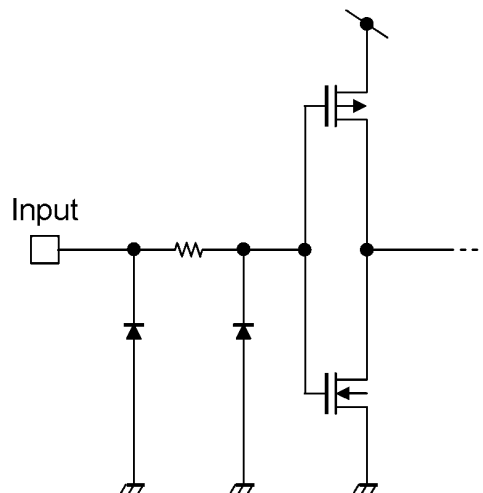
**13.6. AC Characteristics**  
 (Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (SCK-QH')	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	15.0	ns
					50	1.0	18.5	
				$5.0 \pm 0.5$	15	1.0	9.4	
					50	1.0	11.4	
Propagation delay time (SCLR-QH')	$t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	13.7	
					50	1.0	17.2	
				$5.0 \pm 0.5$	15	1.0	9.1	
					50	1.0	11.1	
Propagation delay time (RCK-Q <sub>n</sub> )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	13.5	
					50	1.0	17.0	
				$5.0 \pm 0.5$	15	1.0	8.5	
					50	1.0	10.5	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	1.0	13.5	
					50	1.0	17.0	
				$5.0 \pm 0.5$	15	1.0	10.0	
					50	1.0	12.0	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	1.0	16.2	
				$5.0 \pm 0.5$	50	1.0	11.0	
Maximum clock frequency	$f_{MAX}$		—	$3.3 \pm 0.3$	15	70	—	MHz
					50	50	—	
				$5.0 \pm 0.5$	15	115	—	
					50	85	—	
Input capacitance	$C_{IN}$		—			—	10	pF

**13.7. Noise Characteristics** (Unless otherwise specified,  $T_a = 25$ °C, Input:  $t_r = t_f = 3$  ns)

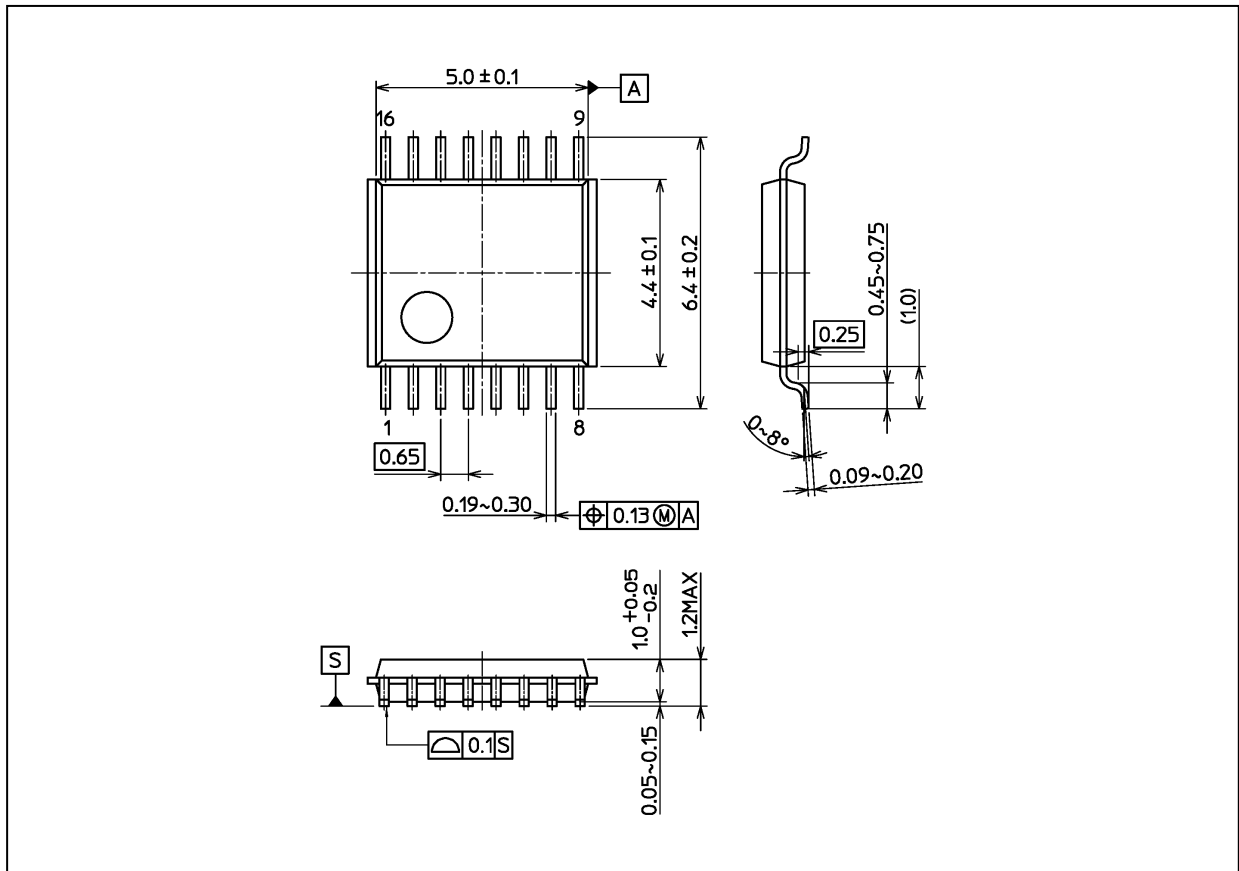
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50$ pF	5.0	0.8	1.0	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50$ pF	5.0	-0.8	-1.0	
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50$ pF	5.0	—	3.5	
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50$ pF	5.0	—	1.5	

**14. Input Equivalent Circuit**



Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

Package Name(s)
Nickname: TSSOP16B

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