QL4036 QuickRAM Data Sheet

36,000 Usable PLD Gate QuickRAM ESP Combining Performance, Density and Embedded RAM

Device Highlights

High Performance & High Density

- 36,000 Usable PLD Gates with 204 I/Os
- 300 MHz 16-bit Counters, 400 MHz Datapaths, 160+ MHz FIFOs
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

High Speed Embedded SRAM

- 14 dual-port RAM modules, organized in user-configurable 1,152 bit blocks
- 5 ns access times, each port independently accessible
- Fast and efficient for FIFO, RAM, and ROM functions

Easy to Use / Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with both 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V busses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O Cells with individually controlled Registered Input Path and Output Enables

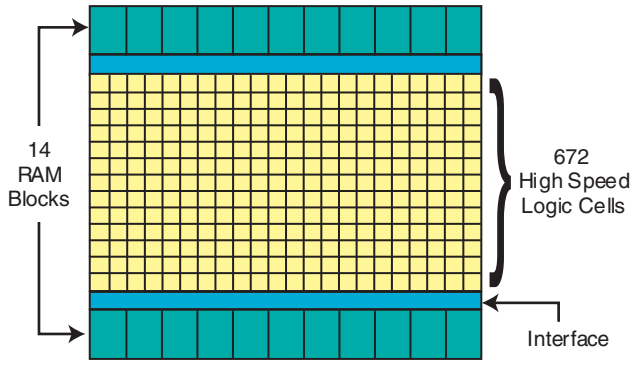


Figure 1: QuickRAM Block Diagram

Architecture Overview

The QuickRAM family of ESPs (Embedded Standard Products) offers FPGA logic in combination with Dual-Port SRAM modules. The QL4036 is a 36,000 usable PLD gate member of the QuickRAM family of ESPs. QuickRAM ESPs are fabricated on a 0.35 µm four-layer metal process using QuickLogic's patented ViaLink®™ technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL4036 contains 672 logic cells and 14 Dual Port RAM modules (see **Figure 1**). Each RAM module has 1,152 RAM bits, for a total of 16,128 bits. RAM Modules are Dual Port (one read port, one write port) and can be configured into one of four modes: 64 (deep) × 18 (wide), 128 × 9, 256 × 4, or 512 × 2 (see **Figure 4**). With a maximum of 82 I/Os, the QL4036 is available in 144-pin TQFP, 208-pin PQFP, 208-pin CQFP, and 256-pin PBGA packages.

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see **Figure 2**). This approach allows up to 512-deep configurations as large as 16 bits wide in the smallest QuickRAM device and 44 bits wide in the largest device.

Software support for the complete QuickRAM family, including the QL4036, is available through two basic packages. The turnkey QuickWorks®™ package provides the most complete ESP software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools packages provides a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Aldec, or other third-party tools for design entry, synthesis, or simulation.

The QuickLogic®™ variable grain logic cell features up to 16 simultaneous inputs and five outputs within a cell that can be fragmented into five independent cells. Each cell has a fan-in of 29 including register and control lines (see **Figure 3**).

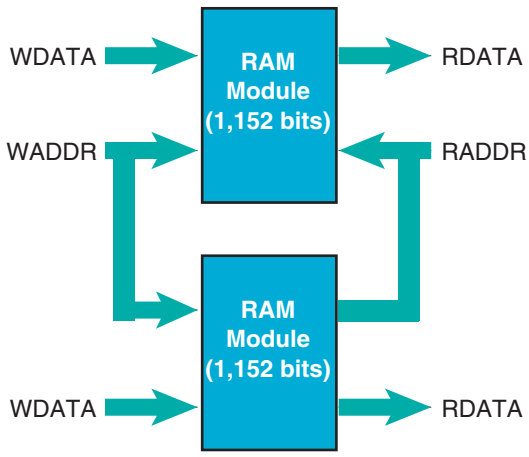


Figure 2: QuickRAM Module Bits

Product Summary

Total of 204 I/O Pins

- 196 bi-directional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- 8 high-drive input/distributed network pins

Eight Low-Skew Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs—each driven by an input-only pin
- Six global clock/control networks available to the logic cell F1, clock, set and reset inputs and the input and I/O register clock, reset and enable inputs as well as the output enable control—each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance Silicon

- Input + logic cell + output total delays = under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz
- FIFO speeds over 160+ MHz

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 10: Operating Range** by the following numbers in the tables provided.

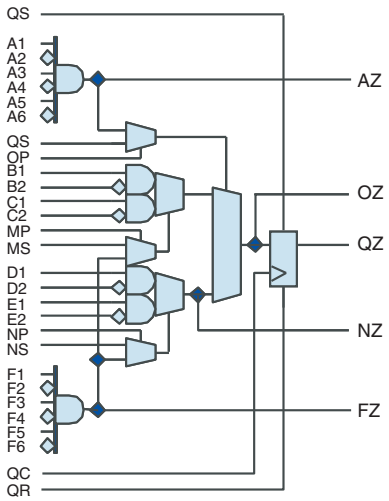


Figure 3: QuickRAM Logic Cell

Table 1: Logic Cell

Symbol	Parameter	Propagation Delays (ns) Fanout (5)				
		1	2	3	4	5
t_{PD}	Combinatorial Delay[a]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time[a]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

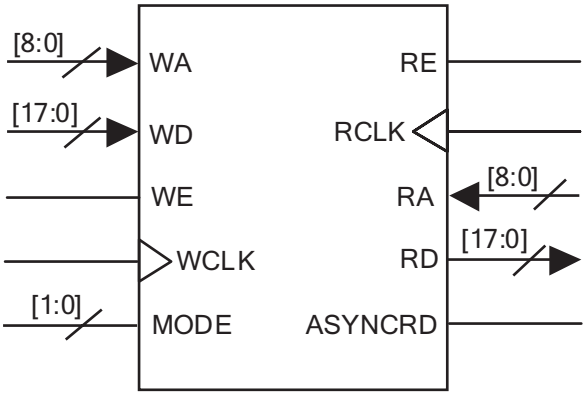


Figure 4: QuickRAM Module

Table 2: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SWA}	WA Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA=RA)[a]	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 3: RAM Cell Synchronous Read Timing

Symbol Logic Cells	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SRA}	RA Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD[a]	4.0	4.3	4.6	4.9	6.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 4: RAM Cell Asynchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
RPDRD	RA to RD[a]	3.0	3.3	3.6	3.9	5.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 5: Input-Only / Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	.19	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register Clock Enable Setup Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Table 6: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

Table 7: I/O Cell Input Delays

Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock to Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register Clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 8: I/O Cell Output Delays

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		3	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-state[a]	2.0	-	-	-	-
t_{PLZ}	Output Delay High to Tri-state[a]	1.2	-	-	-	-

a. These loads are used for t_{PXZ} (see **Figure 5**)

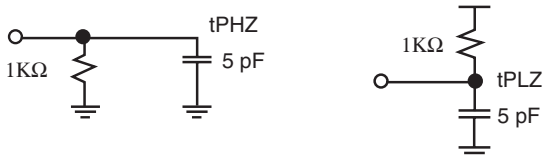


Figure 5: Loads used for t_{PXZ}

DC Characteristics

The DC specifications are provided in the tables below.

Table 9: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 10: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	0.42	2.03	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 11: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
VIH	Input HIGH Voltage		0.5 V_{CC}	$V_{CCI}O$ + 0.5	V
VIL	Input LOW Voltage		-0.5	0.3 V_{CC}	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9 V_{CC}		V
VOL	Output LOW Voltage	IOL = 16 mA[a]		0.45	V
		IOL = 1.5 mA		0.1 V_{CC}	V
II	I or I/O Input Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
CI	Input Capacitance[b]			10	pF
IOS	Output Short Circuit Current[c]	VO = GND	-15	-180	mA
		VO = VCC	40	210	mA
ICC	D.C. Supply Current[d]	VI, VIO = V_{CCIO} or GND	0.50 (typ)	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum ICC is 3 mA for -0 commercial grade and all industrial grade device and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see).

Kv and Kt Graphs

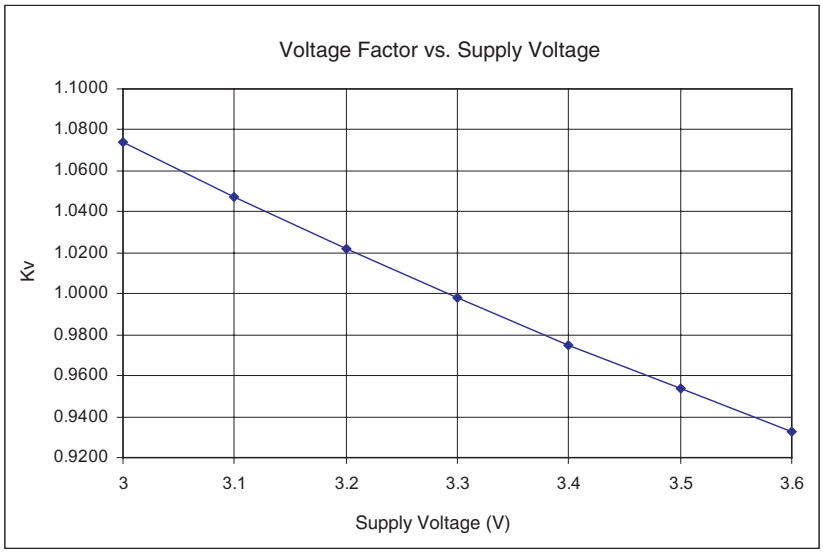


Figure 6: Voltage Factor vs. Supply Voltage

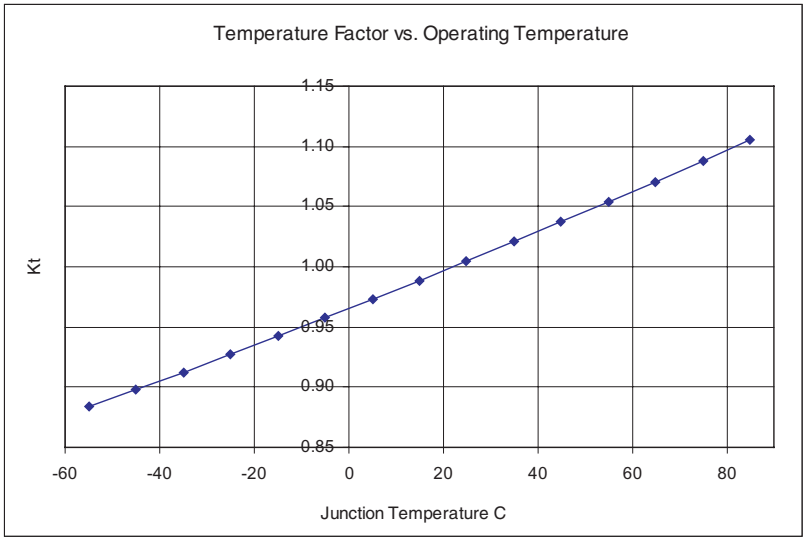


Figure 7: Temperature Factor vs. Operating Temperature

Power-up Sequencing

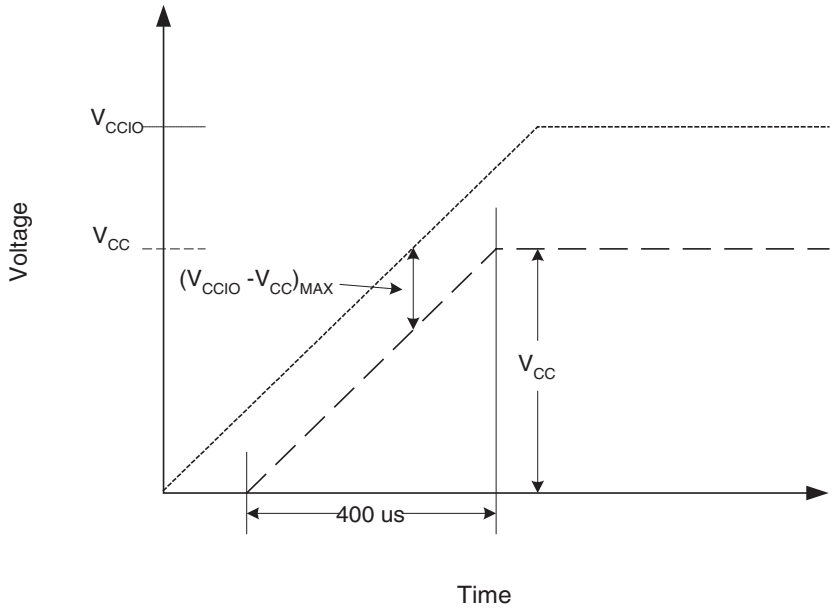


Figure 8: Power-up Requirements

The following requirements must be met when powering up the device (refer to **Figure 8**):

- When ramping up the power supplies keep $(VCCIO - VCC)_{MAX} \leq 500$ mV. Deviation from this recommendation can cause permanent damage to the device.
- V_{CCIO} must lead V_{CC} when ramping the device.
- The power supply must take greater than or equal to 400 µs to reach VCC. Ramping to V_{CC}/V_{CCIO} earlier than 400 µs can cause the device to behave improperly.

An internal diode is present in-between V_{CC} and V_{CCIO}, as shown in **Figure 9**.

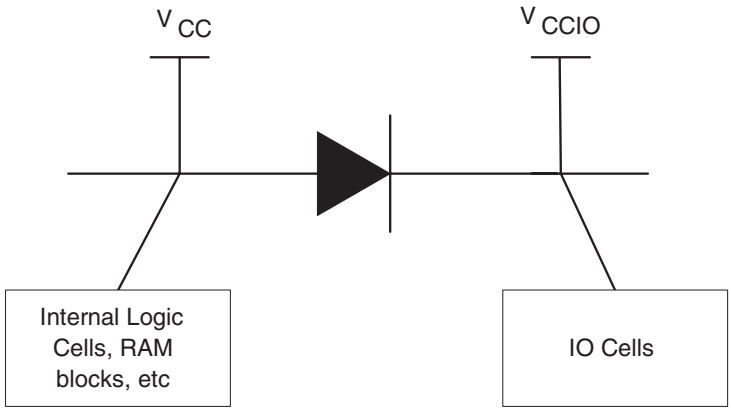


Figure 9: Internal Diode Between VCC and VCCIO

JTAG

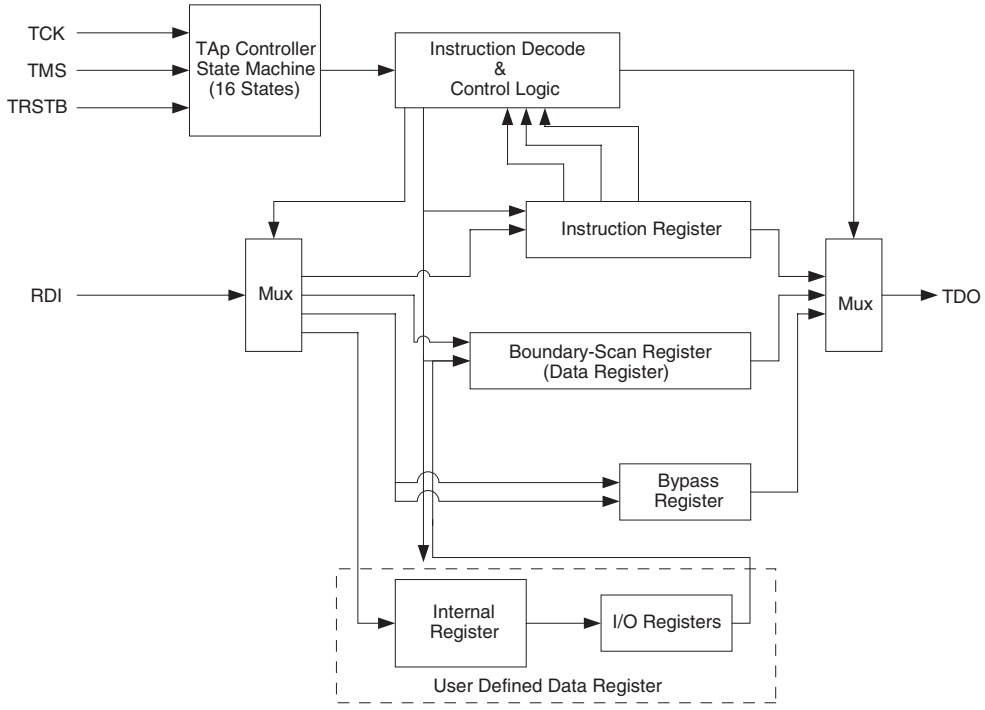


Figure 10: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges. One of these challenges concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The JTAG 1149.1 standard requires the following three tests:

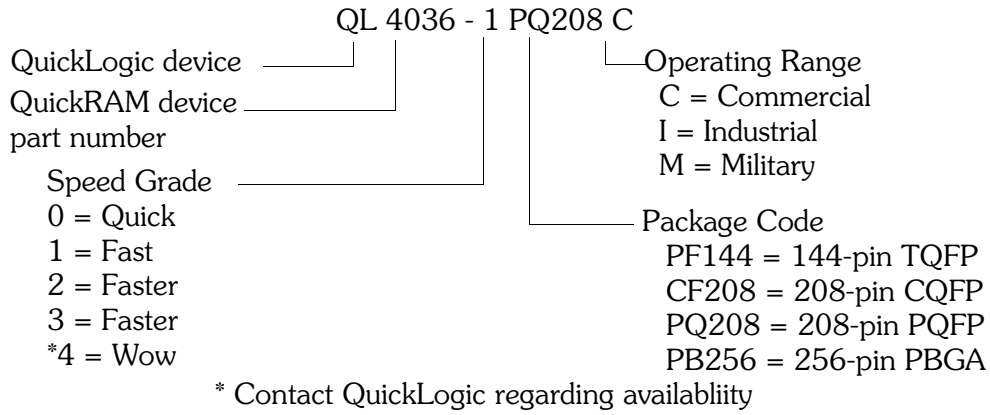
- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register connects the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 12: Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG /RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused.
TRSTB/RRO	Active low Reset for JTAG /RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO/RCO	Test data out for JTAG /RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.
GND/THERM	Ground/Thermal pin	Available on 456-PBGA only. Connect to ground plane on PCB if heat sinking desired. Otherwise may be left unconnected.

Ordering Information



144 TQFP and 208 PQFP/CQFP Pinout Diagrams

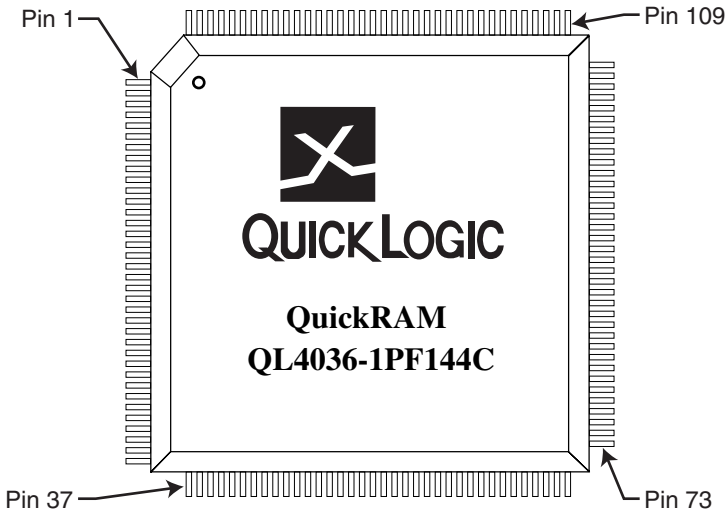


Figure 11: Top View of 144 Pin TQFP

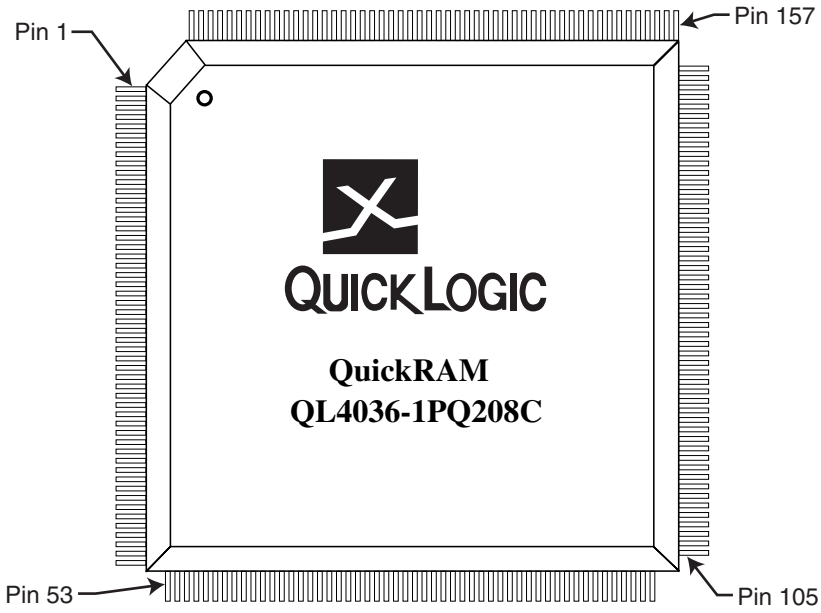


Figure 12: Top View of 208 Pin PQFP/CQFP

144 TQFP and 208 PQFP/CQFP Pinout Table

Table 13: 144 TQFP and 208 PQFP/CQFP Pinout Table

208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function
1	NC	I/O	43	30	GND	85	60	I/O	127	87	GND	169	117	I/O
2	1	I/O	44	31	I/O	86	61	I/O	128	88	I/O	170	118	I/O
3	2	I/O	45	NC	I/O	87	NC	I/O	129	89	GCLK / I	171	119	I/O
4	3	I/O	46	32	I/O	88	62	I/O	130	90	ACLK / I	172	120	I/O
5	NC	I/O	47	NC	I/O	89	63	I/O	131	91	VCC	173	NC	I/O
6	4	I/O	48	33	I/O	90	NC	I/O	132	92	GCLK / I	174	NC	I/O
7	5	I/O	49	NC	I/O	91	NC	I/O	133	93	GCLK / I	175	121	I/O
8	NC	I/O	50	34	I/O	92	64	I/O	134	94	VCC	176	NC	I/O
9	6	I/O	51	35	I/O	93	NC	I/O	135	95	I/O	177	122	GND
10	7	VCC	52	36	I/O	94	65	I/O	136	NC	I/O	178	123	I/O
11	NC	I/O	53	37	I/O	95	66	GND	137	96	I/O	179	124	I/O
12	NC	GND	54	38	TDI	96	67	I/O	138	NC	I/O	180	NC	I/O
13	8	I/O	55	39	I/O	97	NC	VCC	139	97	I/O	181	125	I/O
14	NC	I/O	56	NC	I/O	98	NC	I/O	140	98	I/O	182	126	GND
15	9	I/O	57	40	I/O	99	68	I/O	141	NC	I/O	183	127	I/O
16	NC	I/O	58	NC	I/O	100	69	I/O	142	99	I/O	184	128	I/O
17	10	I/O	59	NC	GND	101	NC	I/O	143	NC	I/O	185	129	I/O
18	11	I/O	60	41	I/O	102	70	I/O	144	100	I/O	186	NC	I/O
19	12	I/O	61	42	VCC	103	71	TRSTB	145	NC	VCC	187	130	VCCIO
20	13	I/O	62	43	I/O	104	72	TMS	146	101	I/O	188	131	I/O
21	NC	I/O	63	NC	I/O	105	NC	I/O	147	102	GND	189	132	I/O
22	14	I/O	64	44	I/O	106	73	I/O	148	103	I/O	190	NC	I/O
23	15	GND	65	45	I/O	107	NC	I/O	149	104	I/O	191	133	I/O
24	16	I/O	66	NC	I/O	108	74	I/O	150	NC	I/O	192	134	I/O
25	17	GCLK / I	67	46	I/O	109	75	I/O	151	105	I/O	193	NC	I/O
26	18	ACLK / I	68	47	I/O	110	76	I/O	152	106	I/O	194	135	I/O
27	19	VCC	69	48	I/O	111	77	I/O	153	NC	I/O	195	136	I/O
28	20	GCLK / I	70	NC	I/O	112	NC	I/O	154	107	I/O	196	NC	I/O
29	21	GCLK / I	71	49	I/O	113	78	I/O	155	NC	I/O	197	137	I/O
30	22	VCC	72	NC	I/O	114	79	VCC	156	108	I/O	198	NC	I/O
31	23	I/O	73	50	GND	115	80	I/O	157	109	TCK	199	138	GND
32	NC	I/O	74	51	I/O	116	NC	GND	158	110	STM	200	139	I/O
33	24	I/O	75	52	I/O	117	81	I/O	159	111	I/O	201	NC	VCC
34	NC	I/O	76	NC	I/O	118	82	I/O	160	NC	I/O	202	140	I/O
35	25	I/O	77	53	I/O	119	NC	I/O	161	112	I/O	203	NC	I/O
36	NC	I/O	78	54	GND	120	83	I/O	162	113	I/O	204	141	I/O
37	26	I/O	79	55	I/O	121	NC	I/O	163	NC	GND	205	142	I/O
38	27	I/O	80	56	I/O	122	84	I/O	164	NC	I/O	206	NC	I/O
39	28	I/O	81	NC	I/O	123	85	I/O	165	114	VCC	207	143	TDO
40	NC	I/O	82	57	I/O	124	NC	I/O	166	115	I/O	208	144	I/O
41	NC	VCC	83	58	VCCIO	125	86	I/O	167	116	I/O			
42	29	I/O	84	59	I/O	126	NC	I/O	168	NC	I/O			

256 PBGA Pinout Diagram

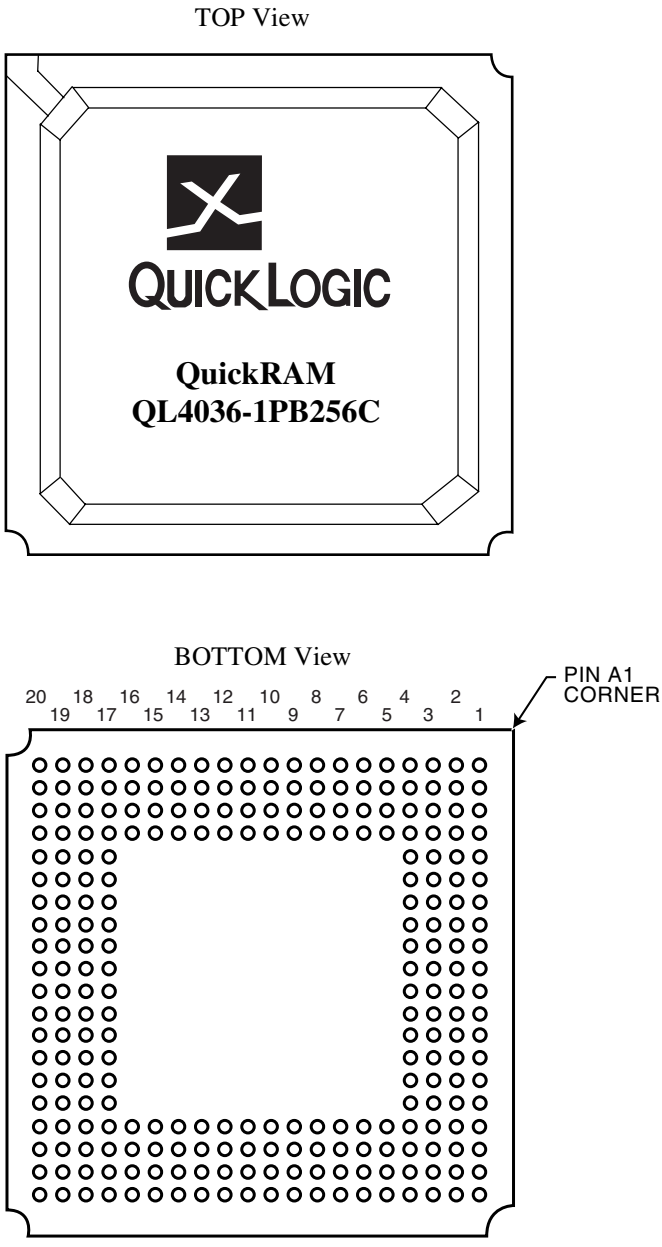


Figure 13: 256 PBGA Pinout Diagram

256 PBGA Pinout Table

Table 14: 256 PBGA Pinout Table

256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function	256 PBGA	Function
A1	VSS	C4	I/O	E19	I/O	L2	ACLK / I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	GCLK / I	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK / I	T19	NC	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	VCC	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	VCCIO	F4	VCC	L19	I/O	U2	I/O	W5	I/O
A7	I/O	C10	I/O	F17	VCC	L20	I/O	U3	I/O	W6	I/O
A8	I/O	C11	I/O	F18	NC	M1	I/O	U4	VSS	W7	I/O
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	I/O	W8	I/O
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	VCC	W9	I/O
A11	I/O	C14	I/O	G1	I/O	M4	NC	U7	I/O	W10	I/O
A12	I/O	C15	I/O	G2	NC	M17	NC	U8	VSS	W11	I/O
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	I/O	W12	I/O
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	VCC	W13	I/O
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	I/O
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	I/O
A17	I/O	C20	I/O	G19	NC	N2	I/O	U13	VSS	W16	I/O
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	I/O	W17	I/O
A19	TCK	D2	I/O	H1	I/O	N4	VSS	U15	VCC	W18	I/O
A20	I/O	D3	I/O	H2	I/O	N17	VSS	U16	I/O	W19	I/O
B1	TDO	D4	VSS	H3	I/O	N18	I/O	U17	VSS	W20	TRSTB
B2	I/O	D5	I/O	H4	VSS	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	VCC	H17	VSS	N20	I/O	U19	I/O	Y2	NC
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	VSS	H19	I/O	P2	I/O	V1	I/O	Y4	I/O
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	NC	Y5	I/O
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	I/O
B8	I/O	D11	VCC	J2	I/O	P17	I/O	V4	I/O	Y7	I/O
B9	I/O	D12	I/O	J3	NC	P18	I/O	V5	I/O	Y8	I/O
B10	I/O	D13	VSS	J4	I/O	P19	NC	V6	I/O	Y9	I/O
B11	I/O	D14	I/O	J17	NC	P20	I/O	V7	I/O	Y10	I/O
B12	I/O	D15	VCC	J18	I/O	R1	NC	V8	I/O	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	I/O	Y12	I/O
B14	I/O	D17	VSS	J20	GCLK / I	R3	I/O	V10	I/O	Y13	I/O
B15	I/O	D18	I/O	K1	I/O	R4	VCC	V11	I/O	Y14	I/O
B16	I/O	D19	I/O	K2	I/O	R17	VCC	V12	VCCIO	Y15	I/O
B17	NC	D20	I/O	K3	I/O	R18	I/O	V13	I/O	Y16	I/O
B18	STM	E1	NC	K4	VCC	R19	I/O	V14	I/O	Y17	I/O
B19	NC	E2	I/O	K17	GCLK / I	R20	I/O	V15	I/O	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK / I	T1	NC	V16	I/O	Y19	I/O
C1	I/O	E4	I/O	K19	GCLK / I	T2	I/O	V17	I/O	Y20	NC
C2	I/O	E17	I/O	K20	NC	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	GCLK / I	T4	NC	V19	TMS		

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Revision History

Table 15: Revision History

Revision	Date	Comments
A	not avail.	First release.
B	not avail.	
C	not avail.	
D	not avail.	
E	not avail.	
F	May 2000	Update of AC/DC Specs and reformat
G	May 2002	Added Kfactor, Power-up, JTAG and mechanical drawing information. Reformatted.

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