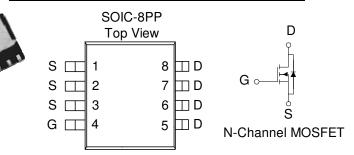
N-Channel 80-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low $r_{DS(on)}$ provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	$I_{D}(A)$		
80	$11 @ V_{GS} = 10V$	18		
	13 @ V _{GS} = 4.5V	17		



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Maximum	Units		
Drain-Source Voltage			80	V		
Gate-Source Voltage			20	V		
Continuous Drain Current ^a	$T_A=25^{\circ}C$		18			
Continuous Drain Current	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	ъ	15	A		
Pulsed Drain Current ^b			50			
Continuous Source Current (Diode Conduction) ^a		I_S	2.3	A		
Paragraphic and a second a second and a second a second and a second a	$T_A=25^{\circ}C$	D_	5.0	w		
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	L D	3.2	**		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
a	$t \ll 10 \sec$	$R_{ heta JA}$	25	°C/W		
Maximum Junction-to-Ambient ^a	Steady State		65	°C/W		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Analog Power AM7482N

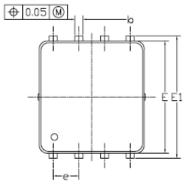
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
D	C11	T. 4 C. 122	Limits			TT •4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{\rm DS} = V_{\rm GS}, I_{\rm D} = 250{\rm uA}$	1			V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 12 \text{ V}$			100	nA	
Zara Cata Valtaga Prain Current	I _{DSS}	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			5		
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			A	
D : G . C . D : A		$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$			11	mΩ	
Drain-Source On-Resistance ^A	fDS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			13		
Forward Tranconductance ^A	gfs	$V_{DS} = 15 \text{ V}, I_{D} = 6 \text{ A}$		40		S	
Diode Forward Voltage	V_{SD}	$I_S = 2.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.7		V	
Dynamic ^b							
Total Gate Charge	Qg	V- 15 V V- 45 V		60		nC	
Gate-Source Charge	Qgs	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_{D} = 6 \text{ A}$		20			
Gate-Drain Charge	Q_{gd}	ID = 0 A		30		1	
Turn-On Delay Time	t _{d(on)}			17			
Rise Time	t _r	$V_{\rm DD} = 15 \; \text{V}, R_{\rm L} = 6 \; \Omega \; \; , \text{ID} = 1 \; \text{A},$		50		nS	
Turn-Off Delay Time	t _{d(off)}	VGEN = 10 V		200			
Fall-Time	t_{f}			70			

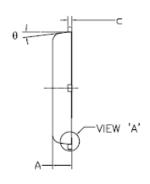
Notes

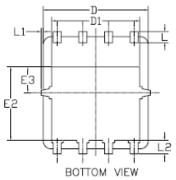
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

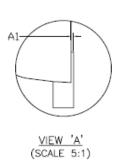
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Package Information









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
SIMBOLS	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.85	0.95	1.00	0.033	0.037	0.039	
A1	0.00		0.05	0.000	0.002		
b	0.30	0.40	0.50	0.012	0.016	0.020	
С	0. 15	0. 20	0. 25	0.006 0.008 0.01			
D		5. 20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC			
Е	5. 55 BSC				0.219 BSC		
E1	6.05 BSC				0.238 BSC		
E2	3. 625 BSC			0.143 BSC			
E3	1. 275 BSC				0.050 BSC		
e	1. 27 BSC				0.050 BSC		
L	0.45	0. 55	0.65	0.018	0.022	0.026	
L1	0		0. 15	0		0.006	
L2	0.68 REF			0.027 REF			
θ	0°		10°	0°		10°	