



UF740

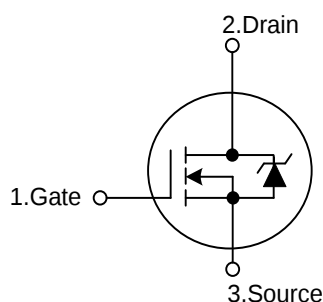
Power MOSFET

**10A, 400V, 0.55Ω N-CHANNEL
POWER MOSFET****DESCRIPTION**

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

- * 10A, 400V, $R_{DS(ON)}$ (0.55Ω)
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF740L-TA3-T	UF740G-TA3-T	TO-220	G	D	S	Tube
UF740L-TF1-T	UF740G-TF1-T	TO-220F1	G	D	S	Tube
UF740L-TF2-T	UF740G-TF2-T	TO-220F2	G	D	S	Tube
UF740L-TF3-T	UF740G-TF3-T	TO-220F	G	D	S	Tube
UF740L-TQ2-T	UF740G-TQ2-T	TO-263	G	D	S	Tube
UF740L-TQ2-R	UF740G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

	(1) R: Tape Reel, T: Tube
	(2) TA3: TO-220, TF1: TO-220F1, TF2: TO-220F2, TF3: TO-220F, TQ2: TO-263
	(3) L: Lead Free, G: Halogen Free

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless Otherwise Specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage ($T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$)		V_{DS}	400	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) ($T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$)		V_{DGR}	400	V
Gate to Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	10	A
	$T_C = 100^\circ\text{C}$	I_D	6.3	A
	Pulsed	I_{DM}	40	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	520	mJ
Power Dissipation	TO-220/TO-263	P_D	125	W
	TO-220F/TO-220F1		44	
	TO-220F2		46	
Derating above 25°C	TO-220/TO-263		1.0	$\text{W}/^\circ\text{C}$
	TO-220F/TO-220F1		0.35	
	TO-220F2		0.37	
Junction Temperature		T_J	+150	$^\circ\text{C}$
Operating Temperature		T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

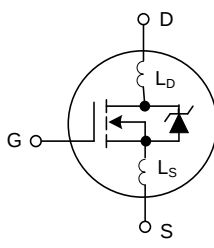
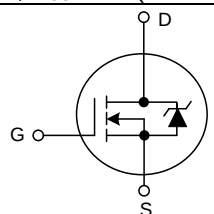
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220/TO-263	θ_{JC}	1.0	$^\circ\text{C}/\text{W}$
	TO-220F/TO-220F1		2.86	
	TO-220F2		2.72	

■ **ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$, Unless Otherwise Specified.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA		400			V
Gate to Threshold Voltage	V _{GS(THR)}	V _{GS} = V _{DS} , I _D = 250μA		2.0		4.0	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V		10			A
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V				25	μA
		V _{DS} =0.8 × Rated BV _{DSS} , V _{GS} =0V, T _J =125°C				250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V				±500	nA
Drain to Source On Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 5.2A (Note 1)			0.38	0.55	Ω
Forward Transconductance	g _{FS}	V _{DS} ≥ 50V, I _D = 5.2A (Note 1)		5.8	8.9		S
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 200V, I _D ≈ 10A, R _{GS} = 9.1Ω, R _L = 20Ω, V _{GS} = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature			65	75	ns
Rise Time	t _R				130	145	ns
Turn-Off Delay Time	t _{DLY(OFF)}				240	260	ns
Fall Time	t _F				145	155	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{G(TOT)}	V _{GS} = 10V, I _D = 10A, I _{G(REF)} = 1.5mA, V _{DS} = 0.8 × Rated BV _{DSS}			138		nC
Gate to Source Charge	Q _{GS}	Gate Charge is Essentially Independent of Operating Temperature			35		nC
Gate to Drain “Miller” Charge	Q _{GD}				35		nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} =25V, f = 1.0MHz			1170		pF
Output Capacitance	C _{OSS}				160		pF
Reverse - Transfer Capacitance	C _{RSS}				26		pF
Internal Drain Inductance	L _D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 		3.5		nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die			4.5		nH
Internal Source Inductance	L _S	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad			7.5		nH
SOURCE TO DRAIN DIODE SPECIFICATIONS							
Source to Drain Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 10A, V _{GS} = 0V (Note 1)				2.0	V
Continuous Source to Drain Current	I _S	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 			10	A	
Pulse Source to Drain Current (Note 2)	I _{SM}				40	A	
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _{SD} = 10A, dI _{SD} /dt = 100A/μs		170	390	790	ns
Reverse Recovery Charge	Q _{RR}	T _J = 25°C, I _{SD} = 10A, dI _{SD} /dt = 100A/us		1.6	4.5	8.2	μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

2. Repetitive rating: Pulse width limited by maximum junction temperature.

3. $V_{DD} = 50V$, starting $T_J = 25^\circ\text{C}$, $L = 9.1mH$, $R_G = 25\Omega$, peak $I_{AS} = 10A$

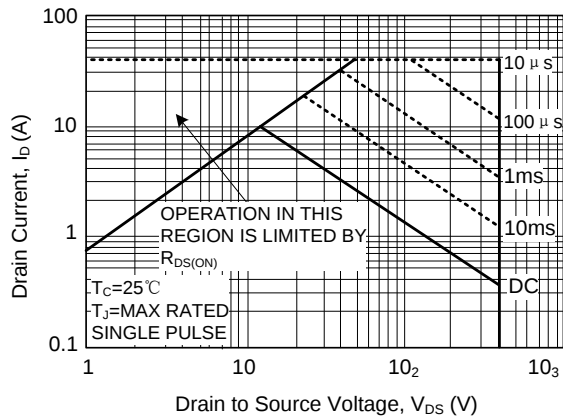
Timing diagram for a MOSFET switching a load. The diagram shows V_{DS} and V_{GS} waveforms. V_{DS} starts at 90%, falls to 10% during $t_{D(ON)}$, stays at 10% during t_R , and then returns to 90% during $t_{D(OFF)}$. V_{GS} starts at 10%, rises to 50% during $t_{D(ON)}$, stays at 50% during t_R , and then falls to 10% during $t_{D(OFF)}$. The pulse width is the time V_{GS} is at 50%. t_{ON} is the time from V_{GS} 10% to V_{DS} 10%. t_{OFF} is the time from V_{DS} 10% to V_{GS} 10%.

The diagram shows a circuit for characterizing a DUT. A 12V BATTERY is connected in series with a 50kΩ resistor and a 0.2μF capacitor. This network is connected to the gate of a MOSFET labeled 'CURRENT REGULATOR'. The drain of the current regulator is connected to the gate of the DUT MOSFET. The DUT MOSFET's source is connected to ground through an I_D CURRENT SAMPLING RESISTOR. The gate of the DUT is also connected to ground through an I_G CURRENT SAMPLING RESISTOR. A pulse waveform is shown at the I_G input, with a peak labeled I_{G(REF)}. The DUT's drain is connected to a V_{DS} (ISOLATED SUPPLY) terminal. The DUT is labeled 'SAME TYPE AS DUT'.

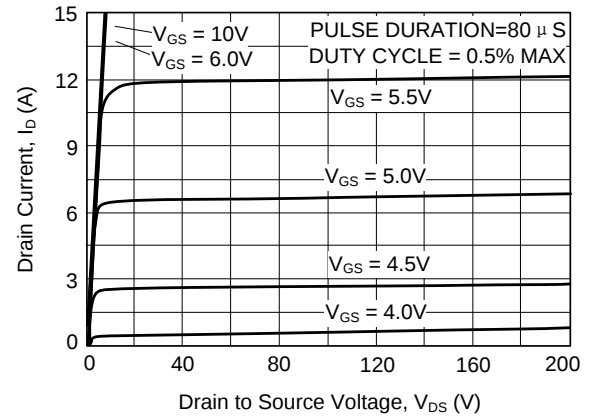
4 of 6
QW-R502-078. G

TYPICAL PERFORMANCE CUVES

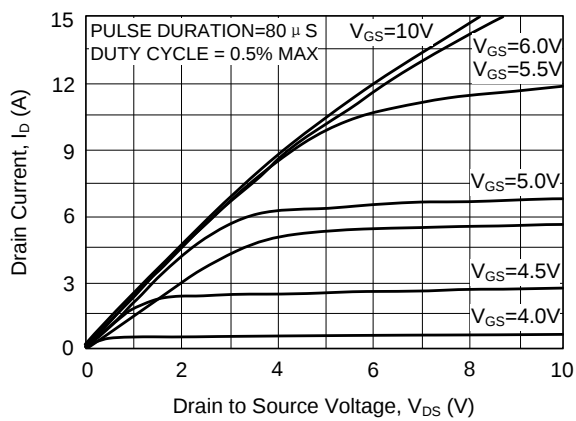
Forward Bias Safe Operating Area



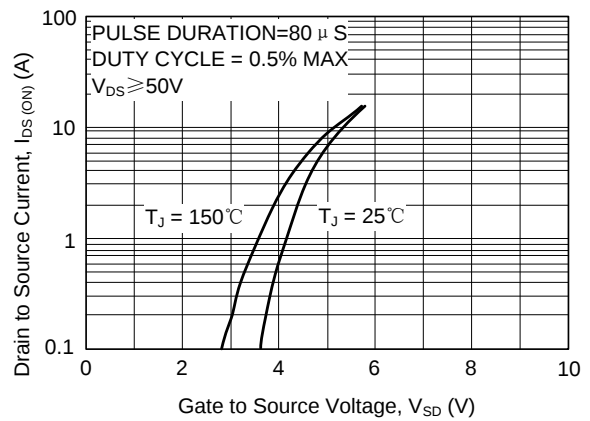
Output Characteristics



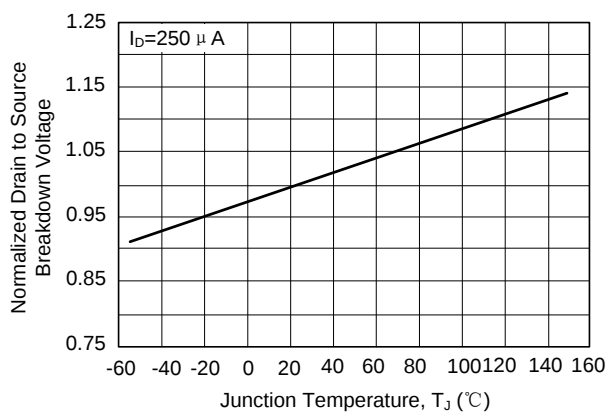
Saturation Characteristics



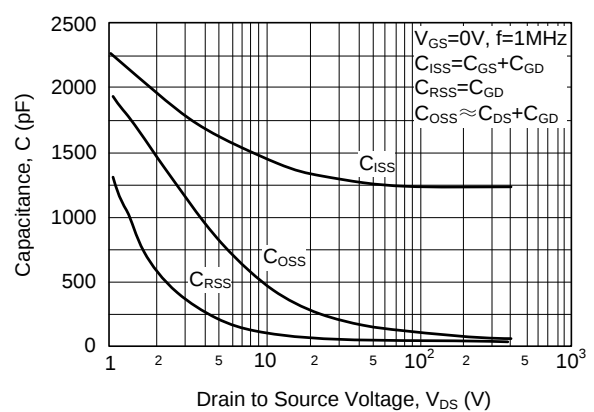
Transfer Characteristics



Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

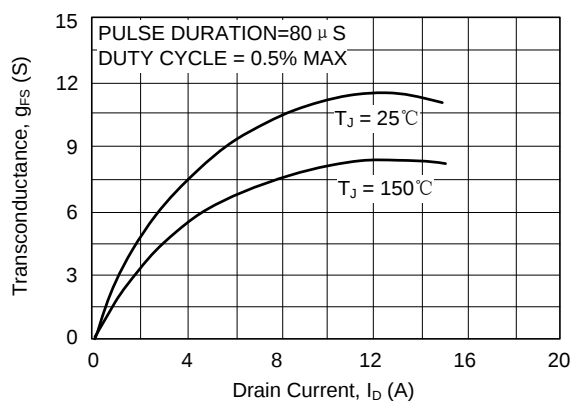


Capacitance vs. Drain to Source Voltage

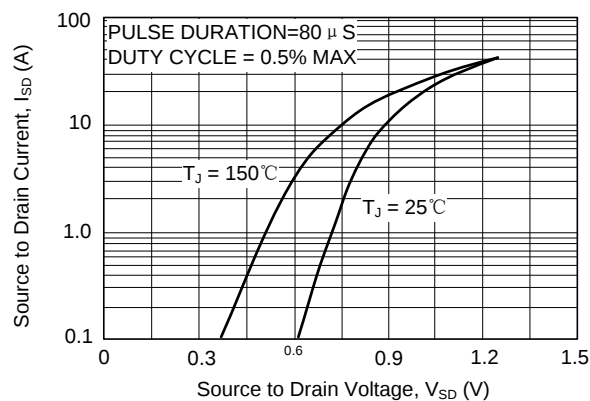


■ TYPICAL PERFORMANCE CUVES (Cont.)

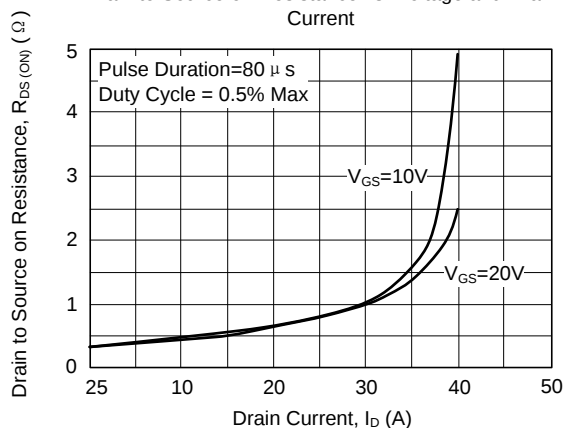
Transconduce vs. Drain Current



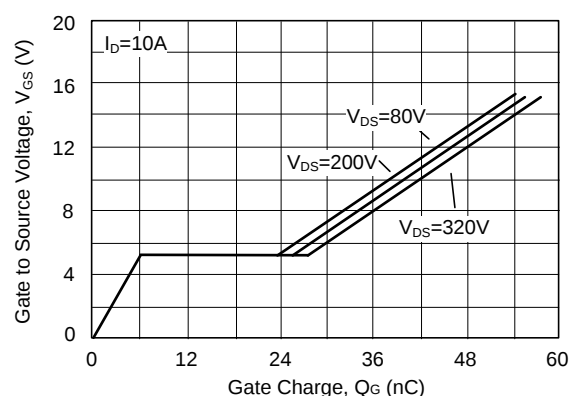
Source to Drain Diode Voltage



Drain to Source on Resistance vs. Voltage and Drain Current



Gate to Source Voltage vs. Gate Charge



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.