AN8050S

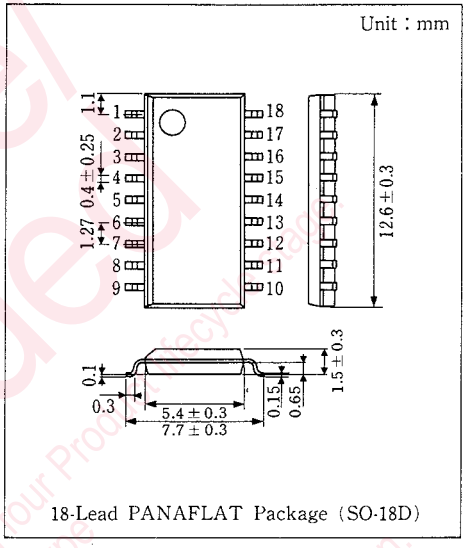
IC for CD Multi Regulator

■ Outline

The AN8050S is an integrated circuit designed for CD multi regulator. It provides +5V and −4.3V regulator output as well as two sets of dual tracking ±5V regulator.

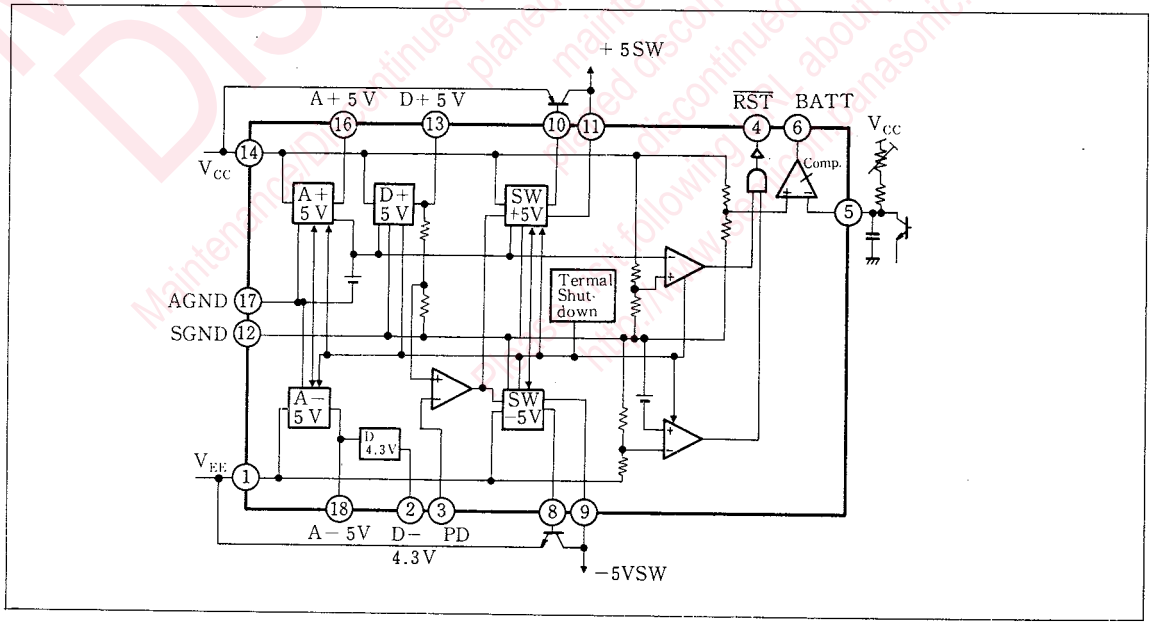
■ Features

- ±5V, tracking regulator
  (±80mA and ±200mA with external transistor)
  +5V(50mA)
- Low voltage drop.
- −4.3V (10mA) output
- Reduced voltage sensing comparator built-in
- Thermal protector built-in.(Thermal Shut Down Circuit)



18-Lead PANAFLAT Package (SO-18D)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{EE}	10	+5V Output
2	D−4.3V (4.3V Output)	11	Tr. Collector
3	Power Down	12	GND
4	Reset Signal Output	13	D+5V Output
5	Comp. Input	14	V_{CC}
6	Comp. Output	15	NC
7	NC	16	A+5V Output
8	−5V Output	17	Audio GND
9	Tr. Collector	18	A−5V

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	10	V
	V_{EE}	−10	
Supply Current	I_{CC}	160	mA
	I_{EE}	−100	
Power Dissipation	P_D	420	mW
Power Down Pin Applied Voltage Tolerance	V_{3tol}	−0.3∼V_{CC}	V
Comparator Pin Applied Voltage Tolerance	V_{5tol}	−0.3∼V_{CC}	V
Operating Ambient Temperature	T_{opr}	−20∼+75	℃
Storage Temperature	T_{stg}	−55∼+125	℃

■ Electrical Characteristics (V_{CC}=7V, V_{EE}=−7V, Ta=25℃)

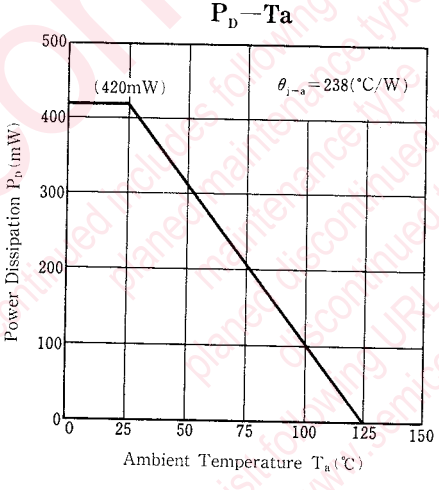
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
+5VA Output Voltage	V_{O16-17}	1	I_O=−50mA	4.75	5.0	5.25	V
−5VA Output Voltage	V_{O18-17}	2	I_O=50mA	−5.25	−5.0	−4.75	V
+5VD Output Voltage	V_{O13-12}	3	I_O=−30mA, V_{EE}=−8V	4.80	5.50	5.30	V
+5VSW Output Voltage	V_{O11-12}	7	PD=0V, I_O=−100mA	4.75	5.0	5.25	V
−5VSW Output Voltage	V_{O9-12}	7	PD=0V, I_O=100mA	−5.30	−5.05	−4.80	V
−4.3VD Output Voltage	V_{O2-17}	2	I_O=2mA	−4.7	−4.3	−3.9	V
+5VA Minimum Input/Output Voltage Difference	V_{DROP16}	1	V_{CC}=5V, V_{EE}=−5V, I_O=−50mA	0		0.3	V
−5VA Minimum Input/Output Voltage Difference	V_{DROP18}	2	V_{CC}=7V, V_{EE}=−5V, I_O=50mA	0		0.3	V
+5VD Minimum Input/Output Voltage Difference	V_{DROP13} *1	3	V_{CC}=5V, V_{EE}=−6V, I_O=−30mA	0		0.3	V
−4.3VD Minimum Input/Output Voltage Difference	V_{DROP2}	2	V_{CC}=7V, V_{EE}=−5V, I_O=2mA	0.4		1.1	V
+5V Maximum Output Current	I_{OP16}	1				−80	mA
−5V Maximum Output Current	I_{OP18}	2		80			mA
+5VD Maximum Output Current	I_{OP13}	3	V_{CC}=7V, V_{EE}=−8V			−50	mA
−4.3VD Maximum Output Current	I_{OP2}	2		5			mA
+5VA Load Regulation	REB_{IL16}	1	I_O=0∼−80mA			80	mV
−5VA Load Regulation	REB_{IL18}	2	I_O=0∼80mA			80	mV
+5VD Load Regulation	REB_{IL13}	3	I_O=0∼−50mA, V_{CC}=7V, V_{EE}=−8V			80	mV
+5VSW Load Regulation	REB_{IL11}	7	I_O=0∼−200mA, T_r. h_{FE}=170			80	mV
−5VSW Load Regulation	REB_{IL9}	7	I_O=0∼200mA, T_r. h_{FE}=170			80	mV
+5VD Line Regulation	REB_{IL16}	1	I_O=−50mA, V_{EE}=−V_{CC}, V_{CC}=5.5V/9V			80	mV

Note) Operating Supply Voltage Range : $V_{CC(opr)}$=±2∼±9V (RST output is not be reversed in this Range.)

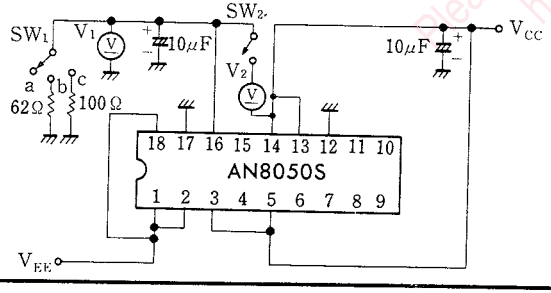
■ Electrical Characteristics (Cont'd) (V_{CC}=7V, V_{EE}=−7V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
−5VA Line Regulation	REB_{IN18}	2	V_{CC}=−V_{EE}'V_{EE}=−5.5/9V,I_O=50mA			80	mV
+5VD Line Regulation	REB_{IN13}*2	3	V_{CC}=5.5V/9V V_{EE}=−6V/−10V, I_O=−30mA			80	mV
+5VSW Line Regulation	REB_{IN11}	7	I_O=−100mA, V_{CC}=−V_{EE}' V_{EE}=−7V/−9V			80	mV
−5VSW Line Regulation	REB_{IN9}	7	V_{CC}=−V_{EE}'V_{EE}=−5.5/−9V,I_O=100mA			80	mV
−4.3VD Line Regulation	REB_{IN2}	2	V_{CC}=−V_{EE}'V_{EE}=−5.5/−9V,I_O=2mA			80	mV
Quiescent Current	I_Q	6			10	18	mA
Bias Current+Side at Load	I_{QL}	6				30	mA
Reset Output "H" Level	$V_{OR(H)}$	4	V_{CC}=7V, V_{EE}=−8V, I_O=−10μA	4.0	4.8	5.25	V
Reset Output "L" Level	$V_{OR(L)}$	4	V_{CC}=4V, V_{EE}=−4.1V, I_O=0.5mA	0	0.5	0.8	V
RST Reduced Voltage Sensing(+)	V_{CCRES}	4	V_{EE}=−7V	4.6	4.8	5.0	V
RST Reduced Voltage Sensing(−)	V_{EERES}	4	V_{CC}=7V	−4.8	−4.6	−4.4	V
BATT COMP Operating Voltage	V_{COMP}	4	V_{CC}=7V, V_{EE}=−8V	2.80	2.92	3.04	V
Battery Indicated Output "H" Level	$V_{BATT(H)}$	4	I_O=10μA, V_{CC}=7V, V_{EE}=−8V	4.0	4.8	5.25	V
Battery Indicated Output "L" Level	$V_{BATT(L)}$	4	I_O=10μA, V_{CC}=7V, V_{EE}=−8V	0	0.5	0.8	V
Power Down Operating Voltage "H" Level	$V_{PD(H)}$	5	V_{CC}=7V, V_{EE}=−8V	3.0			V
Power Down Operating Voltage "L" Level	$V_{PD(L)}$	5	V_{CC}=7V, V_{EE}=−8V			1.2	V
Base Voltage at Power Down Operation −5VSW	V_{10PD}	5	V_{CC}=7V, V_{EE}=−8V	6.9			V

Note) Operating Supply Voltage Range : $V_{CC(OPR)}$=±2~±9V (RST output is not be reversed in this range.)

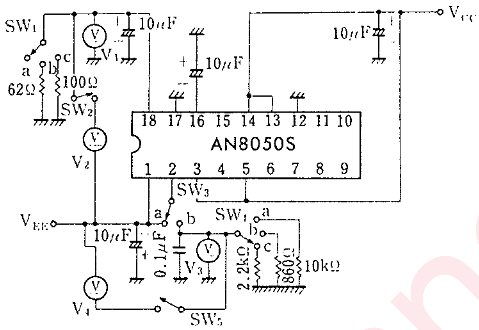


Test Circuit 1 (V_{O16-17}, V_{DROP16}, I_{OP16}, REG_{IL16}, REG_{IN16})



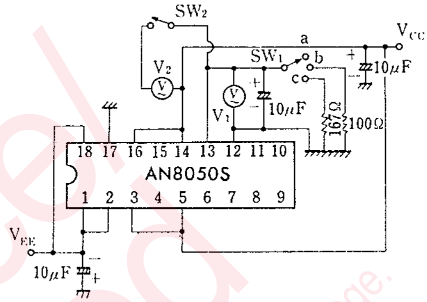
Symbol	Test	Condition			
		V_{CC}	V_{EE}	SW1	SW2
V_{O16-17}	V1	7V	−7V	c	off
V_{DROP16}	V2	5V	−5V	c	on
REG_{IL16}	V1	7V	−7V	a	off
I_{OP16} / REG_{IL16}	ΔV1	7V	−7V	b	off
REG_{IN16}	V1	9V	−9V	c	off
REG_{IN16}	ΔV1	5.5V	−5.5V	c	off

Test circuit 2 (V_{O18-17}, V_{O2-17}, V_{DROP2}, I_{OP18}, I_{OP2}, REG_{IL18}, REG_{IN18}, REG_{IN2})



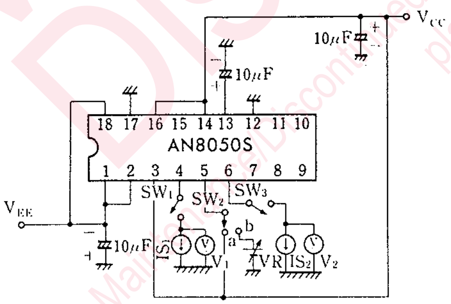
Symbol	Test	Condition						
		V_{CC}	V_{EE}	SW_1	SW_2	SW_3	SW_4	SW_5
V_{O18-17}	V_1	7V	−7V	c	off	a	c	off
V_{DROP18}	V_2	7V	−5V	c	on	a	c	off
I_{OP18} REG_{IL18}	V_1	7V	−7V	a	off	a	c	off
I_{OP18} REG_{IL18}	ΔV_1	7V	−7V	b	off	a	c	off
REG_{IN18}	V_1	9V	−9V	c	off	a	c	off
REG_{IN18}	ΔV_1	5.5V	−5.5V	c	off	a	c	off
V_{O2-17}	V_3	7V	−7V	a	off	b	c	off
V_{DROP2}	V_4	7V	−5V	a	off	b	c	on
I_{OP2}	V_3	7V	−7V	a	off	b	b	off
REG_{IN2}	V_3	9V	−9V	a	off	b	c	off
REG_{IN2}	ΔV_3	5.5V	−5.5V	a	off	b	c	off

Test Circuit 3 (V_{O13-12}, V_{DROP13}, I_{OP13}, REG_{IL13}, REG_{IN13})



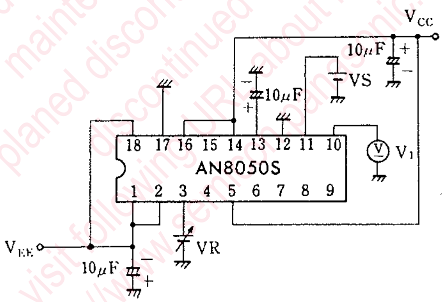
Symbol	Test	Condition			
		V_{CC}	V_{EE}	SW1	SW2
V_{O13-12}	V_1	7V	−8V	c	off
V_{DROP13}	V_2	5V	−6V	c	on
REG_{IL13}	V_1	7V	−8V	a	off
I_{OP13} REG_{IL13}	ΔV_1	7V	−8V	b	off
REG_{I13}	V_1	9V	−10V	c	off
REG_{I13}	ΔV_1	5.5V	−6V	c	off

Test Circuit 4 ($V_{OR(H)}$, $V_{OR(L)}$, $V_{CC\ RES}$, V_{EERES}, V_{COMP}, $V_{BATT(H)}$, $V_{BATT(L)}$)



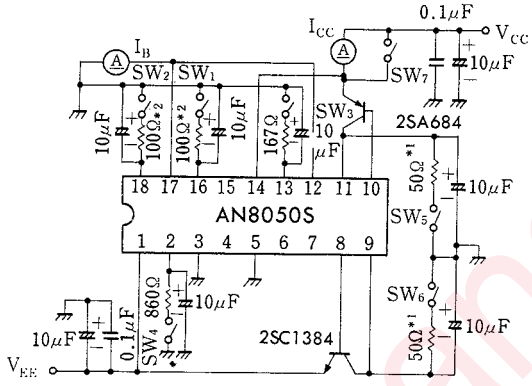
Symbol	Test	Condition									
		V_{CC}	V_{EE}	SW_1	SW_2	SW_3	IS_1	VR	IS_2	V_1	V_2
$V_{OR(H)}$	V_1	7V	−8V	on	a	off	−10μA	—	—	—	—
$V_{OR(L)}$	V_1	4V	4.1V	on	a	off	0.5mA	—	—	—	—
$V_{CC\ RES}$	V_{CC}	—	−7V	on	a	off	0mA	—	—	≦0.8V	—
$V_{EE\ RES}$	V_{EE}	7V	—	on	a	off	0mA	—	—	≦0.8V	—
V_{COMP}	VR	7V	−8V	off	b	on	—	—	0mA	—	≦0.4V
$V_{BATT(H)}$	V_2	7V	−8V	off	b	on	—	1V	−10μA	—	—
$V_{BATT(L)}$	V_2	7V	−8V	off	b	on	—	4V	0.5mA	—	—

Test Circuit 5 ($V_{PD(H)}$, $V_{PD(L)}$, V_{10PD})



Symbol	Test	Condition				
		V_{CC}	V_{EE}	VR	VS	V_1
$V_{PD(H)}$	VR	7V	−8V	—	4.5V	≦5.6V
$V_{PD(L)}$	VR	7V	−8V	—	4.5V	≧6.9V
V_{10PD}	V_1	7V	−8V	7V	4.5V	—

Test Circuit 6 (I_Q, I_{QL})



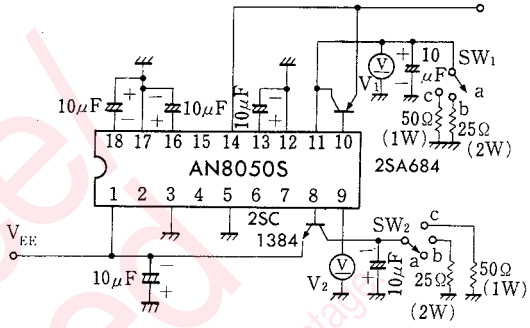
*1 1 W

*2 1/2 W

Symbol	Test	Condition								
		V_{CC}	V_{EE}	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7
I_Q	I_{CC}	7V	−7V	off	off	off	off	off	off	off
I_{QL}	I_{B1}	7V	−7V	off	off	off	off	off	off	on
I_{QL}	I_{B2}	7V	−7V	on	off	on	off	on	off	on

Note) $I_Q = I_{CC}$, $I_{QL} = I_{CC} + I_{B1} - I_{B2}$

Test Circuit 7 ($V_{O11\text{-}12}$, $V_{O9\text{-}12}$, REG_{IL11}, REG_{IL9}, REG_{IN11}, REG_{IN9})



Symbol	Test	Condition			
		V_{CC}	V_{EE}	SW_1	SW_2
$V_{O11\text{-}12}$	V_1	7V	−7V	c	a
REG_{IL11}	V_1	7V	−7V	b	a
REG_{IL11}	ΔV_1	7V	−7V	a	a
REG_{IN11}	V_1	7V	−7V	c	a
REG_{IN11}	ΔV_1	9V	−9V	c	a
$V_{O9\text{-}12}$	V_2	5.5V	−5.5V	a	c
REG_{IL9}	V_2	7V	−7V	a	b
REG_{IL9}	ΔV_2	7V	−7V	a	a
REG_{IL9}	V_2	9V	−9V	a	c
REG_{IN9}	ΔV_2	5.5V	−5.5V	a	c

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