Radiation Hardened CMOS Dual DPST Analog Switch

HS-302RH, HS-302EH

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD Total Dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

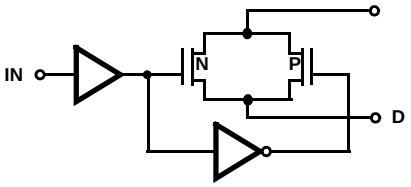
The HS-302RH, HS-302EH analog switches are a monolithic device fabricated using Radiation Hardened CMOS technology and the Intersil dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). These switches offer low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant over the full range of operating voltage and current. ON-resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100kRAD(Si). These devices provide break-before-make switching.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-302RH, HS-302EH are contained in SMD# 5962-95812.

Functional Diagram



TRUTH TABLE

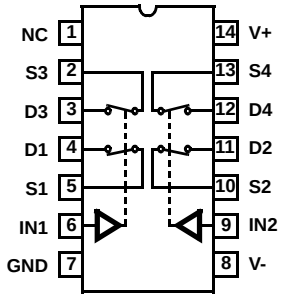
LOGIC	ALL SWITCHES
0	OFF
1	ON

Features

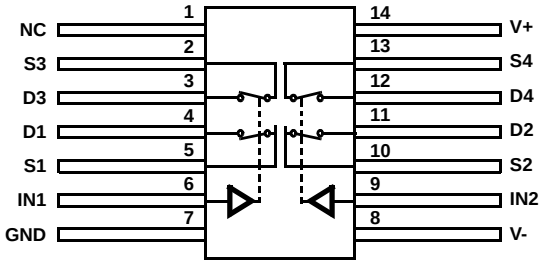
- QML class T, Per MIL-PRF-38535
- Radiation performance
  - Gamma dose (γ) 1 x 10^5 RAD(Si)
- No latch-up, dielectrically isolated device islands
- Pin for pin compatible with Intersil HI-302 series analog switches
- Analog signal range 15V
- Low leakage . . . . . .100nA (Max, Post Rad)
- Low R_{ON} . . . . . .60Ω (Max, Post Rad)
- Low operating power . . . . . .100µA (Max, Post Rad)

Pin Configurations

HS1-302RH, HS1-302EH
(14 LD SBDIP), CDIP2-T14
TOP VIEW



HS9-302RH, HS9-302EH
(14 LD FLATPACK), CDFP3-F14
TOP VIEW



Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant) (Note 1)	PKG. DWG. #
5962R9581201V9A	HS0-302RH-Q	-55 to +125	Die	
5962R9581204V9A	HS0-302EH-Q	-55 to +125	Die	
5962R9581201QCC	HS1-302RH-8	-55 to +125	14 Ld SBDIP	D14.3
5962R9581201VCC	HS1-302RH-Q	-55 to +125	14 Ld SBDIP	D14.3
5962R9581204VCC	HS1-302EH-Q	-55 to +125	14 Ld SBDIP	D14.3
5962R9581201QXC	HS9-302RH-8	-55 to +125	14 Ld Flatpack	K14.A
5962R9581201VXC	HS9-302RH-Q	-55 to +125	14 Ld Flatpack	K14.A
5962R9581204VXC	HS9-302EH-Q	-55 to +125	14 Ld Flatpack	K14.A
HS9-302RH/PROTO	HS9-302RH/PROTO	-55 to +125	14 Ld Flatpack	K14.A
HS0-302RH/SAMPLE	HS0-302RH/SAMPLE	-55 to +125	Die	

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table on page 2 must be used when ordering..

Die Characteristics

DIE DIMENSIONS:

(2130µm x 1930µm x 533µm ±25.4µm)

84 x 76 x 21mils ±1mil

METALLIZATION:

Type: Al

Thickness: 12.5kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (DI)

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

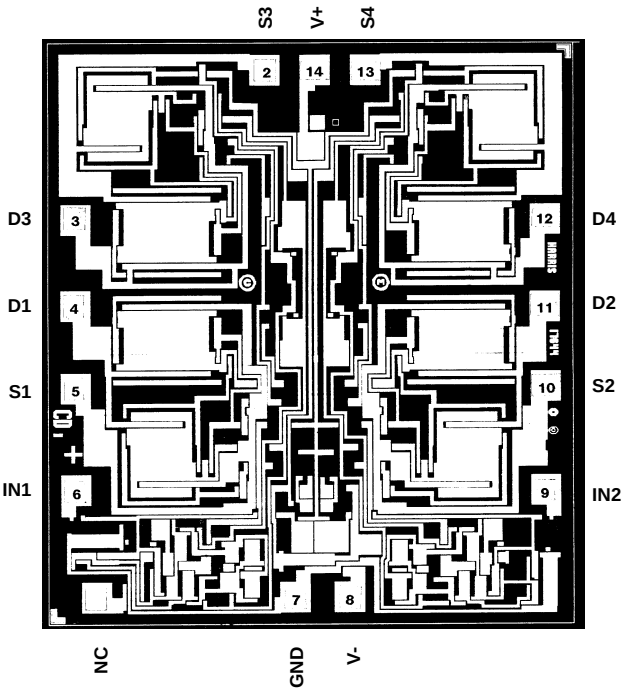
76

PROCESS:

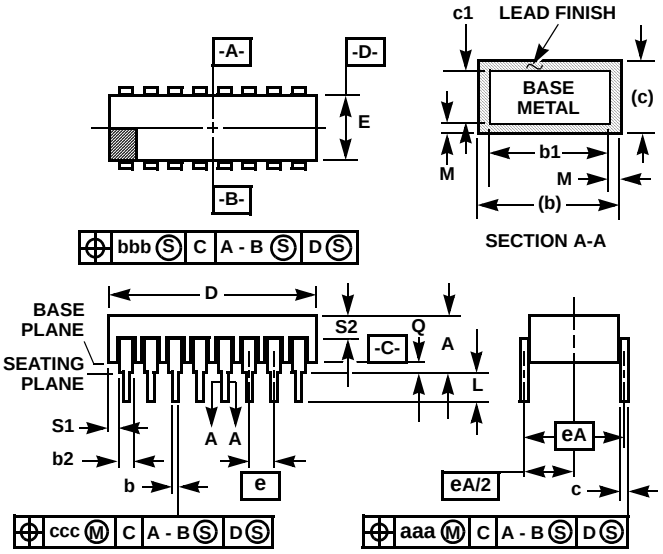
Metal Gate CMOS, Dielectric Isolation

Metallization Mask Layout

HS-302RH, HS-302EH



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

3. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
4. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
6. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
10. N is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
13. Controlling dimension: INCH.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

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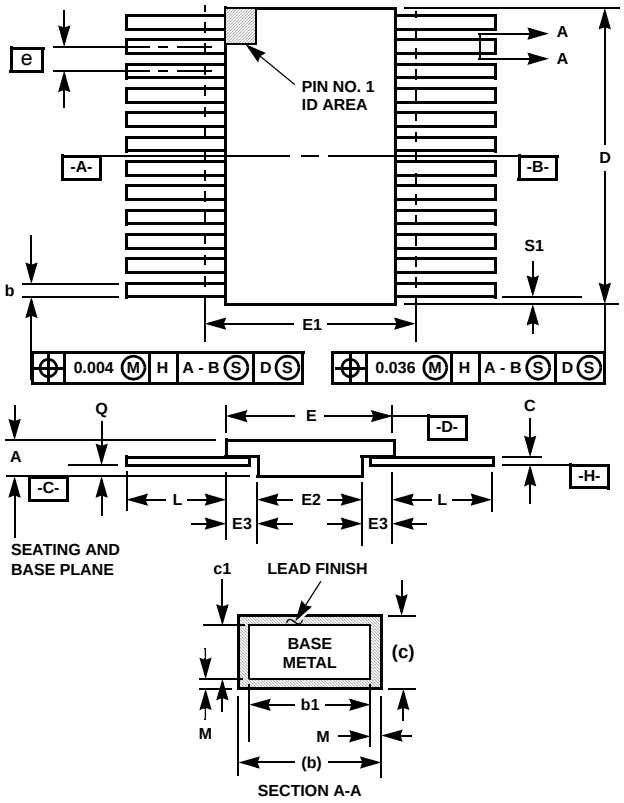
Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.