



Radiation Hardened Ultra High Frequency NPN/PNP Transistor Arrays

ISL73096RH, ISL73127RH, ISL73128RH

The ISL73096RH, ISL73127RH and ISL73128RH are radiation hardened bipolar transistor arrays. The ISL73096RH consists of three NPN transistors and two PNP transistors on a common substrate. The ISL73127RH consists of five NPN transistors on a common substrate. The ISL73128RH consists of five PNP transistors on a common substrate. One of our bonded wafer, dielectrically isolated fabrication processes provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment.

The high gain-bandwidth product and low noise figure of these transistors make them ideal for use in high frequency amplifier and mixer applications. Monolithic construction of the NPN and PNP transistors provides the closest electrical and thermal matching possible. Access is provided to each terminal of the transistors for maximum application flexibility.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-07218. A "hot-link" is provided on our website for downloading.

Features

- Electrically Screened to SMD # 5962-07218
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
 - Gamma Dose (γ) 3×10^5 RAD(Si)
 - SEL Immune . . Bonded Wafer Dielectric Isolation
- NPN Gain Bandwidth Product (F_T) . . . 8GHz (Typ)
- NPN Current Gain (h_{FE}) 130 (Typ)
- NPN Early Voltage (V_A) 50V (Typ)
- PNP Gain Bandwidth Product (F_T) . . . 5.5GHz (Typ)
- PNP Current Gain (h_{FE}) 60 (Typ)
- PNP Early Voltage (V_A) 20V (Typ)
- Noise Figure (50 Ω) at 1GHz 3.5dB (Typ)
- Collector-to-Collector Leakage <1pA (Typ)
- Complete Isolation Between Transistors

Applications

- High Frequency Amplifiers and Mixers
 - Refer to Application Note AN1503
- High Frequency Converters
- Synchronous Detector

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)	PACKAGE (Pb-free)
5962F0721801V9A	ISL73096RHVX	-55 to +125	DIE
5962F0721801VXC	ISL73096RHVF (Notes 1, 2)	-55 to +125	16 LD FLATPACK
5962F0721802V9A	ISL73127RHVX	-55 to +125	DIE
5962F0721802VXC	ISL73127RHVF (Notes 1, 2)	-55 to +125	16 LD FLATPACK
5962F0721803V9A	ISL73128RHVX	-55 to +125	DIE
5962F0721803VXC	ISL73128RHVF (Notes 1, 2)	-55 to +125	16 LD FLATPACK
ISL73096RHF/PROTO	ISL73096RHF/PROTO	-55 to +125	
ISL73096RHX/SAMPLE	ISL73096RHX/SAMPLE	-55 to +125	DIE
ISL73127RHF/PROTO	ISL73127RHF/PROTO	-55 to +125	
ISL73127RHX/SAMPLE	ISL73127RHX/SAMPLE	-55 to +125	DIE

ISL73096RH, ISL73127RH, ISL73128RH

Ordering Information (Continued)

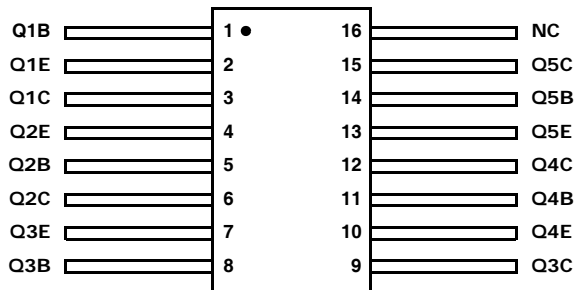
ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)	PACKAGE (Pb-free)
ISL73128RHF/PROTO	ISL73128RHF/PROTO	-55 to +125	
ISL73128RHX/SAMPLE	ISL73128RHX/SAMPLE	-55 to +125	DIE

NOTES:

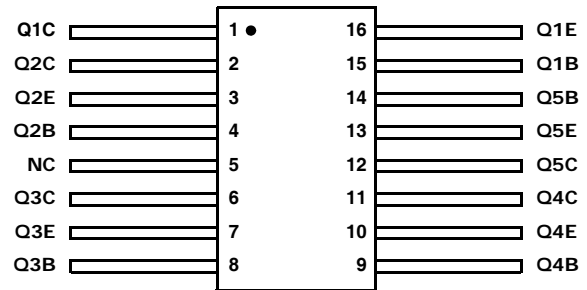
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for [ISL73096RH](#), [ISL73127RH](#), [ISL73128RH](#). For more information on MSL please see techbrief [TB363](#).

Pin Configurations

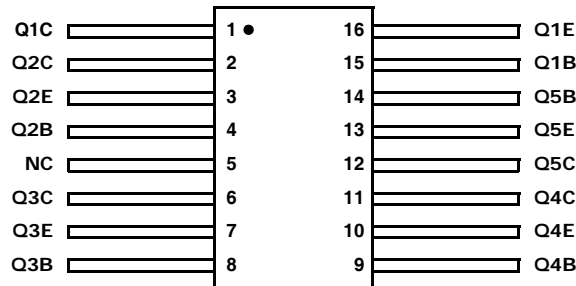
ISL73096RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



ISL73127RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



ISL73128RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



Die Characteristics

DIE DIMENSIONS:

52.8 mils x 52.0 mils x 14 mils ± 1 mil
 1340 μ m x 1320 μ m x 355.6 μ m $\pm 25.4\mu$ m

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
 Thickness: 4k \AA $\pm 0.5\text{k}\text{\AA}$

Top Metallization:

Type: Metal 1: AlCu (2%)/TiW
 Thickness: Metal 1: 8k \AA $\pm 0.5\text{k}\text{\AA}$
 Type: Metal 2: AlCu (2%)
 Thickness: Metal 2: 16k \AA $\pm 0.8\text{k}\text{\AA}$

Substrate:

UHF-1X Bonded Wafer, DI

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Floating

ADDITIONAL INFORMATION:

Worst Case Current Density:

3.04 x 10⁵A/cm²

Transistor Count:

5

Metallization Mask Layout

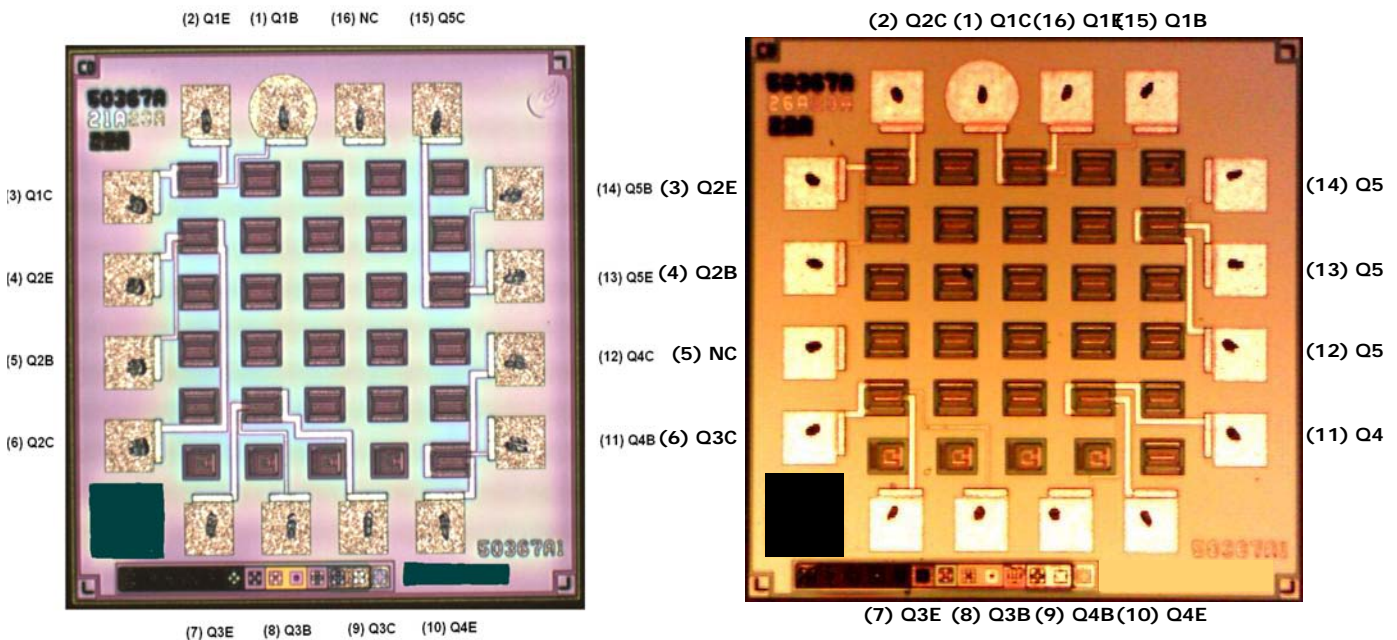


FIGURE 1. ISL73096RH, ISL73127RH

For additional products, see www.intersil.com/product_tree

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Metallization Mask Layout (Continued)

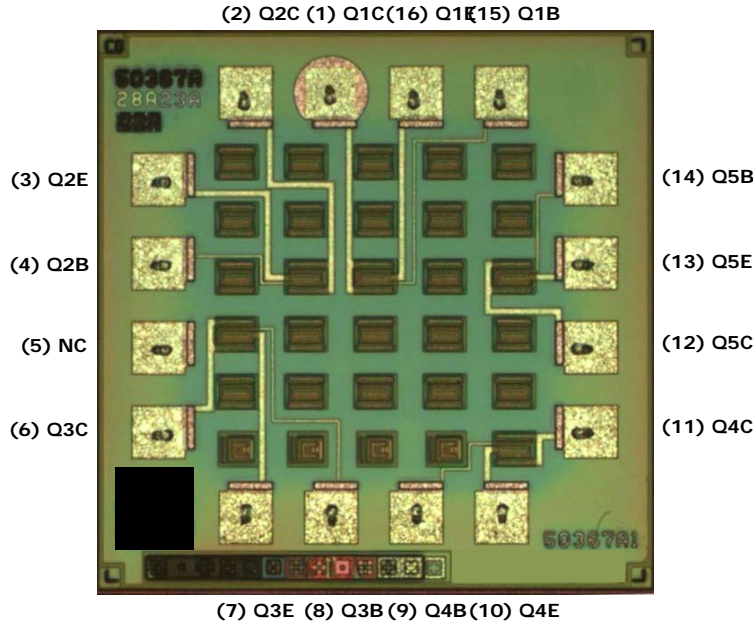


FIGURE 2. ISL73128RH

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
11/12/09	FN6475.3	Converted to new Intersil template. Changed App Note Reference from "AN9315" to "AN1503" to reflect new app note for the radiation hardened product. Updated ordering information with package column, notes to match lead finish and MSL note.
03/23/09	FN6475.2	Under Pinouts, changed DIP symbols to flatpack symbols. Changed (16 LD SBDIP) CDIP2-T16 to (16 LD Flatpack) CDFP4-F16. Under Ordering Information, added the following flatpack device types: 5962F0721801VXC (ISL73096RHVF), 5962F0721802VXC (ISL73127RHVF) and 5962F0721803VXC (ISL73128RHVF).
12/2007	FN6475.1	Added ISL73127RH & ISL73128RH device types.
03/29/07	FN6475.0	Initial Release.

Products

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL73096](http://www.intersil.com/ISL73096), [ISL73127RH](http://www.intersil.com/ISL73127RH), [ISL73128RH](http://www.intersil.com/ISL73128RH)

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