32K x 8 EEPROM - 5 Volt, Byte Alterable

Description

The MYXX28HC256 is a high performance CMOS 32K x 8 E²PROM. It is fabricated with a textured poly floating gate technology, providing a highly reliable 5 Volt only nonvolatile memory.

The MYXX28HC256 supports a 128-byte page write operation, effectively providing a 24ms/byte write cycle and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The MYXX28HC256 also features DATA Polling and Toggle Bit Polling, two methods of providing early end of write detection. The MYXX28HC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the MYXX28HC256 is specified as a minimum 100,000 write cycles per byte and an inherent data retention of 100 years.

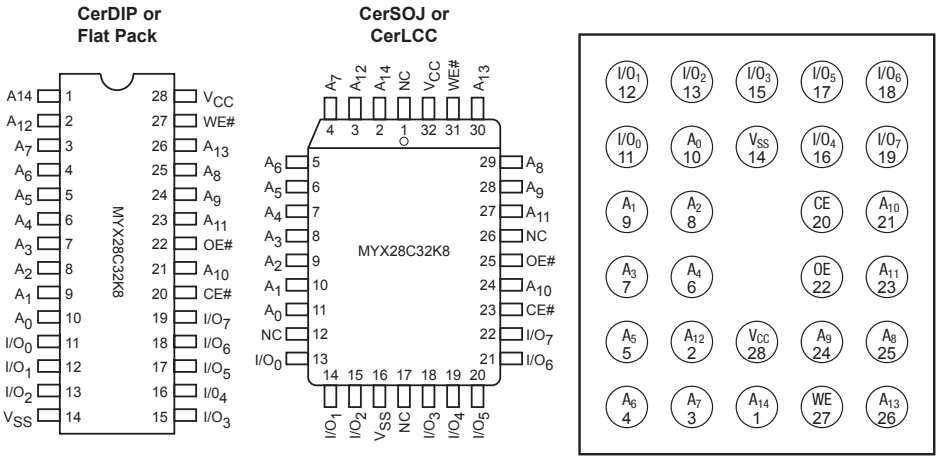


Figure 1 - Pin Configuration

Features

- Access Time (ns): 70, 90, 120, 150
- Simple Byte and Page Write
  - Single 5V Supply
    - *No External High Voltages or VPP Control Circuits*
  - Self-Timed
    - *No Erase Before Write*
    - *No Complex Programming Algorithms*
    - *No Overerase Problem*
- Low Power CMOS:
  - Active: 60mA
  - Standby: 500mA
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 100,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

	Options	Markings
Timing	70 ns access	-7
	90 ns access	-9
	120 ns access	-12
	150 ns access	-15
Packages	Ceramic flat pack	F
	CerDIP, 600 mil	CW
	CerLCC	ECA
	CerPGA	P
	CerSOJ	ECJ
Operating Temp.	Military (-55°C to +125°C)	XT
	Industrial (-40°C to +85°C)	IT

Pin Descriptions

Addresses (A0–A14)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE#)

The Chip Enable input must be LOW to enable all read/write operations. When CE# is HIGH, power consumption is reduced.

Output Enable (OE#)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the MYXX28HC256 through the I/O pins.

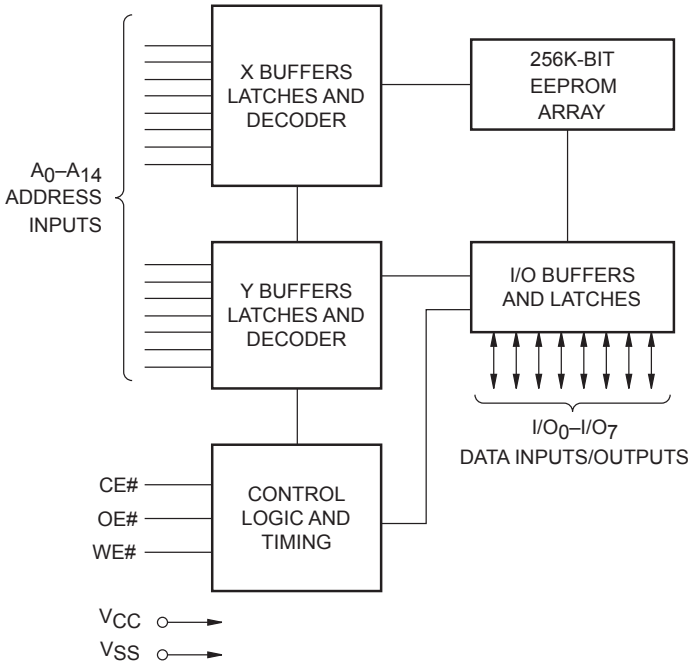
Write Enable (WE#)

The Write Enable input controls the writing of data to the MYXX28HC256.

Table 1 - Pin Names

Parameter	Symbol
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Input/Output
WE#	Write Enable
CE#	Chip Enable
OE#	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Figure 2 - Functional Diagram



Device Operation

Read

Read operations are initiated by both OE# and CE# LOW. The read operation is terminated by either CE# or OE# returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE# or CE# is HIGH.

Write

Write operations are initiated when both CE# and WE# are LOW and OE# is HIGH. The MYXX28HC256 supports both a CE# and WE# controlled write cycle. That is, the address is latched by the falling edge of either CE# or WE#, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE# or WE#, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3ms.

Page Write Operation

The page write feature of the MYXX28HC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the MYXX28HC256 prior to the commencement of the internal programming

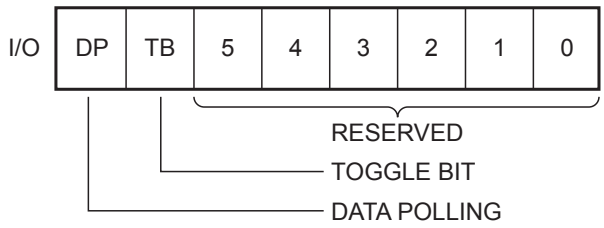
cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A7 through A14) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twentyseven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE# HIGH to LOW transition, must begin within 100ms of the falling edge of the preceding WE#. If a subsequent WE# HIGH to LOW transition is not detected within 100ms, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100ms.

Write Operation Status Bits

The MYXX28HC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 3.

Figure 3 - Status Bit Assignment



DATA Polling (I/O_7)

The MYXX28HC256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the MYXX28HC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The MYXX28HC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

DATA Polling I/O_7

Figure 4 - Data Polling Bus Sequence

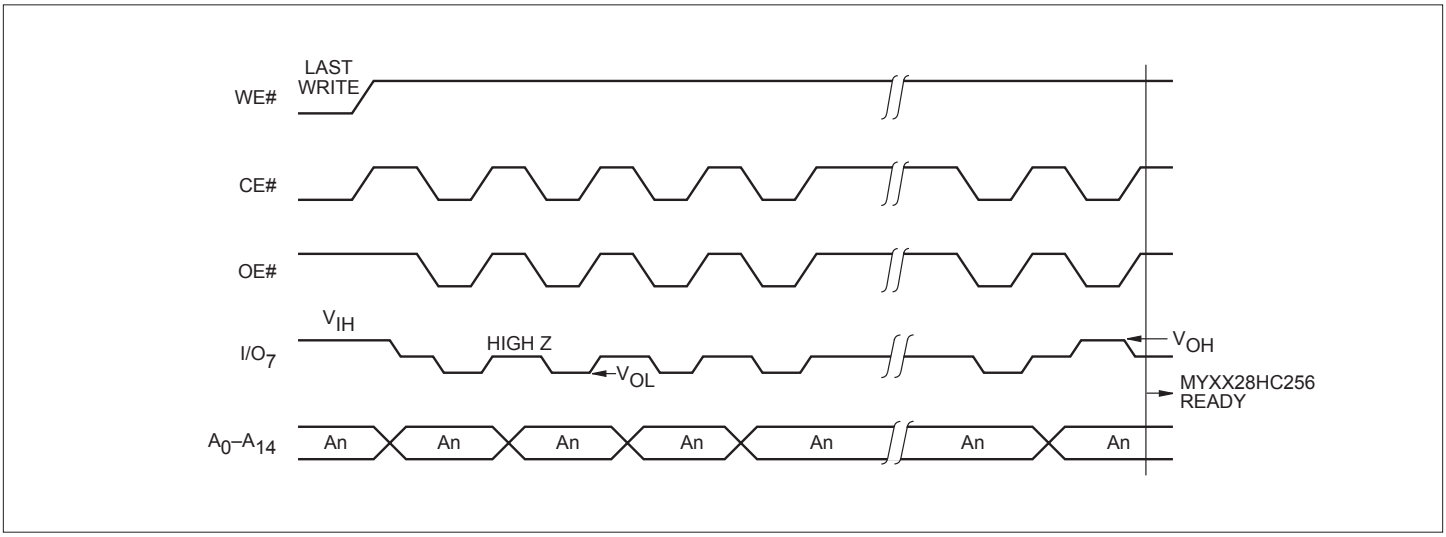
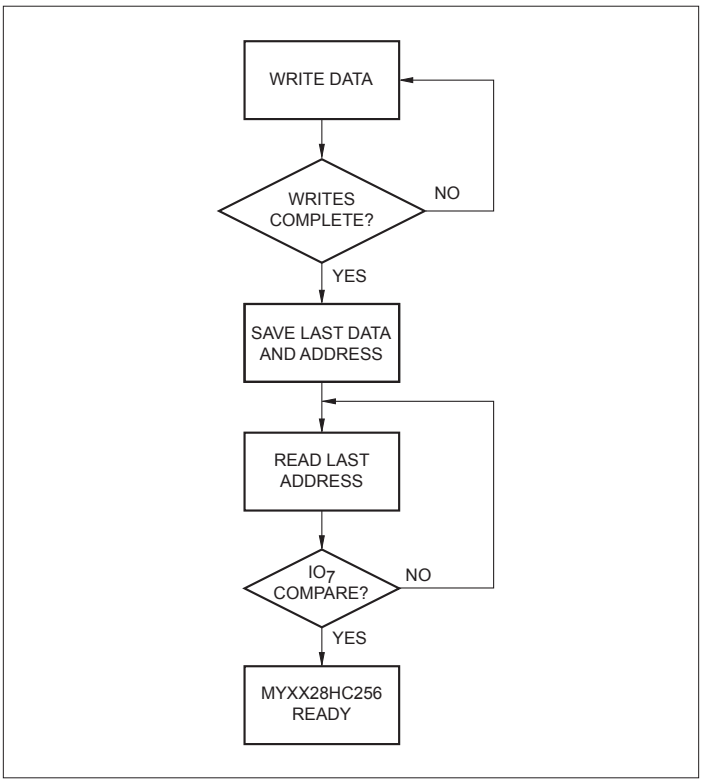


Figure 5 - Data Polling Software Flow



DATA Polling can effectively halve the time for writing to the MYXX28HC256. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 6 - Toggle Bit Bus Sequence

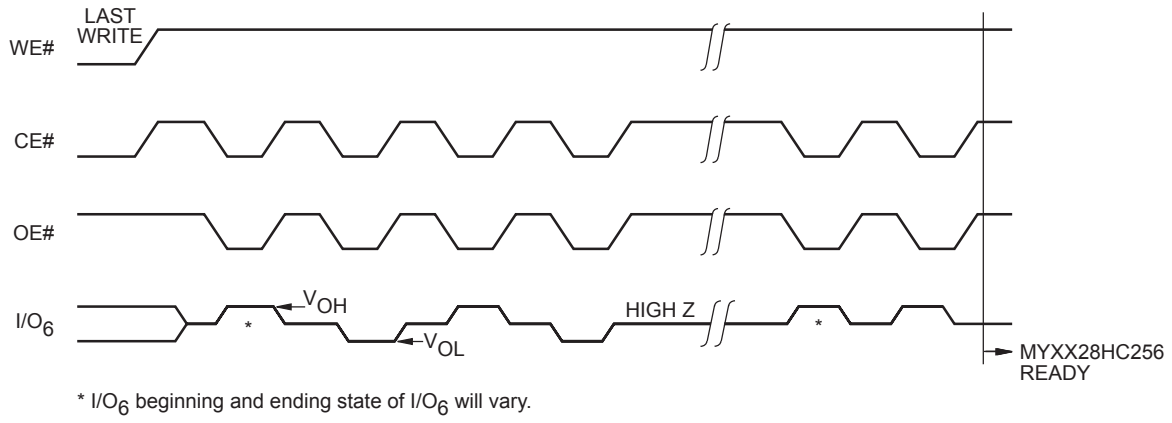
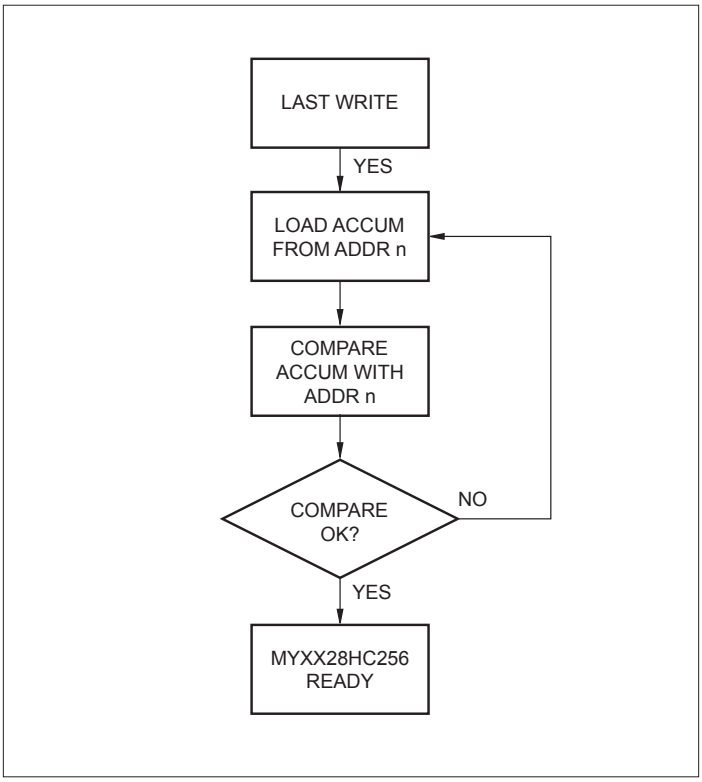


Figure 7 - Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple MYXX28HC256 memories that is frequently updated. The timing diagram in Figure 6 illustrates the sequence of events on the bus. The software flow diagram in Figure 7 illustrates a method for polling the Toggle Bit.

Hardware Data Protection

The MYXX28HC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense - All write functions are inhibited when V_{CC} is $\leq$ 3.5V Typically.
- Write Inhibit - Holding either OE# LOW, WE# HIGH, or CE# HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

Software Data Protection

The MYXX28HC256 offers a software controlled data protection feature. The MYXX28HC256 is shipped from Micross with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable. The MYXX28HC256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the MYXX28HC256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 9 and 10 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

Figure 8 - Timing Sequence - Byte or Page Write

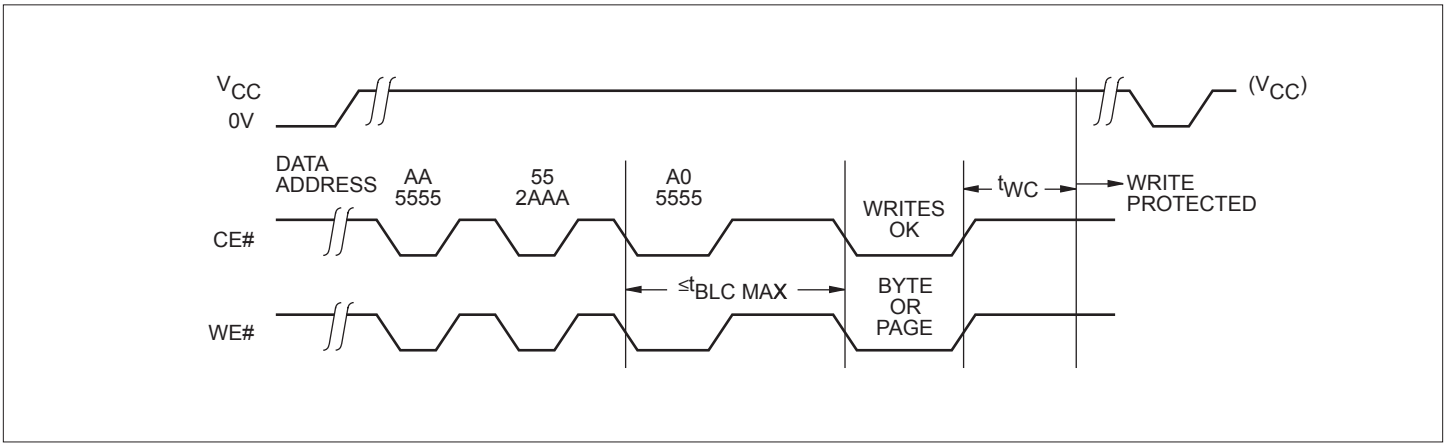
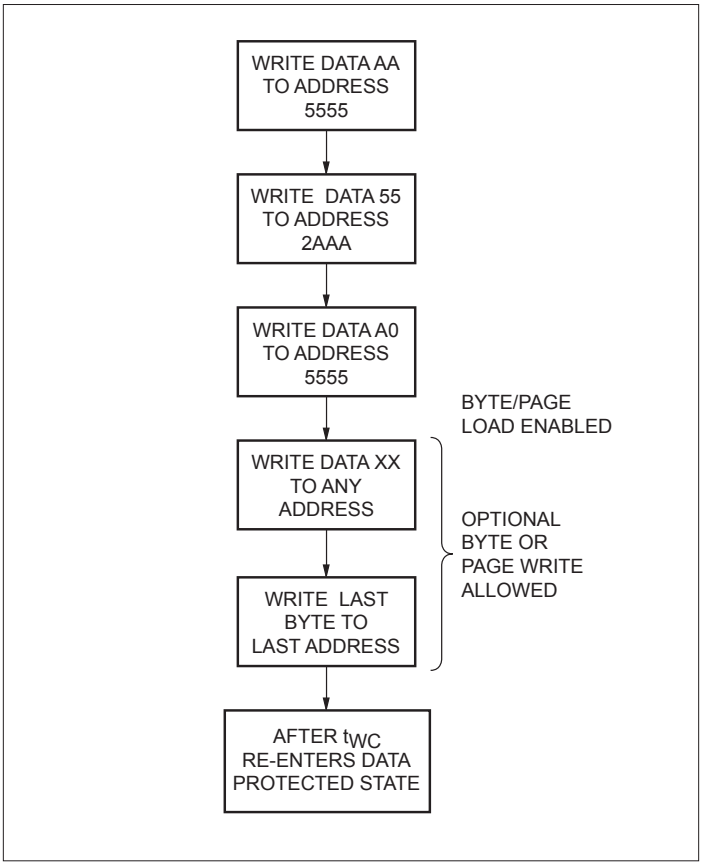


Figure 9 - Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the MYXX28HC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the MYXX28HC256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

Figure 10 - Reset Software Data Protection Timing Sequence

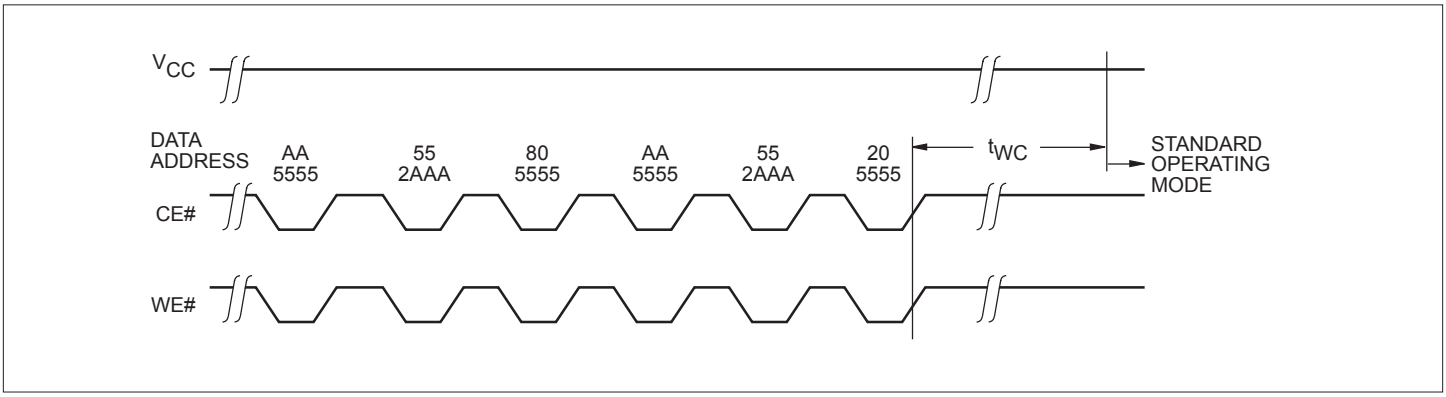
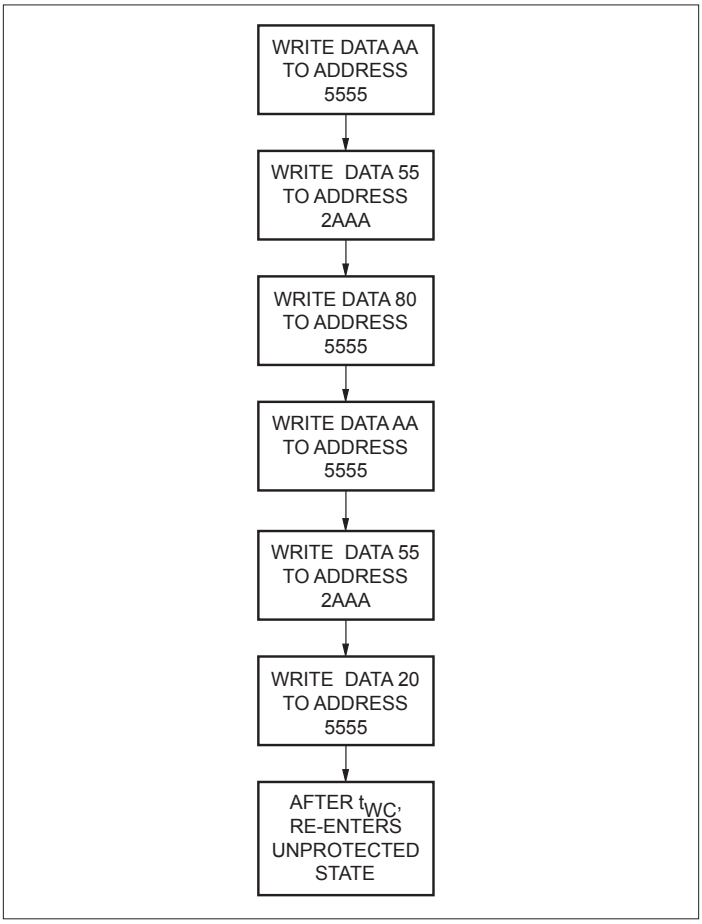


Figure 11 - Write Sequence for Resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the MYXX28HC256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

System Considerations

Because the MYXX28HC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that CE# be decoded from the address bus and be used as the primary device selection input. Both OE# and WE# would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the MYXX28HC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE# will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Table 2 - Absolute Maximum Ratings*

Temperature under bias	-10°C to +85°C
	-65°C to +135°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS}	-1V to +7V
DC output current	10mA
Lead temperature (soldering, 10 sec.)	300°C
Supply voltage	5V ±10%

*Note

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 - Recommended Operating Conditions

Temperature	Min.	Max.
Commerical	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Table 4 - DC Operating Characteristics

Over the recommended operating conditions unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
I_{CC}	V_{CC} Active Current (TTL Inputs)		30	60	mA	CE# = OE# = V_{IL}; WE# = V_{IH} All I/O's = Open; Address Inputs = .4V/2.4V Levels @ f = 10MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	2		CE# = V_{IH}; OE# = V_{IL}; All I/O's = Open; Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		200	500	µA	CE# = V_{CC} - 0.3V; OE# = GND; All I/O's = Open; Other Inputs = V_{CC} - 0.3V
I_{LI}	Input Leakage Current			10		V_{IN} = V_{SS} to V_{CC}; CE# = V_{IH}
I_{LO}	Output Leakage Current			10		V_{OUT} = V_{SS} to V_{CC}; CE# = V_{IH}
V_{IL}[2]	Input LOW Voltage	-1		0.8	V	
V_{IH}[2]	Input HIGH Voltage	2		V_{CC} +1		
V_{OL}	Output LOW Voltage			0.4		I_{OL} = 6mA
V_{OH}	Output HIGH Voltage	2.4				I_{OH} = -4mA

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. V_{IL} min. and V_{IH} max. are for reference only and are not tested.

Table 5 - Power-Up Timing

Symbol	Parameter	Max.	Units
t_{PUR}[1]	Power-Up to Read	100	µs
t_{PUW}[1]	Power-Up to Write	5	ms

1. This parameter is periodically sampled and not 100% tested.

Table 6 - Capacitance

T_A = +25°C; f = 1MHz; V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6		V_{IN} = 0V

Table 7 - Endurance and Data Retention

Parameter	Min.	Max.	Units
Endurance	100,000		Cycles
Data Retention	100		Years

Table 8 - AC Conditions of Test

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

Table 9 - Mode Selection

CE#	OE#	WE#	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
	H	L	Write	D_{IN}	
H	X	X	Standby & Write Inhibit	High Z	Standby
X	L	X	Write Inhibit		
	X	H			

Figure 12 - Equivalent AC Load Circuit

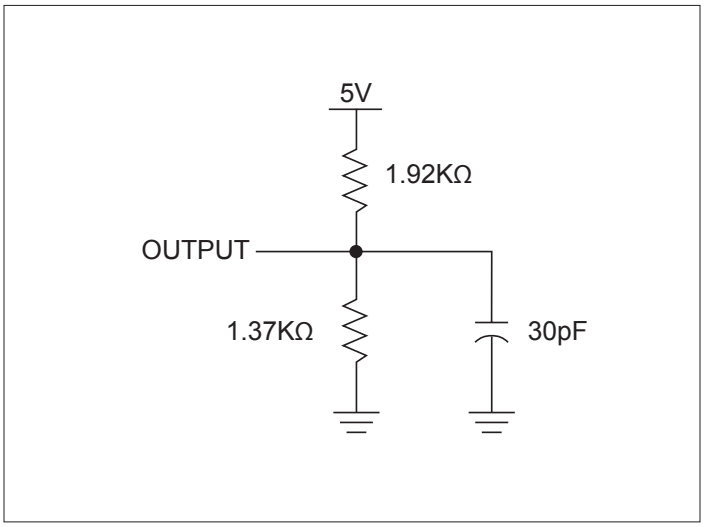


Figure 13 - Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

AC Characteristics

Over the recommended operating conditions unless otherwise specified.

Table 10 - Read Cycle Limits

Symbol	Parameter	MYXX28HC256-70		MYXX28HC256-90		MYXX28HC256-12		MYXX28HC256-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max	
t_{RC}	Read Cycle Time	70		90		120		150		ns
t_{CE}	Chip Enable Access Time		70		90		120		150	
t_{AA}	Address Access Time									
t_{OE}	Output Enable Access Time		35		40		50		50	
t_{LZ}[1]	CE# LOW to Output Active	0		0		0		0		
t_{OLZ}[1]	OE# LOW to Output Active									
t_{HZ}[1]	CE# HIGH to High Z Output		35		40		50		50	
t_{OHZ}[1]	OE# HIGH to High Z Output									
t_{OH}	Output Hold from Address Change	0		0		0		0		

1. t_{LZ} min., t_{HZ}, t_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured, with CL = 5pF, from the point when CE#, OE# return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Figure 14 - Read Cycle

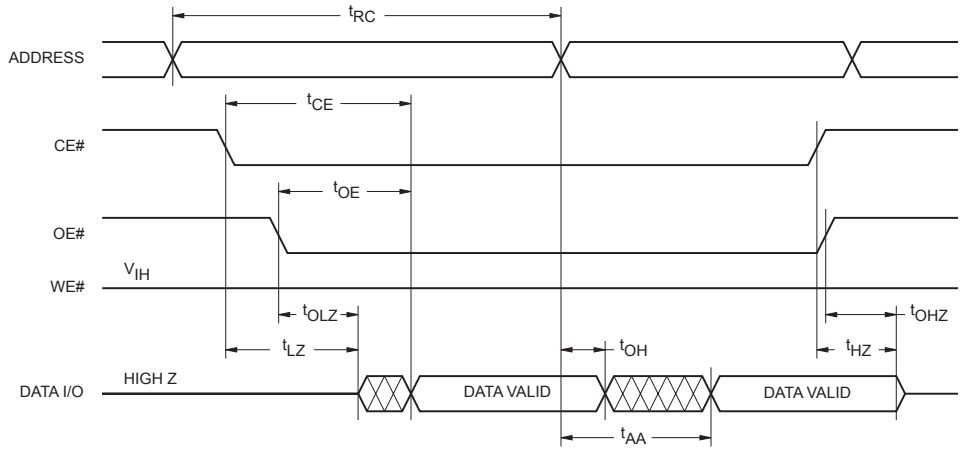


Table 11 - Write Cycle Limits

Symbol	Parameter	Min.	Typ.[1]	Max.	Units
t_{WC}[2]	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			
t_{CS}	Write Setup Time	0			
t_{CH}	Write Hold Time	0			
t_{CW}	CE# Pulse Width	50			
t_{OES}	OE# HIGH Setup Time	0			
t_{OEH}	OE# HIGH Hold Time	0			
t_{WP}	WE# Pulse Width	50			
t_{WPH}[3]	WE# High Recovery (page write only)	50			
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	0			
t_{DW}[3]	Delay to next Write after polling is true	10			µs
t_{BLC}	Byte Load Cycle	0.15		100	

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
3. t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

Figure 15 - WE# Controlled Write Cycle

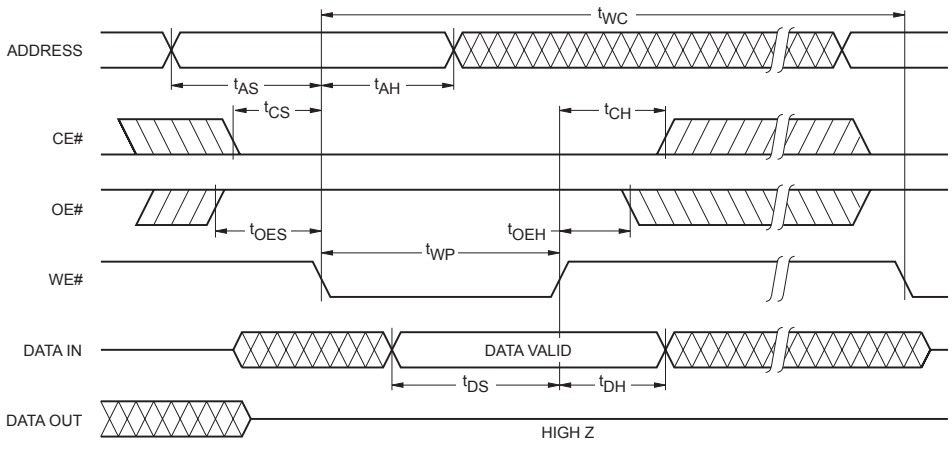


Figure 16 - CE# Controlled Write Cycle

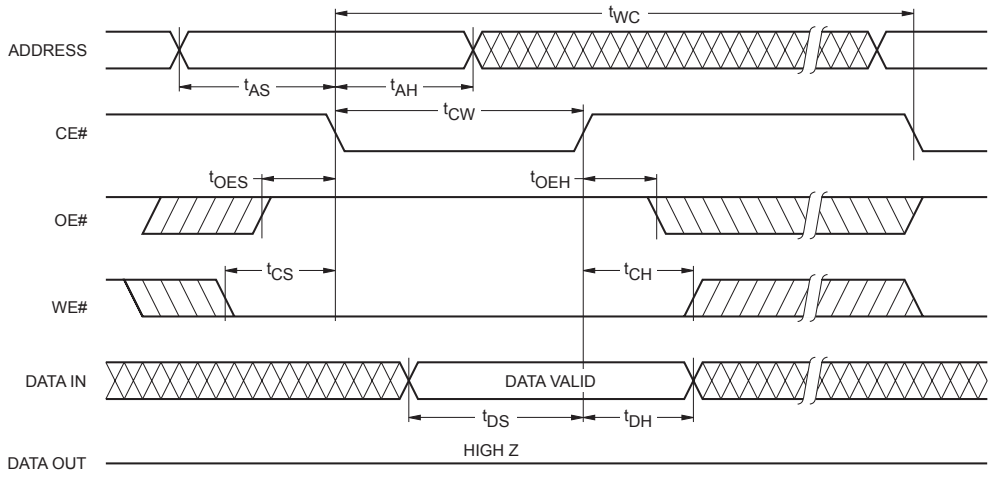
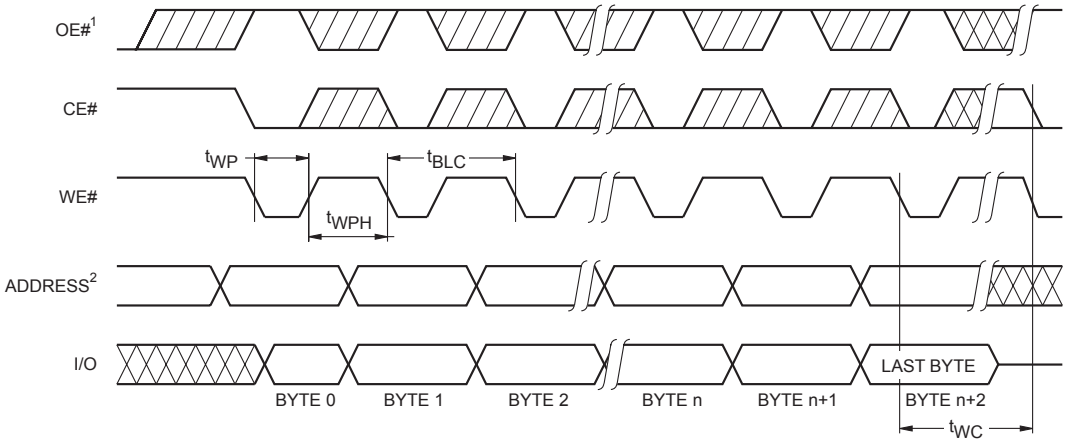


Figure 17 - Page Write Cycle



*For each successive write within the page write operation, A_7–A_{14} should be the same or writes to an unknown address could occur.

1. Between successive byte writes within a page write operation, OE# can be strobed LOW: e.g. this can be done with CE# and WE# HIGH to fetch data from another memory device within the system for the next write; or with WE# HIGH and CE# LOW effectively performing a polling operation.
2. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE# or WE# controlled write cycle timing.

Figure 18 - DATA Polling Diagram[1]

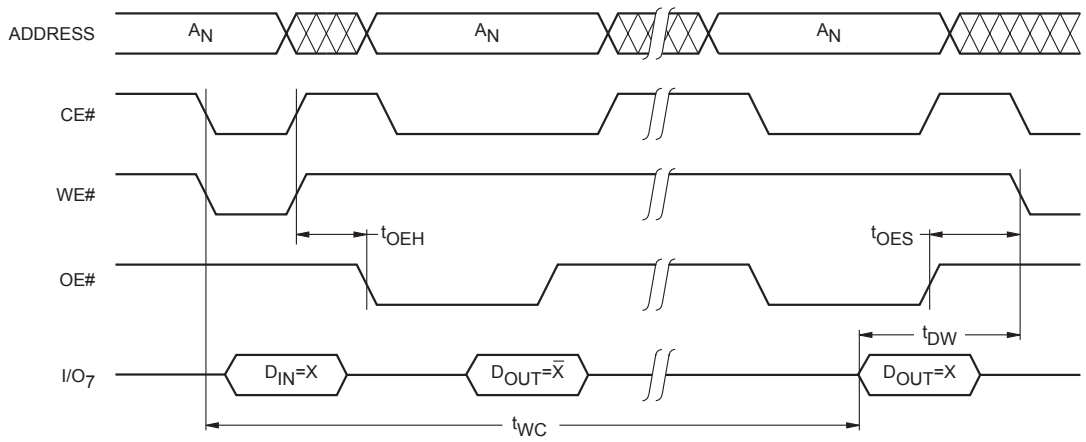
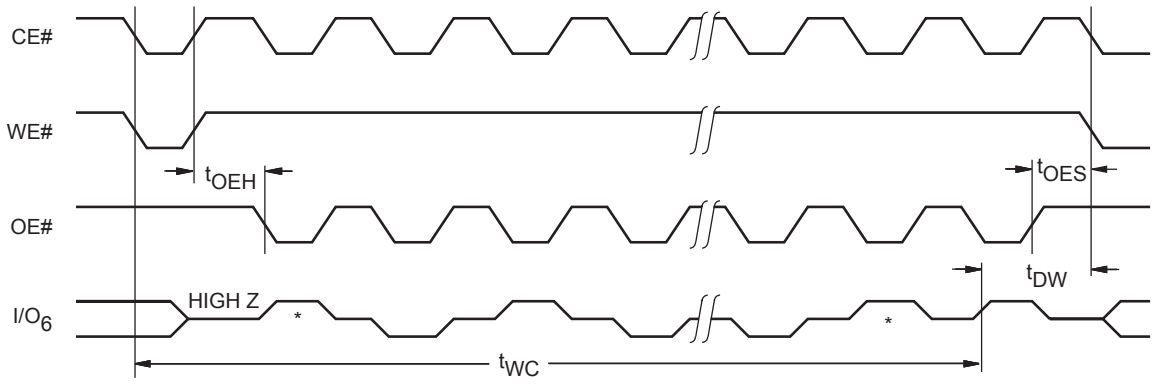


Figure 19 - Toggle Bit Timing Diagram[1]

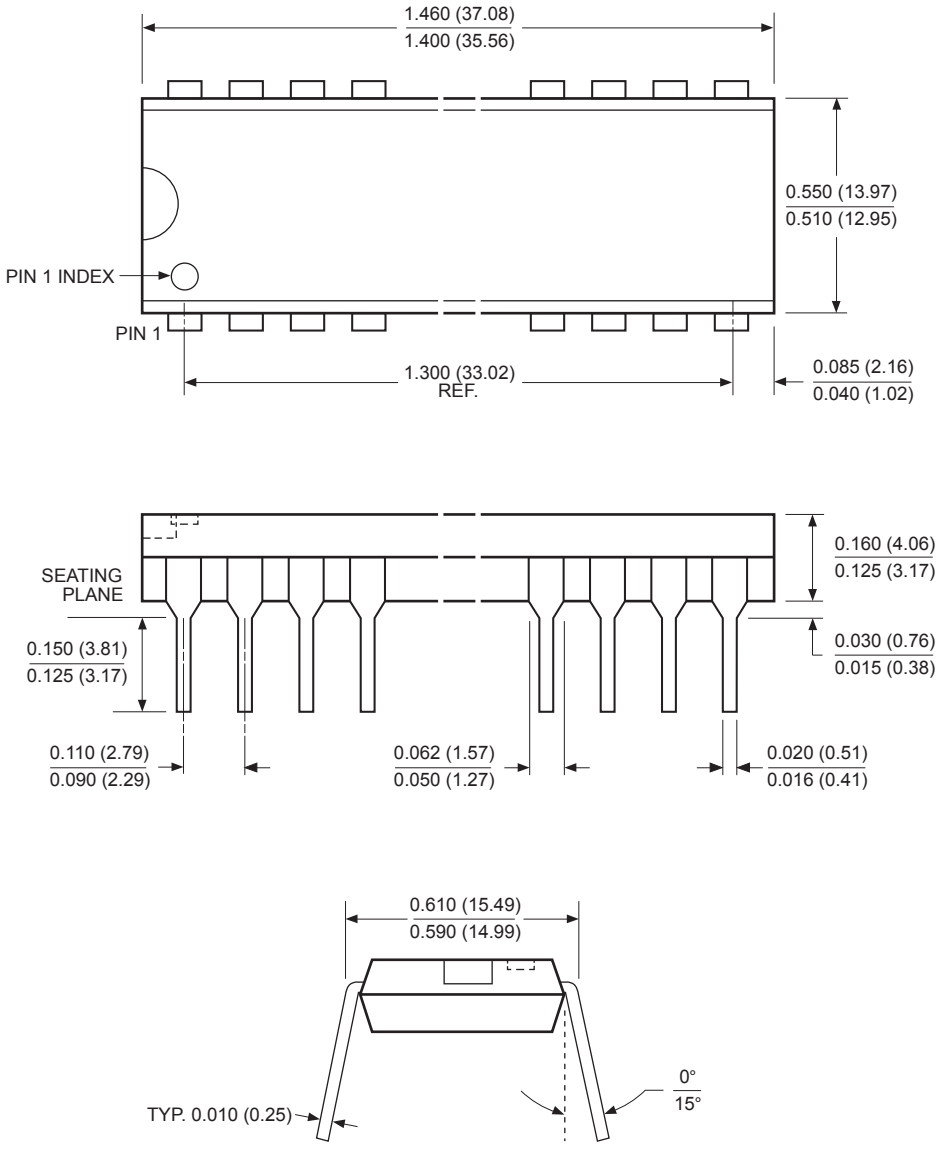


*I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

1. Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Packaging Information

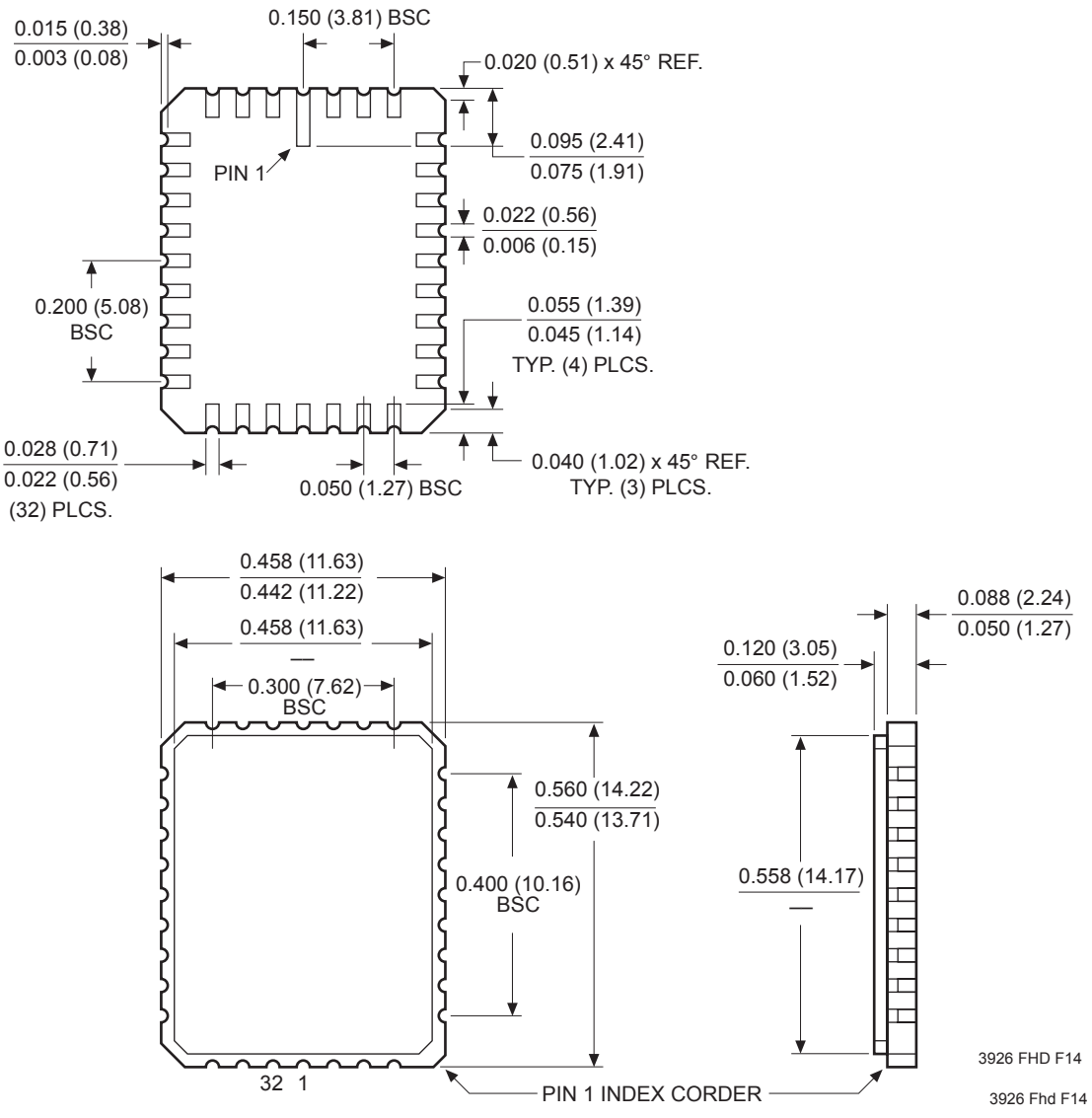
Figure 20 - 28-Lead Hermetic Dual In-line Package Type CW



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information (continued)

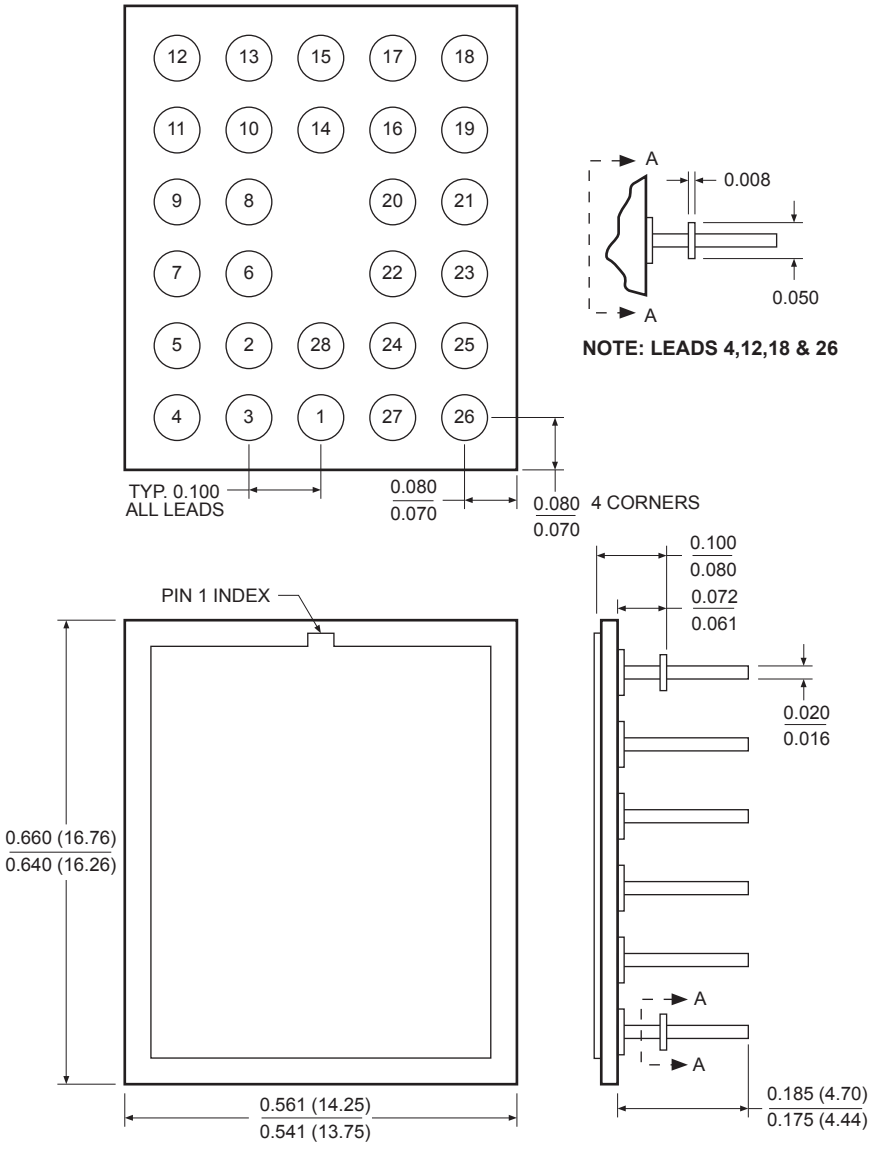
Figure 21 - 32-Pad Ceramic Leadless Chip Carrier Package Type ECA



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NTL ±0.005 (0.127)**

Packaging Information (continued)

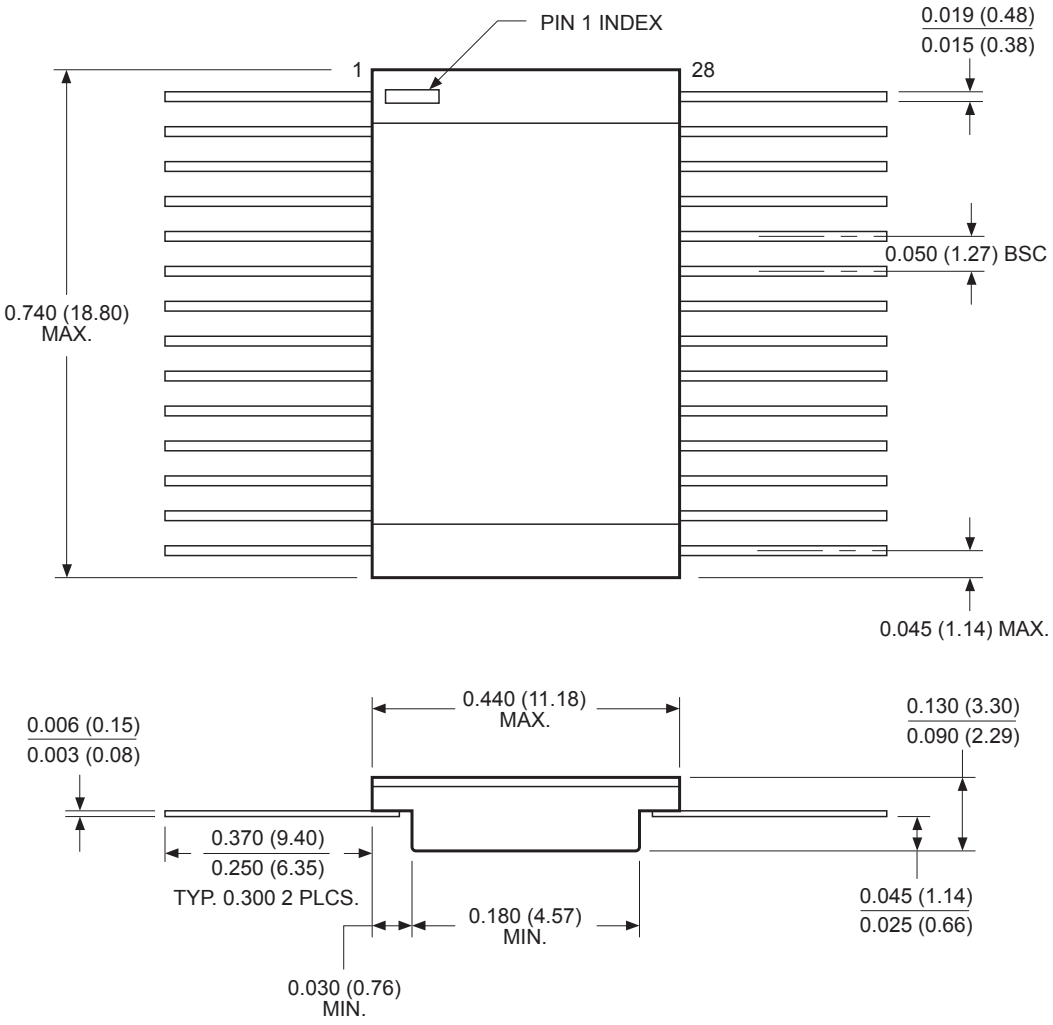
Figure 22 - 28-Lead Ceramic Pin Grid Array Package Type P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information (continued)

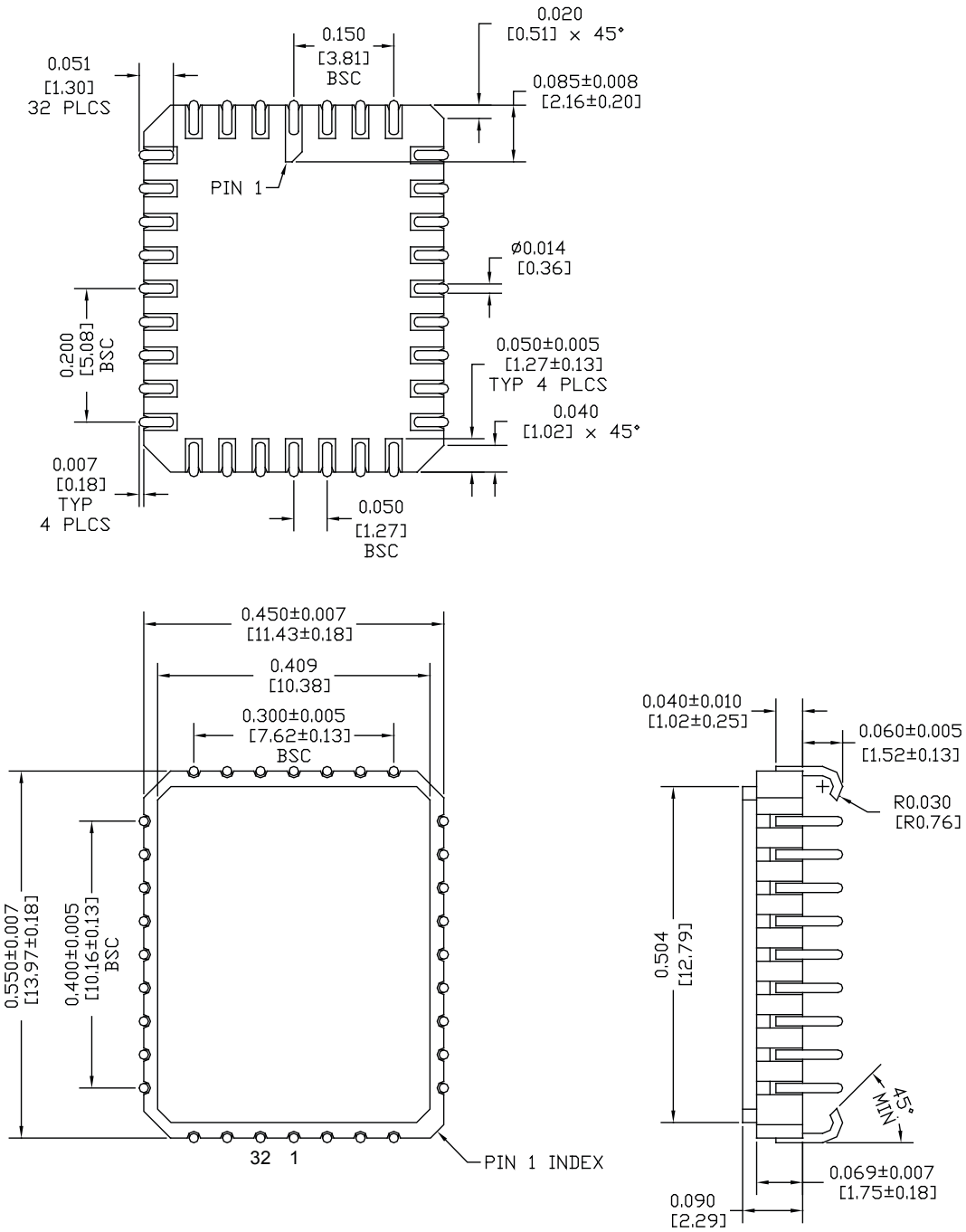
Figure 23 - 28-Lead Ceramic Flat Pack Type F



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information (continued)

Figure 24 - 32-Lead Ceramic SOJ Type ECJ



Ordering Information

Table 12 - Device Numbering

Device Number	Package Type	Speed	Temperature
MYXX28HC256CW	CerDIP	-7 = 70ns	IT/XT
		-9 = 90ns	
		-12 = 120ns	
		-15 = 150ns	
MYXX28HC256ECA-	CerLCC	-7 = 70ns	IT/XT
		-9 = 90ns	
		-12 = 120ns	
		-15 = 150ns	
MYXX28HC256F-	CerFP	-7 = 70ns	IT/XT
		-9 = 90ns	
		-12 = 120ns	
		-15 = 150ns	
MYXX28HC256P-	CerPGA	-7 = 70ns	IT/XT
		-9 = 90ns	
		-12 = 120ns	
		-15 = 150ns	
MYXX28HC256ECJ	CerSOJ	-7 = 70ns	IT/XT
		-9 = 90ns	
		-12 = 120ns	
		-15 = 150ns	

IT = Industrial Temperature Range -40°C to +85°C

XT = Extended Temperature Range -55°C to +125°C

Document Title

32K x 8 EEPROM - 5 Volt, Byte Alterable

Revision History

Revision #	History	Release Date	Status
1.3	Initial Release	November 2012	Preliminary
1.4	Added ceramic SOJ package drawing and option Changed status to "Released" Corrected part number Corrected figure designations	February 2013	Released