To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA2703GR

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2703GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

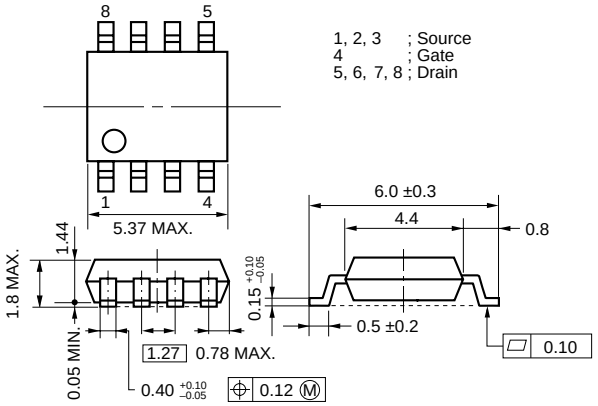
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 4.2 mΩ MAX. (V_{GS} = 10 V, I_D = 9.0 A)
  $R_{DS(on)2}$ = 6.4 mΩ MAX. (V_{GS} = 4.5 V, I_D = 9.0 A)
- Low C_{iss}: C_{iss} = 2600 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2703GR	Power SOP8

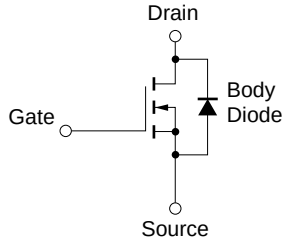
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±17	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±68	A
Total Power Dissipation (T_A = 25°C) Note2	P_T	2.2	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	17	A
Single Avalanche Energy Note3	E_{AS}	28.9	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 → 0 V

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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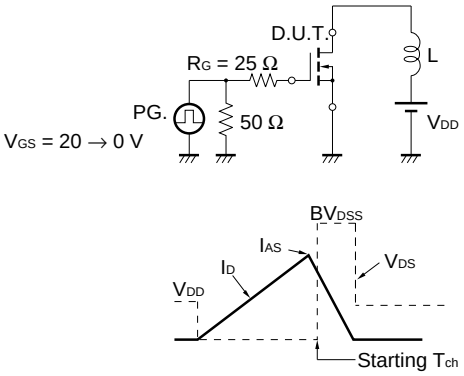
Printed in Japan

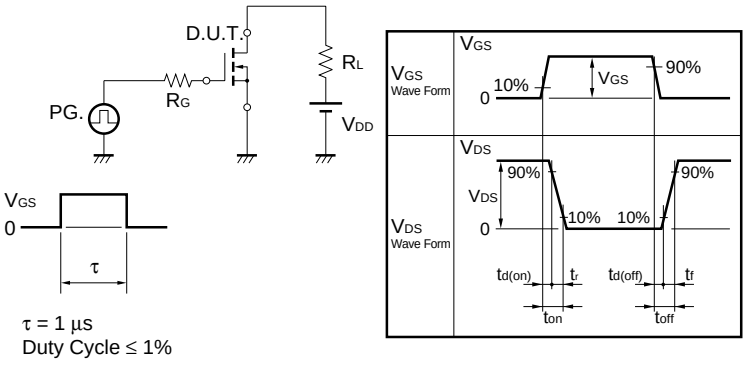
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 9.0 A	11	21.5		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 9.0 A		3.3	4.2	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 9.0 A		4.5	6.4	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 9.0 A		5.7	7.6	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		2600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1000		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		340		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 9.0 A		20		ns
Rise Time	t_r	V_{GS} = 10 V		24		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		75		ns
Fall Time	t_f			22		ns
Total Gate Charge	Q_G	V_{DD} = 15 V		26		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V		7		nC
Gate to Drain Charge	Q_{GD}	I_D = 17 A		11		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 17 A, V_{GS} = 0 V		0.8	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 17 A, V_{GS} = 0 V		50		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		51		nC

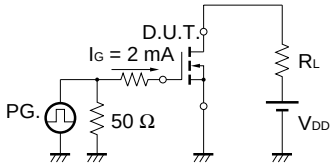
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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