



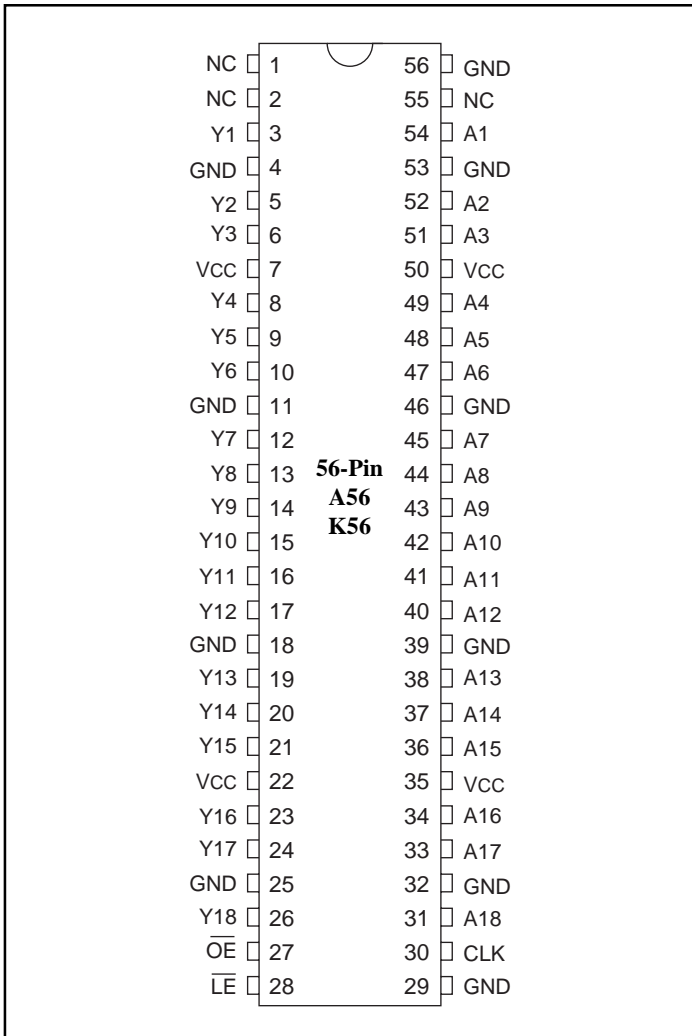
# PI74AVC16834

## 18-Bit Universal Bus Driver with 3-State Outputs

### Product Features

- Very high-speed, low-noise universal bus driver with embedded resistor outputs
- Meets PC133 SDRAM Registered DIMM specification
- Implements output impedance control for low-noise and heavy-load applications
- Fast Propagation Delay:  
2.5ns max. for 50pF test load
- $V_{CC} = 3.3V$  or  $2.5V$  or  $1.8V$
- Packages available:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 173 mil wide plastic TVSOP (K)

### Product Pin Configuration



### Product Description

Pericom Semiconductor's PI74AVC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

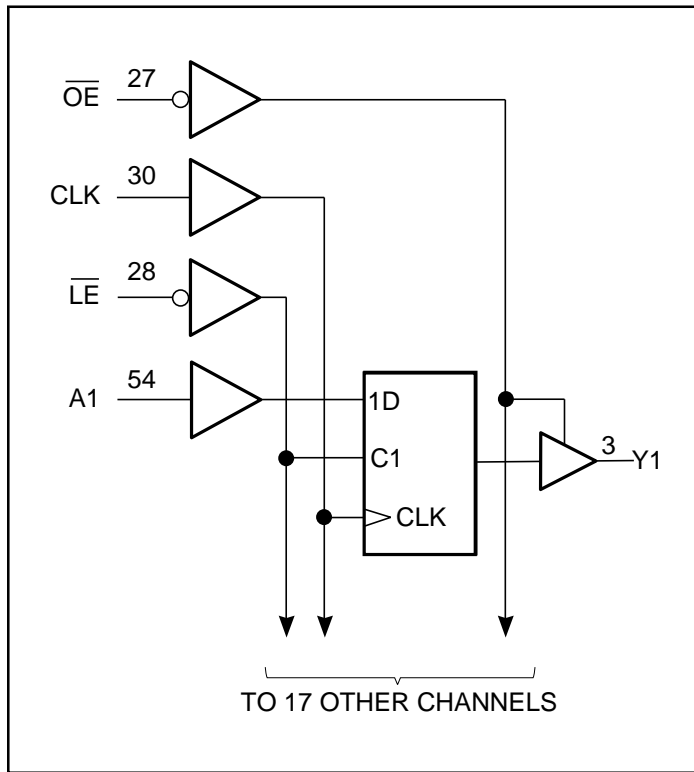
The 18-bit PI74AVC16834 universal bus driver is designed for 1.8V to 3.6V  $V_{CC}$  operation.

Data flow from A to Y is controlled by Output Enable ( $\overline{OE}$ ). The device operates in the transparent mode when  $\overline{LE}$  is LOW. The A data is latched if CLK is held at a high or low logic level. If  $\overline{LE}$  is HIGH, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state.

The PI74AVC16834 bus driver is designed to drive an array of 133 MHz synchronous memory chips, with minimal undershoot/overshoot noise, and to meet the input signal rise/fall time requirement of memory chips.

The output drivers of this part have an embedded series-resistor. For DIMM module design, no external series termination resistors near the buffer drivers or any other termination resistors are required. This feature simplifies DIMM module layout design, and results in cost savings.

### Logic Block Diagram



### Truth Table<sup>(1)</sup>

Inputs				Outputs Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Yo <sup>(2)</sup>
L	H	L	X	Yo <sup>(3)</sup>

**Note:**

- 1 H = High Signal Level  
 L = Low Signal Level  
 Z = High Impedance  
 ↑ = Transition LOW-to-HIGH  
 X = Irrelevant
2. Output level before the indicated steady-state input conditions were established, provided that CLK is HIGH before  $\overline{LE}$  goes HIGH.
3. Output level before the indicated steady-state input conditions were established.

### Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{LE}$	Latch Enable (Active LOW)
CLK	Clock Input
A	Data Input
Y	Data Output
GND	Ground
V <sub>CC</sub>	Power



**Recommended Operating Conditions<sup>(1)</sup>**

Parameters	Description	Test Conditions	Min.	Max.	Units
V <sub>CC</sub>	Supply Voltage	Operating	1.65	3.6	V
		Data Retention Only	1.2		
V <sub>IH</sub>	High-level Input Voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65V to 1.95V	0.65 x V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3V to 2.7V	1.7		
		V <sub>CC</sub> = 3V to 3.6V	2		
V <sub>IL</sub>	Low-level Input Voltage	V <sub>CC</sub> = 1.2V		GND	
		V <sub>CC</sub> = 1.65V to 1.95V		0.35 x V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3V to 2.7V		0.7	
		V <sub>CC</sub> = 3V to 3.6V		0.8	
V <sub>IN</sub>	Input Voltage		0	3.6	
V <sub>OUT</sub>	Output Voltage	Active State	0	V <sub>CC</sub>	
		3-State	0	3.6	
I <sub>OHS</sub>	High-level Output Current <sup>(2)</sup>	V <sub>CC</sub> = 1.65V to 1.95V		-4	
		V <sub>CC</sub> = 2.3V to 2.7V		-8	
		V <sub>CC</sub> = 3V to 3.6V		-12	
I <sub>OLS</sub>	Low-level Output Current <sup>(2)</sup>	V <sub>CC</sub> = 1.65V to 1.95V		4	
		V <sub>CC</sub> = 2.3V to 2.7V		8	
		V <sub>CC</sub> = 3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.65V to 3.6V		5	ns/V
T <sub>A</sub>	Operating Free-Air Temperature		-40	85	°C

**Note:**

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Dynamic drive is greater than standard output drive of I<sub>OH</sub> = -24mA and I<sub>OL</sub> = 24mA

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Parameters		Test Conditions		$V_{CC}^{(1)}$	Min.	Typ. <sup>(2)</sup>	Max.	Units
$V_{OH}$		$I_{OHS} = -100\mu\text{A}$	$V_{IH}$ or $V_{IL}$	1.65 to 3.6	$V_{CC} - 0.2$			V
		$I_{OHS} = -4\text{mA}$	$V_{IH} = 1.07\text{V}$	1.65	1.2			
		$I_{OHS} = -8\text{mA}$	$V_{IH} = 1.7\text{V}$	2.3	1.75			
		$I_{OHS} = -12\text{mA}$	$V_{IH} = 2\text{V}$	3.0	2.3			
$V_{OL}$		$I_{OLS} = 100\mu\text{A}$	$V_{IH}$ or $V_{IL}$	1.65 to 3.6			0.2	V
		$I_{OLS} = 4\text{mA}$	$V_{IL} = 0.57\text{V}$	1.65			0.45	
		$I_{OLS} = 8\text{mA}$	$V_{IL} = 0.7\text{V}$	2.3			0.55	
		$I_{OLS} = 12\text{mA}$	$V_{IL} = 0.8\text{V}$	3.0			0.7	
$I_I$	Control Inputs	$V_I = V_{CC}$ or GND		3.6			2.5	$\mu\text{A}$
$I_{OFF}$		$V_I = 0$ or $3.6\text{V}$		0			$\pm 10$	
$I_{OZ}^{(3)}$		$V_O = V_{CC}$ or GND	$\overline{OE} = V_{CC}$	3.6			$\pm 10$	
$I_{CC}$		$V_I = V_{CC}$ or GND	$I_O = 0$	3.6			40	
$C_I$	Control Inputs	$V_I = V_{CC}$ or GND		2.5		4.5		pF
				3.3		4.5		
	Data Input			2.5		4.0		
				3.3		4.0		
$C_O$	Outputs	$V_O = V_{CC}$ or GND		2.5		6.5		
				3.3		6.5		

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are measured at  $+25^\circ\text{C}$ .
- For I/O ports, the  $I_{OZ}$  includes the input leakage current.

**Timing Requirements over Operating Range**

Parameters	Description	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$f_{\text{CLOCK}}$	Clock Frequency		150		150		150	MHz
$t_W$ Pulse Duration	$\overline{LE}$ Low	2.0		1.2		1.0		ns
	CLK High or Low	2.0		1.2		1.0		
$t_{SU}$ Setup time	Data before CLK $\uparrow$	1.4		1.2		1.0		
	Data before $\overline{LE}\uparrow$ , CLK High or Low	1.4		1.2		1.0		
$t_H$ Hold time	Data after CLK $\uparrow$	1.0		0.8		0.6		
	Data after $\overline{LE}\uparrow$ , CLK High or Low	1.0		0.8		0.6		

**Switching Characteristics Over Recommended Operating Free-Air Temperature Range**

Unless otherwise noted, see Figures 1 through 3.

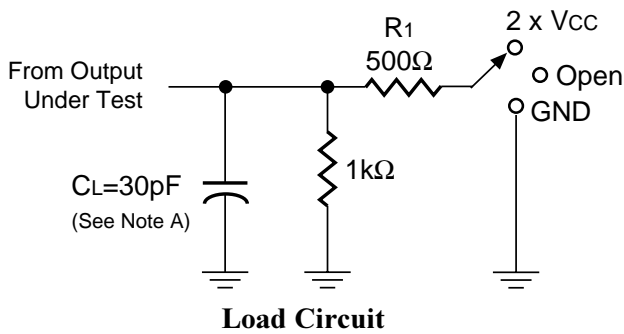
Parameter	From (Input)	To (Output)	$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V^{(1)} \pm 0.3V$		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$f_{max}$			150		150		150		MHz
$t_{pd}$	A	Y	1.0	4.5	0.8	3.0	0.7	2.4	ns
	$\overline{LE}$		1.0	5.0	0.8	3.3	0.7	2.5	
	CLK		1.0	4.5	0.8	3.0	0.7	2.5	
$t_{en}$	$\overline{OE}$		1.5	5.5	1.0	4.5	1.0	4.0	
$t_{DIS}$	$\overline{OE}$		1.5	5.0	1.0	4.5	1.0	4.0	

**Note 1.** Load at 50pF and 500Ω.

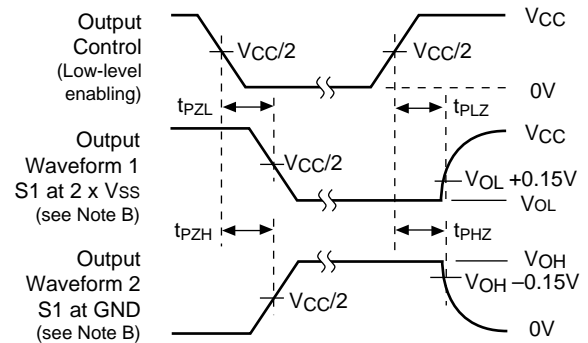
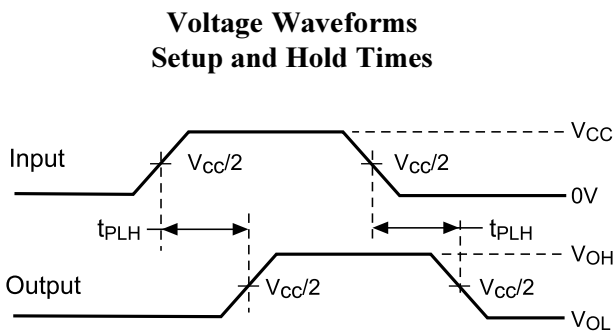
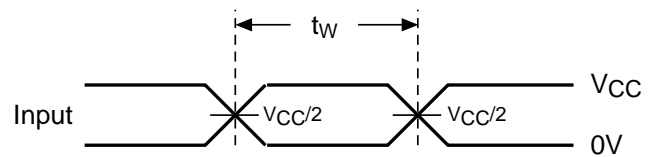
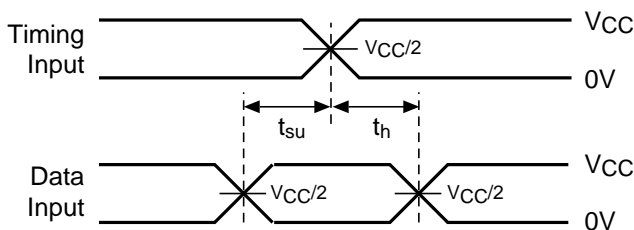
**Operating Characteristics,  $T_A = 25^\circ C$**

Parameters		Test Conditions	$V_{CC} = 1.8V$	$V_{CC} = 2.5V$	$V_{CC} = 3.3V$	Units
			Typ.	Typ.	Typ.	
$C_{pd}$ Power dissipation capacitance	Outputs Enabled	$C_L = 0,$ $f = 10 \text{ MHz}$	45	48	52	pF
	Outputs Disabled		23	25	28	

Parameter Measurement Information ( $V_{CC} = 1.8V \pm 0.15V$ )



TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open 2 x $V_{CC}$ GND

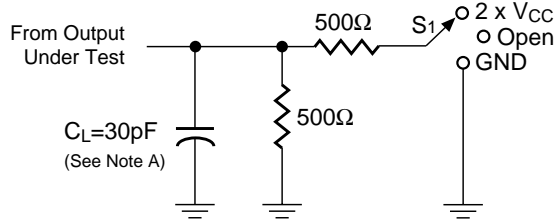


Notes:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50\Omega$ ,  $t_r \leq 2ns$ ,  $t_f \leq 2ns$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{dis}$ .

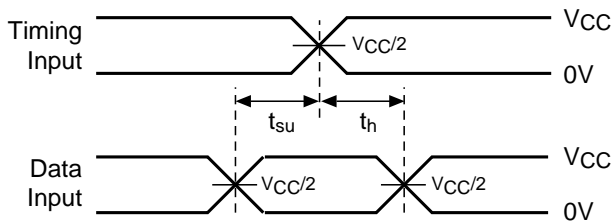
Figure 1. Load Circuit and Voltage Waveforms

Parameter Measurement Information ( $V_{CC} = 2.5V \pm 0.2V$ )

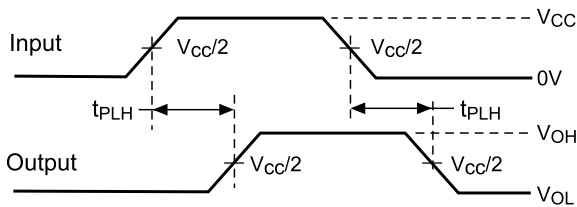


Load Circuit

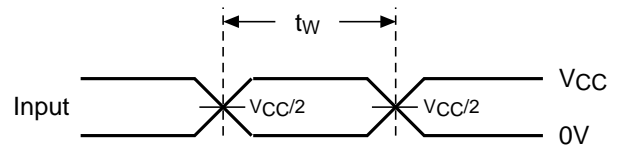
TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $2 \times V_{CC}$ GND



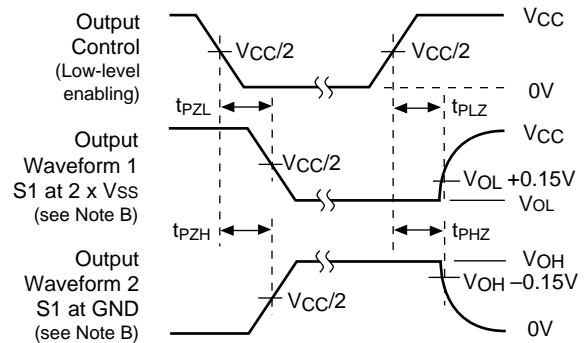
Voltage Waveforms  
Setup and Hold Times



Voltage Waveforms  
Propagation Delay Times



Voltage Waveforms  
Pulse Duration



Voltage Waveforms  
Enable and Disable Times

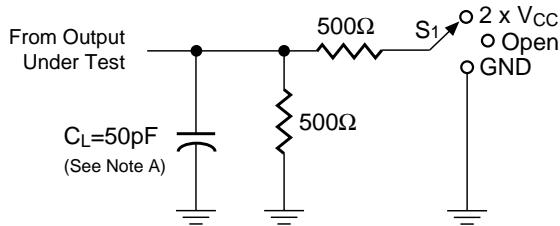
Notes:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 2\text{ns}$ ,  $t_f \leq 2\text{ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{dis}$ .

Figure 2. Load Circuit and Voltage Waveforms

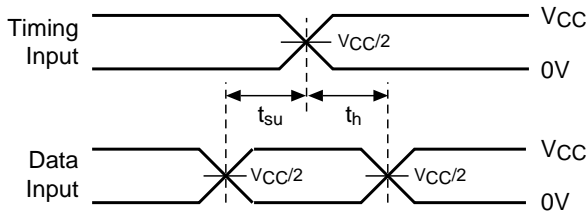


Parameter Measurement Information ( $V_{CC} = 3.3V \pm 0.3V$ )

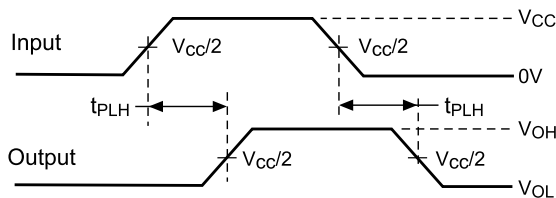


Load Circuit

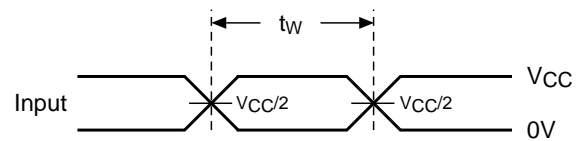
TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PHL}$	Open $2 \times V_{CC}$ GND



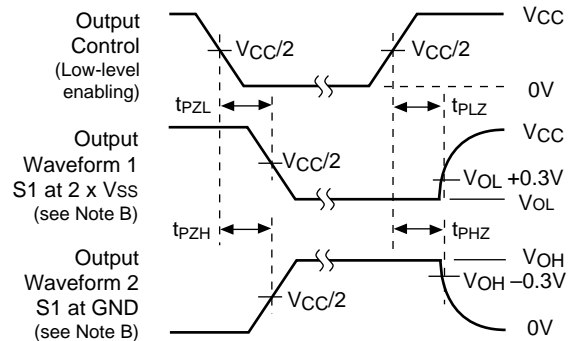
Voltage Waveforms  
Setup and Hold Times



Voltage Waveforms  
Propagation Delay Times



Voltage Waveforms  
Pulse Duration



Voltage Waveforms  
Enable and Disable Times

Notes:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50\Omega$ ,  $t_r \leq 2$ ns,  $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{dis}$ .

Figure 3. Load Circuit and Voltage Waveforms