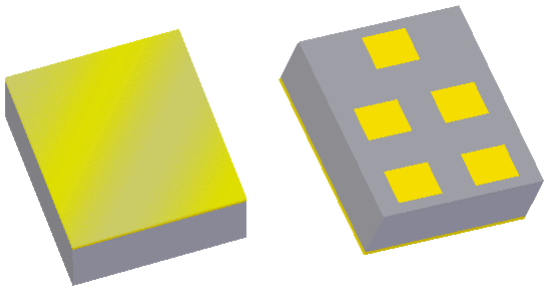
SAWTEK a TriQuint company

Preliminary Data Sheet

Part Number 856562
2140 MHz SAW Filter

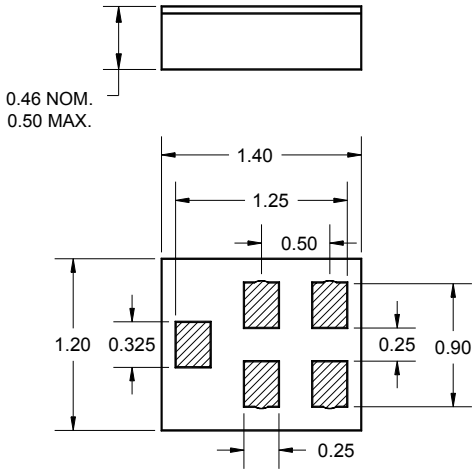
Features

- For WCDMA applications
- Usable bandwidth of 60 MHz
- Low loss
- Single-ended input, 50 Ω
- Balanced output, 100 Ω
- Ceramic Chip Scale Package (CSP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free



Package

Surface Mount 1.40 x 1.20 x 0.46 mm

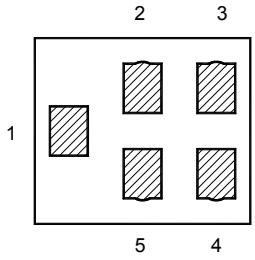


Dimensions shown are nominal in millimeters
All tolerances are ±0.10mm

Body: Al_2O_3 ceramic
Lid: *Kovar* or *Alloy 42*, *Au* over *Ni* plated
Terminations: *Au* plating 0.5 - 1.0μm,
over a 2 - 6μm *Ni* plating

Pin Configuration

Bottom View



Pin No.	Description
1	Input
3,4	Output
2,5	Case ground

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Electrical Specifications [1]

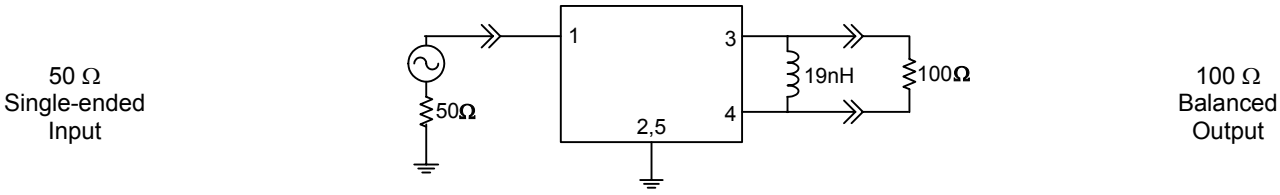
Operating Temperature Range: [2] -30 to +85 °C

Parameter [3]	Minimum	Typical	Maximum	Unit
Center Frequency	-	2140	-	MHz
Maximum Insertion Loss				
2110 - 2170 MHz	-	2	2.5	dB
Absolute Attenuation				
10 - 1920 MHz	30	35	-	dB
1920 - 1980 MHz	35	48	-	dB
1980 - 2050 MHz	25	35	-	dB
2230 - 2300 MHz	10	18	-	dB
4220 - 4340 MHz	10	57	-	dB
Amplitude Ripple				
2110 - 2170 MHz	-	0.1	1.5	dB p-p
Output Amplitude Balance ($\|S_{31}/S_{21}\|$)				
2110 - 2170 MHz	-1.8	-0.67	1.8	dB
Output Phase Balance [$\Phi(S_{31})-\Phi S_{21}+180$]				
2110 - 2170 MHz	-13	-9.4	13	degree
Input/Output VSWR				
2110 - 2170 MHz	-	1.5:1	2.2:1	-
Source Impedance [4]	-	50	-	Ω
Load Impedance (Balanced) [4]	-	100 || 19nH	-	Ω

Notes:

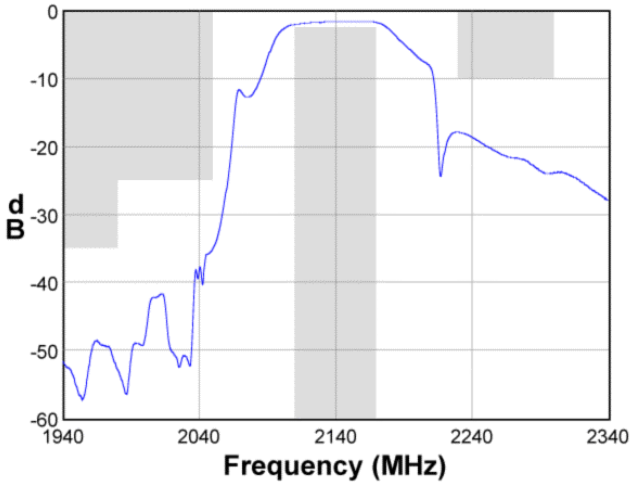
1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

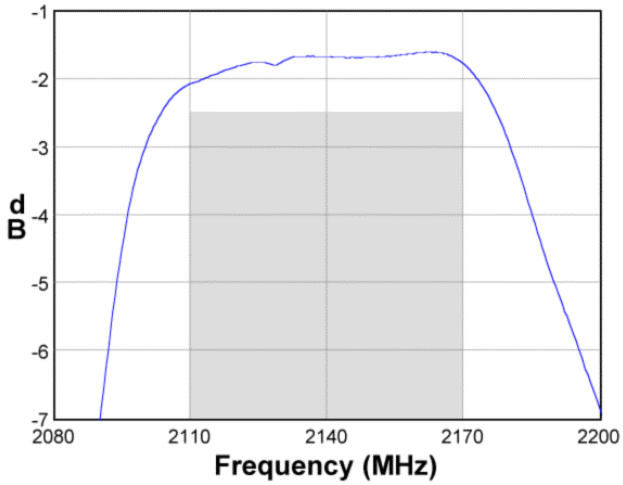


Typical Performance (at +25°C)

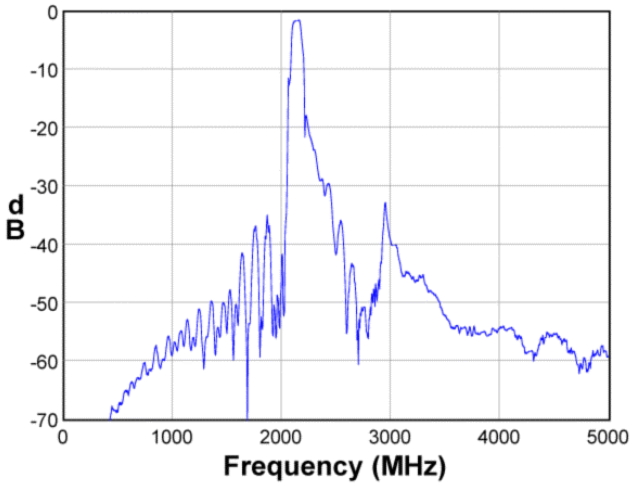
Frequency Response



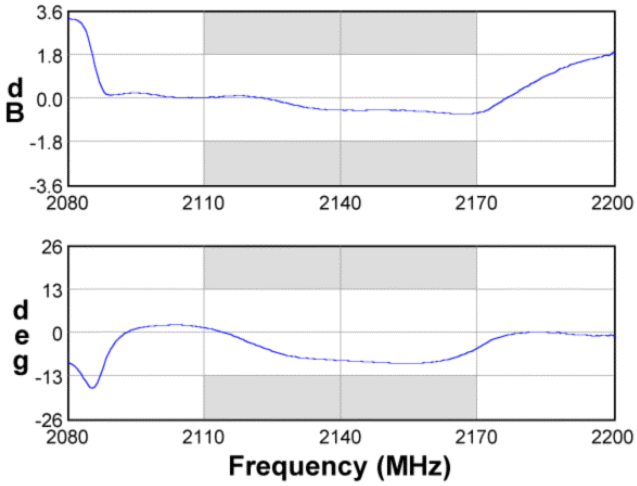
Passband Response



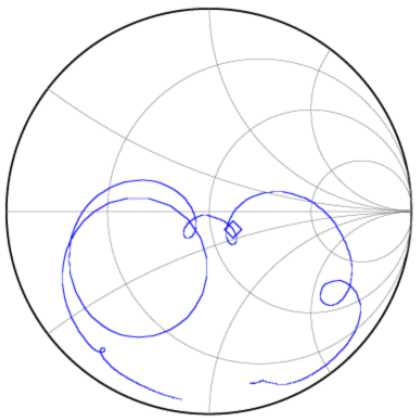
Wideband Response



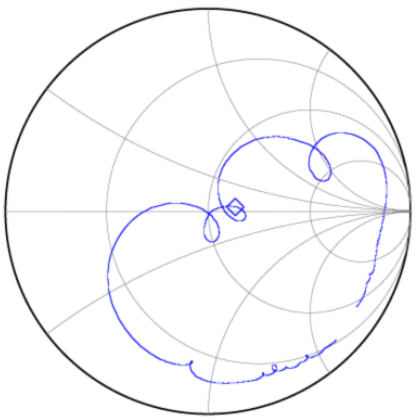
Amplitude/Phase Balance



Input Smith Chart



Output Smith Chart



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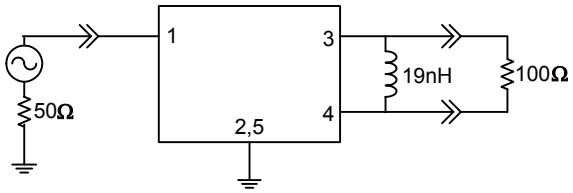
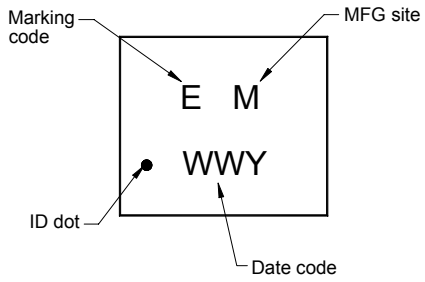
Matching Schematics

50 Ω
Single-ended
Input



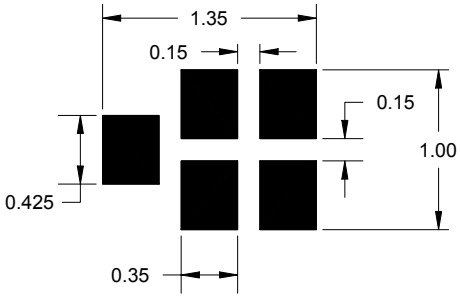
100 Ω
Balanced
Output

Marking



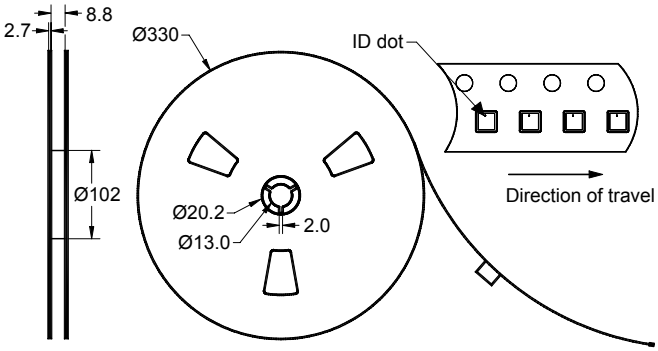
The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

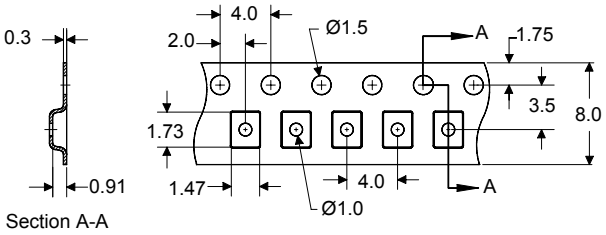
PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel





Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

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Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T_{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD)
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS)

Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260°C** peak reflow temperature (see soldering profile)

Links to Additional Technical Information

PCB Layout Tips | Qualification Flowchart | Soldering Profile

S-Parameters | RoHS information | Other Technical Information

Contact Information

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