## MN101E56/57/76 Series

## 8-bit Single-chip Microcontroller

## Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.
This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EF57 series has an internal 128 KB of ROM and 6 KB of RAM. Peripheral functions include 5 external interrupts, 29 internal interrupts including NMI, 12 timer counters, 4 types of serial interfaces, A/D converter, D/A converter, LCD driver, 2 types of watchdog timer, data automatic function and buzzer output. The system configuration is suitable for in camera, timer selector for VCR, CD player, or minicomponent.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz ), high-speed (crystal/ceramic frequency: max. 10 MHz ) / low-speed (internal frequency: 30 kHz ), low-speed (crystal/ceramic frequency: 32.768 kHz ) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz . A machine cycle in the PLL mode is 50 ns (maximum).

## Product Summary

This datasheet describes the following model.

| Model | ROM Size | RAM Size | Classification | Package |
| :---: | :---: | :---: | :---: | :---: |
| MN101EF76K | 256 KB | 10 KB |  | LQFP128-P-1818C |
| MN101EF57G | 128 KB | Flash EEPROM version |  |  |
| MN101EF56K | 256 KB |  |  | QFP100-P-1818B |

Note) DMOD internal pull-up resistor is in only Flash EEPROM version.
When using In-circuit Emulator, it is necessary to connect the pull-up resistor on the circuit board.
$\square$

Features (continued)

- Interrupts

| Interrupts | MN101EF76K 36 sets | MN101EF57G 34 sets | MN101EF56K 36 sets |
| :---: | :---: | :---: | :---: |
| Overrun interrupt |  |  |  |
| Non-maskable interrupt (NMI) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer interrupt |  |  |  |
| Timer 0 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 1 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 2 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 3 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 4 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 6 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 7 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Time-base interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 7 compare register 2 match interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 8 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 8 compare register 2 match interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| PWM overflow interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| PWM under flow interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Timer 9 compare register 2 match interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 24H timer interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Alarm match interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial interrupt |  |  |  |
| LIN interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 0 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 0 UART reception interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 1 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 1 UART reception interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 2 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 2 UART reception interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 3 interrupt | $\bigcirc$ |  | $\bigcirc$ |
| Serial 3 UART reception interrupt | $\bigcirc$ |  | $\bigcirc$ |
| Serial 4 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Serial 4 stop condition interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| A/D interrupt |  |  |  |
| A/D conversion interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Data automatic transfer interrupt |  |  |  |
| ATC1 interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| Low voltage detection interrupt |  |  |  |
| Low voltage detection interrupt | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| External interrupt |  |  |  |
| IRQ0 (Edge selection, noise filter connectable) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| IRQ1 (Edge selection, noise filter connectable) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| IRQ2 (Edge selection, both edge interrupt, noise filter connectable) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| IRQ3 (Edge selection, both edge interrupt, noise filter connectable) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| IRQ4 (Edge selection, both edge interrupt, noise filter connectable, <br> KEY scan interrupt) | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |

## Features (continued)

- Timer Counter: 12 sets

General-purpose 8 -bit timer u 5 sets
General-purpose 16 -bit timer $u 2$ sets
General-purpose 16 -bit timer $u 2$ sets
Motor control 16-bit timer u 1 set
8 -bit free-run timer u 1 set
Time-base timer u 1 set
Baud rate timer u 1 set
24 H timer u 1 set

## Timer 0 (General-purpose 8-bit timer)

Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TMOIOB, event count, simple pulse width measurement
Double-buffered compare register (u1)* Function in MN101EF76K and MN101EF56K
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

## Timer 1 (General-purpose 8-bit timer)

Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 0)
Double-buffered compare register (u1)* Function in MN101EF76K and MN101EF56K
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement,
24 -bit cascade connection (connected with timer 0,1 ), timer synchronous output
Double-buffered compare register (u1)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs $/ 4$, fs $/ 8$, fslow, external clock, timer A output Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 3 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 2), 32-bit cascade connection (connected with timer 0, 1, 2)
Double-buffered compare register (u1)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/ 128 , fs/2, fs/4, fs $/ 8$, fslow, external clock, timer A output

Timer 4 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2bit) type PWM output, event count, simple pulse width measurement Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs $/ 2$, fs $/ 4$, fs $/ 8$, fslow, external clock, timer A output

## Features (continued)

## - Timer Counter (continued)

Timer 6 (8-bit free-run timer, time-base timer)
8 -bit free-run timer
Clock source:
fpll-div, fpll-div $/ 2^{2}$, fpll-div $/ 2^{3}$, fpll-div $/ 2^{12}$, fpll-div $/ 2^{13}$, fs, fslow, fslow $/ 2^{2}$, fslow $/ 2^{3}$, fslow $/ 2^{12}$, fslow $/ 2^{13}$
Time-base timer
Interrupt generation cycle:
fpll-div/ $/ 2^{7}$, fpll-div $/ 2^{8}$, fpll-div $/ 2^{9}$, fpll-div $/ 2^{10}$, fpll-div $/ 2^{13}$, fpll-div $/ 2^{15}$, fslow $/ 2^{7}$, fslow $/ 2^{8}$, fslow $/ 2^{9}$, fslow $/ 2^{10}$, fslow $/ 2^{13}$, fslow/2 ${ }^{15}$

## Timer 7 (General-purpose 16-bit timer)

## Clock source:

fpll-div, fs, external clock, timer A output, serial 0 transfer clock output, timer 6 compare match cycle divided by 1,2, 4, 16
Hardware configuration:
Double-buffered compare register (u2)
Double-buffered input capture register (u2)
Timer interrupt (u2 vector)
Timer function:
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, timer synchronous output, event count, input capture function (both edges operable)
Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

## Timer 8 (General-purpose 16-bit timer)

Clock source:
fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16
Hardware configuration:
Double-buffered compare register (u2)
Double-buffered input capture register (u1)
Timer interrupt (u2 vector)
Timer function:
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture function (both edges operable)
32-bit cascade connection (connected with timer 7), 32-bit PWM output, input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)
Clock source:
fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
Hardware configuration:
Double-buffered compare register (u2)
Timer interrupt (u3 vector)
Timer function:
Square wave output (Timer pulse output) can be changed to large current output, complementary
3-phase PWM output, triangle wave and saw tooth wave are supported, dead time insertion available, event count
Pin output control:
PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4 ) ("Hi-z", output data fixed)

Timer A (baud rate timer)
Clock output for peripheral functions
Clock source:
fpll-div divided by $1 / 1,2,4,8,16,32$, and fs divided by 2,4

## Features (continued)

## - Timer Counter (continued)

24H timer
Clock source (Usable frequency)
fpll ( $4 \mathrm{MHz}, 4.19 \mathrm{MHz}, 5 \mathrm{MHz}, 8 \mathrm{MHz}, 8.38 \mathrm{MHz}, 10 \mathrm{MHz}, 16 \mathrm{MHz}, 16.77 \mathrm{MHz}, 20 \mathrm{MHz}$ ), fx ( 32.768 kHz ), frc ( $20 \mathrm{MHz}, 16 \mathrm{MHz}$ ), frcs ( 30 kHz )
Hardware configuration:
0.5 seconds counter, minute counter, hour counter

Alarm compare register (in 0.5 seconds, in minutes, in hours) (u1)
Timer interrupt (u2 vector)
Timer function:
Interval function (interrupts every 0.5 seconds, 1 second, 1 minute, 1 hour, 24 hours)
Alarm function

## - Watchdog timer

Overrun detection cycle is selectable from $\mathrm{fs} / 2^{16}, \mathrm{fs} / 2^{18}, \mathrm{fs} / 2^{20}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Watchdog timer2

Overrun detection cycle is selectable from frcs $/ 2^{4}$, frcs $/ 2^{5}, \operatorname{frcs} / 2^{6}, \operatorname{frcs} / 2^{7}, \operatorname{frcs} / 2^{8}, \operatorname{frcs} / 2^{9}, \operatorname{frcs} / 2^{10}, \operatorname{frcs} / 2^{11}, \operatorname{frcs} / 2^{12}, \operatorname{frcs} / 2^{13}, \operatorname{frcs} / 2^{14}$, frcs/ $2^{15}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Synchronous output function (Timer synchronous output, interrupt synchronous output)

Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)

- Buzzer Output

Output frequency can be selected from fpll-div/2 $2^{9}$, fpll-div/ $/ 2^{10}$, fpll-div/2 $2^{11}$, fpll-div $/ 2^{12}, \mathrm{fpll}-\operatorname{div} / 2^{13}, \mathrm{fpll}$-div $/ 2^{14}, \mathrm{fslow} / 2^{3}, \mathrm{fslow} / 2^{4}$

- A/D converter

MN101EF76K: 10-bit u 24 channels
MN101EF57G: 10-bit u 12 channels
MN101EF56K: 10-bit u 24 channels

- D/A converter

MN101EF76K: 8-bit u 4 channels
MN101EF57G: 8-bit u 2 channels
MN101EF56K: 8-bit u 4 channels

- Data automatic transfer: 1 system

Data is automatically transferred in all memory space
External interrupt activation/internal event activation/software activation
Max. 255 byte continuous transfer
Serial continuous transmission and reception is supported
Burst transfer function (Including interrupt emergency stop)

## Features (continued)

- Serial interface

MN101EF76K: 5 systems
MN101EF57G: 4 systems
MN101EF56K: 5 systems
Serial interface 0 (Hardware LIN / Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source:
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
Continuous transmission, continuous reception, continuous transmission and reception are available.
Full duplex UART (Baud rate timer: selected from timer 0 to 4 , or timer A)
Parity check, overrun error/framing error are detected
Transfer bits 7 to 8 are selectable
Hardware LIN
Synch Break generation, Wake-up detection, Synch Break detection, Synch Field measurement are available
Serial interface 1 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source:
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
Continuous transmission, continuous reception, continuous transmission and reception are available.
Full duplex UART (Baud rate timer: selected from timer 0 to 4 , or timer A)
Parity check, overrun error/framing error are detected
Transfer bits 7 to 8 are selectable
Serial interface 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source:
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4 , Timer A output divided by 1, 2, 4, 8, 16, External clock
MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
Continuous transmission, continuous reception, continuous transmission and reception are available.
Full duplex UART (Baud rate timer: selected from timer 0 to 4 , or timer A)
Parity check, overrun error/framing error are detected
Transfer bits 7 to 8 are selectable

Serial interface 3 (Full duplex UART / Synchronous serial interface) * Function in MN101EF76K and MN101EF56K
Synchronous serial interface
Transfer clock source:
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4 , Timer A output divided by 1, 2, 4, 8, 16, External clock MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
Continuous transmission, continuous reception, continuous transmission and reception are available.
Full duplex UART (Baud rate timer: selected from timer 0 to 4 , or timer A)
Parity check, overrun error/framing error are detected
Transfer bits 7 to 8 are selectable

## Features (continued)

- Serial interface (continued)

Serial interface 4 (Multi master IIC / Synchronous serial interface)
Synchronous serial interface
Transfer clock source:
fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4, Timer 0 to 4 , Timer A output divided by 1, 2, 4, 8, 16, External clock
MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
Continuous transmission, continuous reception, continuous transmission and reception are available.
Multi master IIC
7, 10-bit slave address is settable
General call communication mode is supported

- Auto reset circuit
- Low voltage detection circuit
- Clock Monitoring Function
- LED driver: 8 sets
- LCD driver

Segment output
MN101EF76K: Max. 55 pins (SEG0 to SEG54)
MN101EF57G: Max. 41 pins (SEG0 to SEG40)
MN101EF56K: Max. 55 pins (SEG0 to SEG54)
Segment output pins can be switched to I/O ports in 1 bit.

* At reset, Segment outputs are input ports.

Common output: 4 pins
COM0 to 3 can be switched to I/O ports in 1 bit.
Display mode selection
Static
1/2 duty, $1 / 2$ bias
$1 / 3$ duty, $1 / 3$ bias
1/4 duty, $1 / 3$ bias
LCD driver clock
When the source clock is the main clock (fpll)
$1 / 2^{18}, 1 / 2^{17}, 1 / 2^{16}, 1 / 2^{15}, 1 / 2^{14}, 1 / 2^{13}, 1 / 2^{12}, 1 / 2^{11}$
When the source clock is the sub clock (fslow)
$1 / 2^{9}, 1 / 2^{8}, 1 / 2^{7}, 1 / 2^{6}$
Timer 0 to 4, Timer A output
LCD power supply
LCD power supply is separated from $V_{D D 5}$. (can be used when $V_{L C 1} d V_{D D 5}$ )
External power supply voltage can be selectable. (Supply voltage is supplied from $\mathrm{V}_{\mathrm{LC} 1}, \mathrm{~V}_{\mathrm{LC} 2}$, and $\mathrm{V}_{\mathrm{LC} 3}$ )
Internal dividing resistors (External power supply voltage is divided the voltage input to $\mathrm{V}_{\mathrm{LC} 1}$ by internal resistors.)

Features (continued)

- Ports

| Ports | MN101EF76K <br> $(\mathrm{pins})$ | MN101EF57G <br> $(\mathrm{pins})$ | MN101EF56K <br> $(\mathrm{pins})$ |
| :--- | :---: | :---: | :---: |
| I/O ports | 104 | 70 | 90 |
| LCD segment | 55 | 41 | 55 |
| LCD common | 4 | 4 | 4 |
| Serial interface communication | 30 | 21 | 30 |
| Timer I/O | 34 | 21 | 28 |
| Buzzer output | 4 | 2 | 4 |
| A/D input | 24 | 16 | 24 |
| External interrupt | 10 | 5 | 5 |
| LCD power supply | 3 | 3 | 3 |
| LED driver (high-current) | 8 | 8 | 8 |
| High-speed oscillation | 2 | 2 | 2 |
| Low-speed oscillation | 2 | 2 | 2 |
| D/A output | 4 | 2 | 4 |
| Special function pins | 10 | 10 | 10 |
| Operation mode input | 3 | 3 | 3 |
| Reset input | 1 | 1 | 1 |
| Analog reference voltage input | 1 | 1 | 1 |
| Power supply | 4 | 4 | 4 |

## ■ Pin Description

- MN101EF76K (LQFP128-P-1818C)


■ Pin Description (continued)

- MN101EF57G (LQFP080-P-1414A, TQFP080-P-1212F)


■ Pin Description (continued)

- MN101EF56K (QFP100-P-1818B)



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