QUAD, ±16.5kV ESD Protected, 3.0V to 5.5V, RS-485/RS-422 Receivers

ISL32173E, ISL32175E, ISL32177E, ISL32273E, ISL32275E, ISL32277E

These Intersil devices are ±16.5kV IEC61000-4-2 ESD protected, 3.0V to 5.5V powered, QUAD receivers for balanced communication using the RS-485 and RS-422 standards. Each receiver has low input currents (±200µA), so it presents a 1/4 unit load to the RS-485 bus, and allows up to 128 receivers on the bus.

The ISL32173E, ISL32175E, ISL32177E are high data rate receivers that operate at data rates up to 80Mbps. Their 8ns maximum propagation delay skew (tolerance) guarantees excellent part-to-part matching. The ISL32273E, ISL32275E, ISL32277E are reduced supply current versions that operate at data rates up to 20Mbps.

Receiver outputs are tri-statable, and incorporate a hot plug feature to keep them disabled during power up and down. Versions are available with a common EN/$\overline{EN}$ (‘173 pinout), a two channel EN12/EN34 (‘175 pinout), or a versatile individual channel enable (see Table 1).

A 26% smaller footprint is available with the ISL32177E and ISL32277E QFN packages, and these two devices also feature a logic supply pin (V_L). The V_L supply sets the switching points of the enable inputs, and the receiver outputs’ V_{OH}, to levels compatible with a lower supply voltage in mixed voltage systems. Individual channel and group enable pins increase the ISL32177E and ISL32277E’s flexibility.

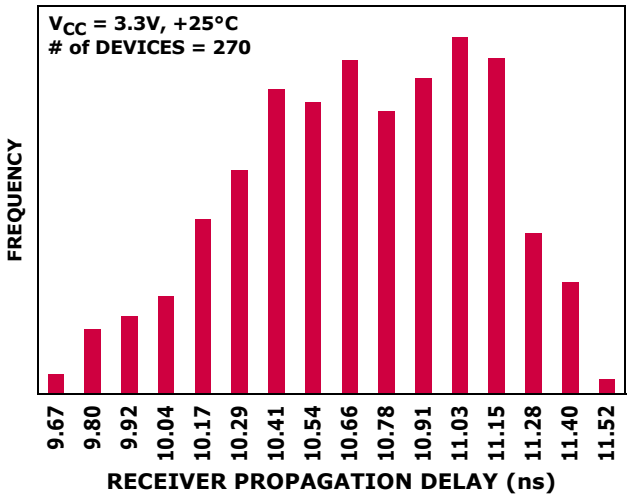
Features

- IEC61000 ESD Protection (RS-485 Inputs) ±16.5kV
  - Class 3 ESD on all Other Pins . . . . . >8kV HBM
- Wide Supply Range. . . . . 3.0V to 5.5V
- Wide Common Mode Range . . . . . -7V to +12V
- Low Part-to-Part Propagation Delay Tolerance. . . . . ±4ns (max)
- Specified for +125°C Operation
- Fail-Safe Open Rx Inputs
- 1/4 Unit Load Allows 128 Devices on the Bus
- Available in Industry Standard Pinouts (‘173/’175) and a 4x4 QFN (ISL32X77E) with Added Features
- Logic Supply Pin (V_L) Eases Operation in Mixed Supply Systems (ISL32X77E)
- High Data Rates . . . . . up to 80M or 20Mbps
- Low Shutdown Supply Current 60µA
- Tri-statable Rx Outputs
- 5V Tolerant Logic Inputs When V_{CC} = 3.3V

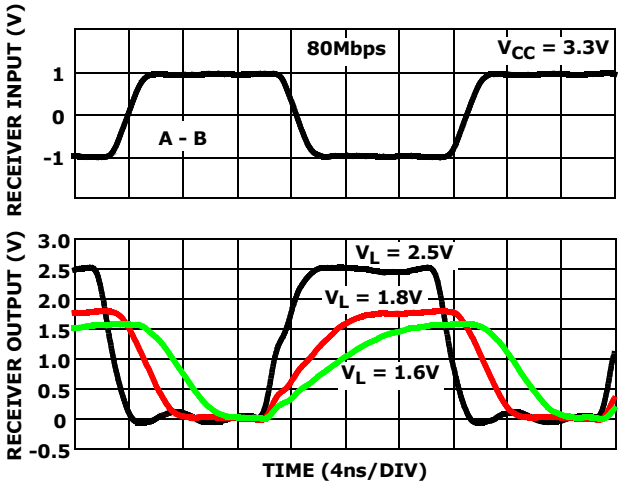
Applications

- Telecom Equipment
- Motor Controllers/Encoders
- Programmable Logic Controllers
- Industrial/Process Control Networks

ISL32177E Part-to-Part Prop Delay Variability



ISL3217XE Data Rate and V_L Performance



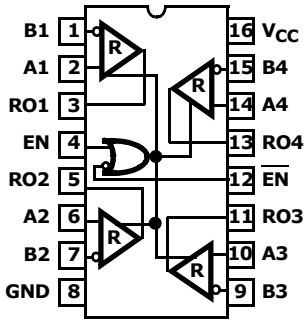
ISL32173E, ISL32175E, ISL32177E, ISL32273E, ISL32275E, ISL32277E

TABLE 1. SUMMARY OF FEATURES

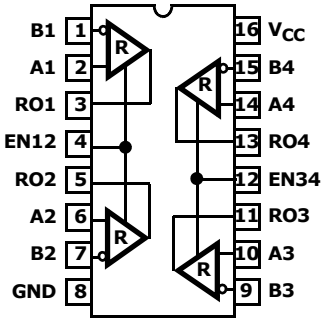
PART NUMBER	FUNCTION	DATA RATE (Mbps)	HOT PLUG?	V_L SUPPLY PIN?	Rx ENABLE TYPE	MAX. TOTAL SUPPLY CURRENT (mA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL32173E	4 Rx	80	YES	NO	EN, $\overline{EN}$	15	YES	16
ISL32175E	4 Rx	80	YES	NO	EN12, EN34	15	YES	16
ISL32177E	4 Rx	80	YES	YES	INDIVIDUAL AND GROUP ENABLES	15	YES	24
ISL32273E	4 Rx	20	YES	NO	EN, $\overline{EN}$	5.5	YES	16
ISL32275E	4 Rx	20	YES	NO	EN12, EN34	5.5	YES	16
ISL32277E	4 Rx	20	YES	YES	INDIVIDUAL AND GROUP ENABLES	5.5	YES	24

Pin Configurations

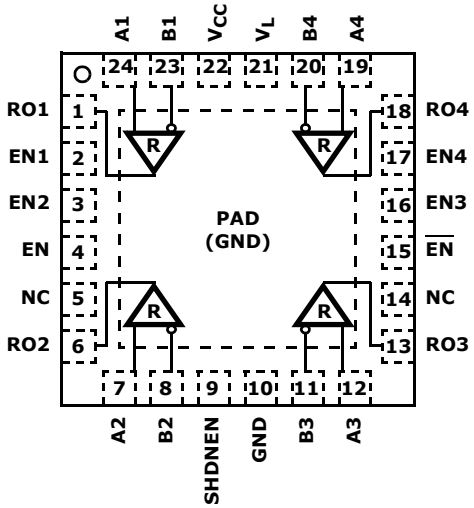
ISL32173E, ISL32273E
(16 LD N-SOIC, 16 LD TSSOP)
TOP VIEWS



ISL32175E, ISL32275E
(16 LD N-SOIC, 16 LD TSSOP)
TOP VIEWS



ISL32177E, ISL32277E
(24 LD QFN)
TOP VIEW



Pin Descriptions

ISL32173E, ISL32273E PIN NUMBER	ISL32175E, ISL32275E PIN NUMBER	ISL32177E, ISL32277E PIN NUMBER	PIN	FUNCTION
4, 12	-	4, 15	EN, $\overline{EN}$	Group driver output enables, that are internally pulled high to V_{CC}. All receiver outputs are enabled by driving EN high OR $\overline{EN}$ low, and the outputs are all high impedance when EN is low AND $\overline{EN}$ is high (i.e., if using only the active high EN, connect $\overline{EN}$ to V_{CC} or V_L through a 1kΩ resistor; if using only the active low $\overline{EN}$, connect EN directly to GND). If the group enable function isn't required, connect EN to V_{CC} (or V_L) through a 1kΩ or greater resistor, or connect $\overline{EN}$ directly to GND. (ISL32X73E and ISL32X77E only)
-	4, 12	-	EN12, EN34	Paired driver output enables, that are internally pulled high to V_{CC}. Driving EN12 (EN34) high enables the channel 1 and 2 (3 and 4) RO outputs. Driving EN12 (EN34) low disables the channel 1 and 2 (3 and 4) outputs. If the enable function isn't required, connect EN12 and EN34 to V_{CC} (or V_L) through a 1kΩ or greater resistor. (ISL32X75E only).
-	-	2, 3, 16, 17	EN1, EN2, EN3, EN4	Individual receiver output enables that are internally pulled high to V_{CC}. Forcing ENX high (along with EN high OR $\overline{EN}$ low) enables the channel X output (ROX). Driving ENX low disables the channel X output, regardless of the states of EN and $\overline{EN}$. If the individual channel enable function isn't required, connect ENX to V_{CC} (or V_L) through a 1kΩ or greater resistor. (ISL32X77E only)
-	-	9	SHDNEN	Low power SHDN mode enable that is internally pulled high to V_{CC}. A high level allows the ISL32X77E to enter a low power mode when all channels are disabled. A low level prevents the device from entering the low power mode. (ISL32X77E only)
3, 5, 11, 13	3, 5, 11, 13	1, 6, 13, 18	RO1, RO2, RO3, RO4	Channel X receiver output: If A - B ≥ 200mV, RO is high; If A - B ≤ -200mV, RO is low. RO = High if A and B are unconnected (floating).
8	8	10, PAD	GND	Ground connection. This is also the potential of the QFN thermal pad.
2, 6, 10, 14	2, 6, 10, 14	24, 7, 12, 19	A1, A2, A3, A4	±16.5kV IEC61000-4-2 ESD Protected RS-485/422 level, channel X noninverting receiver input.
1, 7, 9, 15	1, 7, 9, 15	23, 8, 11, 20	B1, B2, B3, B4	±16.5kV IEC61000-4-2 ESD Protected RS-485/422 level, channel X inverting receiver input.
16	16	22	V_{CC}	System power supply input (3.0V to 5.5V). On devices with a V_L pin powered from a separate supply, power up V_{CC} first.
-	-	21	V_L	Logic power supply input (1.4V to V_{CC}) that powers all the TTL/CMOS inputs and outputs (logic pins). V_L sets the V_{IH} and V_{IL} levels of the enable and SHDNEN pins, and sets the V_{OH} level of the RO pins. Connect the V_L pin to the lower voltage power supply of a logic device (e.g., UART or µcontroller) interfacing with the ISL32X77E logic pins. If V_L and V_{CC} are different supplies, power up this supply after V_{CC}, and keep $V_L \leq V_{CC}$. To minimize input current and SHDN supply current, logic pins that are strapped high externally (preferably through a 1kΩ resistor) should connect to V_{CC}, but they may also connect to V_L. (ISL32X77E only)
-	-	5, 14	NC	No Connection.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL32173EIBZ	ISL32173 EIBZ	-40 to +85	16 Ld SOIC	M16.15
ISL32173EFBZ	ISL32173 EFBZ	-40 to +125	16 Ld SOIC	M16.15
ISL32173EIVZ	32173 EIVZ	-40 to +85	16 Ld TSSOP	MDP0044
ISL32173EFVZ	32173 EFVZ	-40 to +125	16 Ld TSSOP	MDP0044
ISL32175EIBZ	ISL32175 EIBZ	-40 to +85	16 Ld SOIC	M16.15
ISL32175EFBZ	ISL32175 EFBZ	-40 to +125	16 Ld SOIC	M16.15
ISL32175EIVZ	32175 EIVZ	-40 to +85	16 Ld TSSOP	MDP0044
ISL32175EFVZ	32175 EFVZ	-40 to +125	16 Ld TSSOP	MDP0044
ISL32177EIRZ	321 77EIRZ	-40 to +85	24 Ld QFN	L24.4x4C
ISL32177EFRZ	321 77EFRZ	-40 to +125	24 Ld QFN	L24.4x4C
ISL32273EIBZ	ISL32273 EIBZ	-40 to +85	16 Ld SOIC	M16.15
ISL32273EFBZ	ISL32273 EFBZ	-40 to +125	16 Ld SOIC	M16.15
ISL32273EIVZ	32273 EIVZ	-40 to +85	16 Ld TSSOP	MDP0044
ISL32273EFVZ	32273 EFVZ	-40 to +125	16 Ld TSSOP	MDP0044
ISL32275EIBZ	ISL32275 EIBZ	-40 to +85	16 Ld SOIC	M16.15
ISL32275EFBZ	ISL32275 EFBZ	-40 to +125	16 Ld SOIC	M16.15
ISL32275EIVZ	32275 EIVZ	-40 to +85	16 Ld TSSOP	MDP0044
ISL32275EFVZ	32275 EFVZ	-40 to +125	16 Ld TSSOP	MDP0044
ISL32277EIRZ	322 77EIRZ	-40 to +85	24 Ld QFN	L24.4x4C
ISL32277EFRZ	322 77EFRZ	-40 to +125	24 Ld QFN	L24.4x4C

NOTES:

1. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL32173E,ISL32175E,ISL32177E,ISL32273E, ISL32275E, ISL32277E. For more information on MSL please see tech brief TB363.

Truth Tables

RECEIVER OUTPUT (ROX ENABLED, ALL VERSIONS)	
INPUTS (A-B)	**OUTPUT (RO)**
≥0.2V	1
≤-0.2V	0
Inputs Open (Floating)	1

RECEIVER ENABLE (ISL32173E, ISL32273E)		
INPUTS		**OUTPUTS**
EN	$\overline{EN}$	ROX
X	0	ENABLED
1	X	ENABLED
0	1	DISABLED*

NOTE: *Low Power SHDN Mode When Disabled

Truth Tables (Continued)

RECEIVER ENABLE (ISL32175E, ISL32275E)					
INPUTS		OUTPUTS			
EN12	EN34	RO1	RO2	RO3	RO4
0	0	Z*	Z*	Z*	Z*
0	1	Z	Z	EN	EN
1	0	EN	EN	Z	Z
1	1	EN	EN	EN	EN

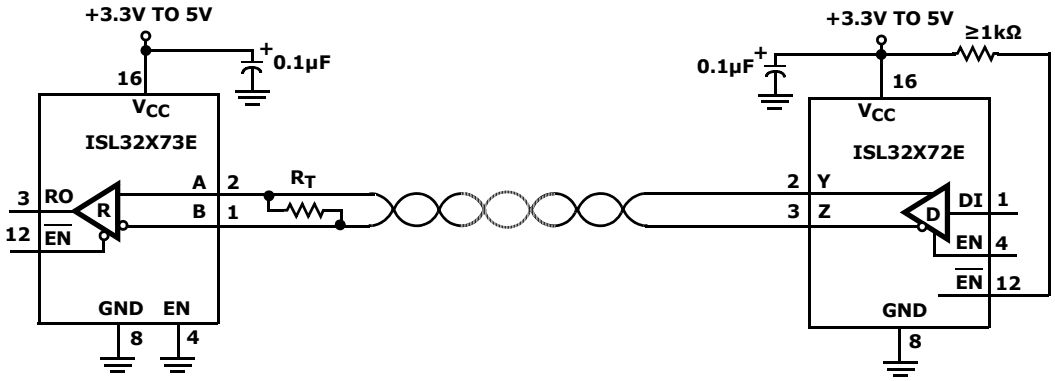
NOTE: *Low Power SHDN Mode When All Outputs Disabled; Z = Tri-state

RECEIVER ENABLE (ISL32177E, ISL32277E)					
INPUTS				OUTPUTS	
ENX	EN	$\overline{EN}$	SHDNEN	ROX	COMMENTS
0	X	X	0	Z	Chan X output disabled
EN1-4 = 0	X	X	1	Z*	All outputs disabled
X	0	1	0	Z	All outputs disabled
X	0	1	1	Z*	All outputs disabled
1	X	0	X	EN	Individual ENX controls chan
1	1	X	X	EN	

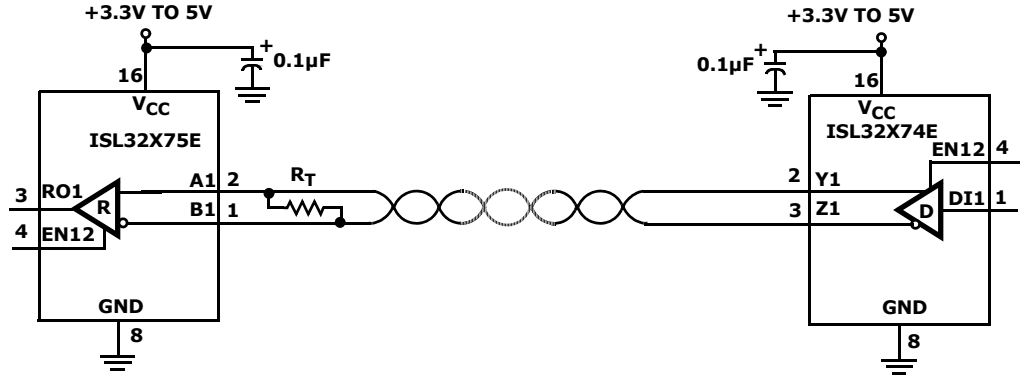
NOTE: * Low Power SHDN Mode; Z = Tri-state

Typical Operating Circuits (1 of 4 Channels Shown)

NETWORK USING GROUP ENABLES

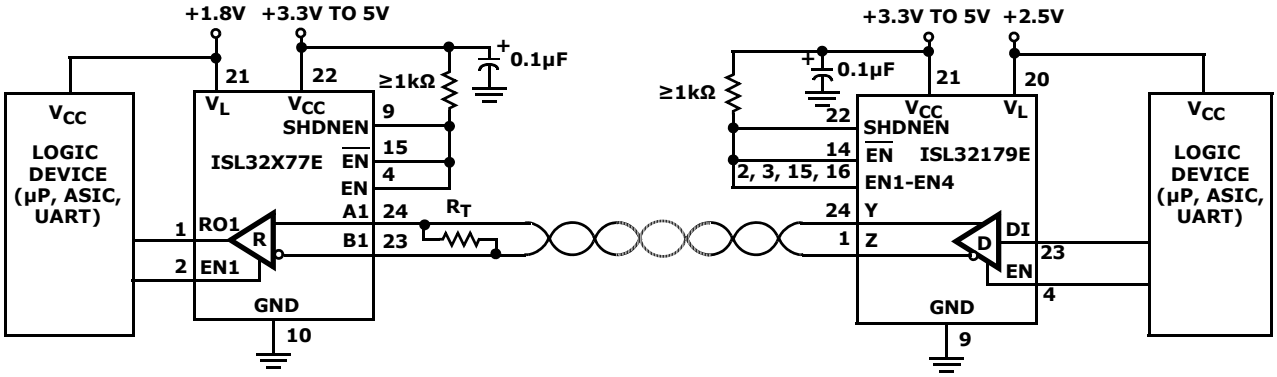


NETWORK USING PAIRED ENABLES



Typical Operating Circuits (1 of 4 Channels Shown) (Continued)

NETWORK WITH V_L PIN FOR INTERFACING TO LOWER VOLTAGE LOGIC DEVICES



USING INDIVIDUAL CHANNEL ENABLES AND CONFIGURED FOR LOWEST SHDN SUPPLY CURRENT
NOTE: IF POWERED FROM SEPARATE SUPPLIES, POWER UP V_{CC} BEFORE V_L

USING ACTIVE HIGH GROUP ENABLE AND CONFIGURED FOR LOWEST SHDN SUPPLY CURRENT
NOTE: IF POWERED FROM SEPARATE SUPPLIES, POWER UP V_{CC} BEFORE V_L

Absolute Maximum Ratings

V_{CC} to GND 7V
V_L to GND (Note 4) . . . . . -0.3V to (V_{CC} +0.3V)
Input Voltages
EN (All varieties) . . . . . -0.3V to 7V
A, B . . . . . -9V to +13V
Output Voltages
RO (Note 5) . . . . . -0.5V to (V_{CC} + 0.3V)
RO (Note 4) . . . . . -0.5V to (V_L + 0.3V)
Short Circuit Duration
RO (One output at a time) . . . . . Indefinite
ESD Rating . . . . . See "Electrical Specifications" Table

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SOIC Package (Notes 6, 9)	78	30
16 Ld TSSOP Package (Notes 6, 9)	104	25
24 Ld QFN Package (Notes 7, 8)	42	5

Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltages
V_{CC} . . . . . 3V to 5.5V
V_L (Note 4) . . . . . 1.6V to V_{CC}
Temperature Range
ISL32X7XEI . . . . . -40°C to +85°C
ISL32X7XEF . . . . . -40°C to +125°C
Bus Pin Common Mode Voltage Range . . . . . -7V to +12V
RO Output Current . . . . . -9mA to +9mA
RO Load Capacitance . . . . . ≤6pF

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. ISL32177E and ISL32277E only.
5. Excluding the ISL32177E and ISL32277E.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
8. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
9. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL32177E and ISL32277E only); Typicals are at the worst case of V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. **Boldface limits apply over the operating temperature range.** (Notes 10, 14)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
DC CHARACTERISTICS								
Input High Voltage (Logic Pins, Note 17)	V_{IH1}	V_L = V_{CC} if ISL32177E or ISL32277E	V_{CC} ≤3.6V	Full	**2**	-	-	V
	V_{IH2}		V_{CC} ≤ 5.5V	Full	**2.2**	-	-	V
	V_{IH3}	2.7V ≤ V_L < 3.0V (ISL32177E and ISL32277E Only)		Full	**2**	-	-	V
	V_{IH4}	2.3V ≤ V_L < 2.7V (ISL32177E and ISL32277E Only)		Full	**1.6**	-	-	V
	V_{IH5}	1.6V ≤ V_L < 2.3V (ISL32177E and ISL32277E Only)		Full	**0.72*V_L**	-	-	V
	V_{IH6}	1.4V ≤ V_L < 1.6V (ISL32177E and ISL32277E Only)		25	-	0.4*V_L	-	V
Input Low Voltage (Logic Pins, Note 17)	V_{IL1}	V_L = V_{CC} if ISL32177E and ISL32277E		Full	-	-	**0.8**	V
	V_{IL2}	V_L ≥ 2.7V (ISL32177E and ISL32277E Only)		Full	-	-	**0.6**	V
	V_{IL3}	2.3V ≤ V_L < 2.7V (ISL32177E and ISL32277E Only)		Full	-	-	**0.6**	V
	V_{IL4}	1.6V ≤ V_L < 2.3V (ISL32177E and ISL32277E Only)		Full	-	-	**0.22*V_L**	V
	V_{IL5}	1.4V ≤ V_L < 1.6V (ISL32177E and ISL32277E Only)		25		0.35* V_L	-	V

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL32177E and ISL32277E only); Typicals are at the worst case of V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. **Boldface limits apply over the operating temperature range.** (Notes 10, 14) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
Logic Input Current	I_{IN1}	EN, $\overline{EN}$, ENX, SHDNEN = 0V or V_{CC}		Full	**-15**	-	**15**	µA
	I_{IN2}	EN12, EN34 = 0V or V_{CC} (ISL32X75E Only)		Full	**-30**	-	**30**	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	**-200**	-	**200**	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	30	-	mV
Input Current (A, B)	I_{IN3}	V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	-	**0.2**	mA
			V_{IN} = -7V	Full	**-0.2**	-	-	mA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	**48**	-	-	kΩ
Receiver Output Leakage Current	I_{OZ}	EN = 0V, 0 ≤ V_O ≤ V_{CC} (0 to V_L if ISL32177E or ISL32277E)		Full	**-10**	-	**10**	µA
Receiver Short-Circuit Current, V_O = High or Low	I_{OS}	EN = 1, 0V ≤ V_O ≤ V_{CC} (0 to V_L if ISL32177E or ISL32277E)	20Mbps Versions	Full	-	-	**±100**	mA
			80Mbps Versions	Full	-	-	**±155**	mA
Receiver Output High Voltage	V_{OH1}	I_O = -8mA, V_{ID} = 200mV (V_L = V_{CC} if ISL32177E or ISL32277E)	V_{CC} ≥ 4.5V	Full	**V_{CC} - 1**	-	-	V
		I_O = -6mA, V_{ID} = 200mV (V_L = V_{CC} if ISL32177E or ISL32277E)	V_{CC} ≥ 3.0V	Full	**2.4**	-	-	V
	V_{OH2}	I_O = -2mA, V_L ≥ 2.3V	ISL32177E and ISL32277E Only	Full	**V_L - 0.3**	-	-	V
	V_{OH3}	I_O = -1.5mA, V_L = 1.8V		Full	**V_L - 0.3**	-	-	V
	V_{OH4}	I_O = -200µA, V_L ≥ 1.4V		Full	**V_L - 0.2**	-	-	V
Receiver Output Low Voltage	V_{OL1}	I_O = 8mA, V_{ID} = -200mV, V_L = V_{CC} if ISL32177E, ISL32277E		Full	-	-	**0.4**	V
	V_{OL2}	I_O = 5mA, V_L ≥ 1.8V	ISL32177E and ISL32277E Only	Full	-	-	**0.4**	V
	V_{OL3}	I_O = 2mA, V_L ≥ 1.4V	ISL32177E and ISL32277E Only	Full	-	-	**0.4**	V
SUPPLY CURRENT								
No-Load Supply Current, 80Mbps Versions	$80I_{CC}$	EN = 1, or $\overline{EN}$ = 0 (ISL32173E and ISL32177E), or EN12 = EN34 = 1 (ISL32175E), or EN1 = EN2 = EN3 = EN4 = 1 (ISL32177E)		Full	-	-	**15**	mA
	$80I_{CC1/2}$	EN12 = 1 and EN34 = 0, or vice versa (ISL32175E only), or if only two channels are enabled on the ISL32177E		Full	-	-	**8.5**	mA
	$80I_{CCD}$	SHDNEN = 0, EN1 = EN2 = EN3 = EN4 = 0 or EN = 0 and $\overline{EN}$ = 1 (ISL32177E only)		Full	-	-	**2.5**	mA

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL32177E and ISL32277E only); Typicals are at the worst case of V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. **Boldface limits apply over the operating temperature range.** (Notes 10, 14) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
No-Load Supply Current, 20Mbps Versions	$20I_{CC}$	EN = 1, or $\overline{EN}$ = 0 (ISL32273E and ISL32277E), or EN12 = EN34 = 1 (ISL32275E), or EN1 = EN2 = EN3 = EN4 = 1 (ISL32277E)		Full	-	-	**5.5**	mA
	$20I_{CC1/2}$	EN12 = 1 and EN34 = 0, or vice versa (ISL32275E only), or if only two channels are enabled on the ISL32277E		Full	-	-	**3.5**	mA
	$20I_{CCD}$	SHDNEN = 0, EN1 = EN2 = EN3 = EN4 = 0 or EN = 0 and $\overline{EN}$ = 1 (ISL32277E only)		Full	-	-	**1.2**	mA
Shutdown Supply Current	I_{SHDN}	All outputs disabled (Note 18) (all except ISL32X75E)		Full	-	-	**15**	µA
		All outputs disabled (Note 19) (all except ISL32X73E)		Full	-	-	**60**	µA
ESD PERFORMANCE								
RS-485 Pins (A, B)		IEC61000-4-2, From Bus Pins to GND	Air Gap	25	-	±16.5	-	kV
			Contact	25	-	±8	-	kV
		Human Body Model, From Bus Pins to GND		25	-	±15	-	kV
All Pins		HBM		25	-	±8	-	kV
		Machine Model		25	-	500	-	V
RECEIVER SWITCHING CHARACTERISTICS (ISL32273E, ISL32275E, ISL32277E, 20Mbps)								
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, C_L=15pF		Full	**20**	-	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 1)		Full	-	37	**55**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 1)		Full	-	2.7	**6**	ns
Prop Delay Skew Chan-to-Chan	t_{SKC-C}	(Figure 1), (Note 11)		Full	-	3	**8**	ns
Prop Delay Skew Part-to-Part	t_{SKP-P}	(Figure 1), (Note 12)		Full	-	4	**20**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2), (Notes 15, 21)		Full	-	150	**190**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2), (Notes 15, 21)		Full	-	155	**190**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2)		Full	-	19	**30**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2)		Full	-	19	**30**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2), (Notes 16, 20)		Full	-	-	**850**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2), (Notes 16, 20)		Full	-	-	**850**	ns
RECEIVER SWITCHING CHARACTERISTICS (ISL32173E, ISL32175E, ISL32177E, 80Mbps)								
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, C_L≤ 15pF	V_{CC}≤ 3.6V	Full	**80**	-	-	Mbps
			V_{CC} > 3.6V	Full	**20**	-	-	Mbps
		V_{ID} = ±1.5V, C_L≤ 6pF, 3.6V ≤ V_{CC} ≤ 5.5V		Full	**80**	-	-	Mbps

Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; V_L = V_{CC} (ISL32177E and ISL32277E only); Typicals are at the worst case of V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. **Boldface limits apply over the operating temperature range.** (Notes 10, 14) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 13)	TYP	MAX (Note 13)	UNITS
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 1)	Full	**7**	11	**16**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 1)	Full	-	0.4	**2**	ns
Prop Delay Skew Chan-to-Chan	t_{SKC-C}	(Figure 1), (Note 11)	Full	-	0.7	**4**	ns
Prop Delay Skew Part-to-Part	t_{SKP-P}	(Figure 1), (Note 12)	Full	-	1.2	**8**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2), (Notes 15, 21)	Full	-	57	**75**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2), (Notes 15, 21)	Full	-	59	**75**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2)	Full	-	18	**30**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2)	Full	-	19	**30**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 2), (Notes 16, 20)	Full	-	-	**850**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 2), (Notes 16, 20)	Full	-	-	**850**	ns

NOTES:

10. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
11. Channel-to-channel skew is the magnitude of the worst case delta between any two propagation delays of any two outputs on the same IC, at the same test conditions.
12. t_{SKP-P} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC}, temperature, etc.).
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. EN = 0 indicates that the output(s) under test are disabled via the appropriate logic pin settings. EN = 1 indicates that the logic pins are set to enable the output(s) under test.
15. For ISL32177E and ISL32277E, keep SHDNEN low to avoid entering SHDN. For ISL32175E and ISL32275E ensure that at least one channel remains enabled to prevent SHDN.
16. For ISL32177E and ISL32277E, keep SHDNEN high to enter SHDN when all drivers are disabled.
17. Logic Pins are the enable variants and SHDNEN.
18. EN low and $\overline{EN}$ high on the ISL32X73E. SHDNEN, $\overline{EN}$, EN1-EN4 all high and EN low on the ISL32X77E.
19. EN12 and EN34 low on ISL32X75E. SHDNEN high, with EN1-EN4 low plus EN and $\overline{EN}$ high on the ISL32X77E.
20. Shutdown is entered by simultaneously disabling all four outputs for at least 600ns.
21. Does not apply to the ISL32173E nor the ISL32273E; only the EN from SHDN parameters apply to these two parts.

Test Circuits and Waveforms

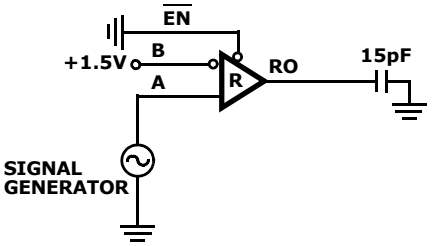


FIGURE 1A. TEST CIRCUIT

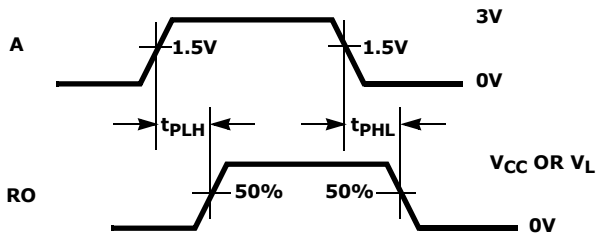
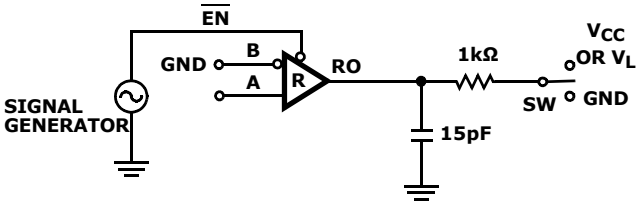


FIGURE 1B. MEASUREMENT POINTS

FIGURE 1. RECEIVER PROPAGATION DELAY



PARAMETER	A	SW
t_{HZ}	+1.5V	GND
t_{LZ}	-1.5V	V_{CC}
t_{ZH} (Notes 15, 21)	+1.5V	GND
t_{ZL} (Notes 15, 21)	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Notes 16, 20)	+1.5V	GND
$t_{ZL(SHDN)}$ (Notes 16, 20)	-1.5V	V_{CC}

FIGURE 2A. TEST CIRCUIT

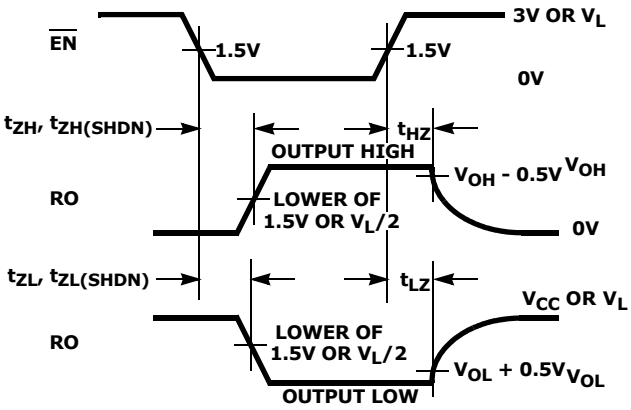


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize differential receivers for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 48kΩ surpasses the RS-422 specification of 4kΩ and is four times the RS-485 "Unit Load (UL)" requirement of 12kΩ minimum. Thus, these products are known as "one-quarter UL" receivers and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common mode voltages as great as +9V/-7V outside the power supplies (i.e., +12V and -7V with V_{CC} = 3.0V), making them ideal for long networks where induced voltages, and ground potential differences are realistic concerns.

All the receivers include a "fail-safe open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

All receivers easily support a 20Mbps data rate, and the ISL32173E, ISL32175E, and ISL32177E support data rates up to 80Mbps. All receiver outputs are tri-statable, with the enable scheme varying by part type (see next section).

Receiver Enable Functions

All product types include functionality to allow disabling of the Rx outputs. The ISL32X73E types feature group (all four Rx) enable functions that are active high (EN) or active low ($\overline{EN}$). Receivers enable when EN = 1, or when $\overline{EN}$ = 0, and they disable only when EN = 0 and $\overline{EN}$ = 1. ISL32X75E versions use active high paired enable

functions (EN12 and EN34) that enable (when high) or disable (when low) the corresponding pairs of Rx. All four of these enable pins have internal pull-up resistors to V_{CC}, but unused enable pins that need to be high (e.g., $\overline{EN}$ when using the EN input for enable control, or EN12 and EN34 when using always enabled receivers) should always be connected externally to V_{CC}. If V_{CC} transients might exceed 7V, then inserting a series resistor between the input(s) and V_{CC} limits the current that flows if the input's ESD protection starts conducting.

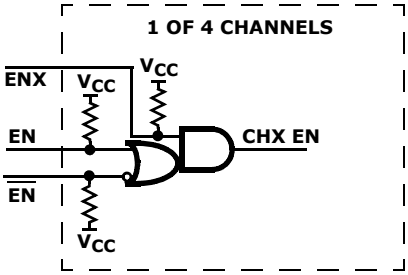


FIGURE 3. ISL32X77E ENABLE LOGIC

The ISL32177E and ISL32277E have the most flexible enable scheme. Their six enable pins allow for group, paired, or individual channel enable control. Figure 3 details the ISL32X77E's internal enable logic. To utilize a group enable function, connect all the ENX pins high, and handle the EN and $\overline{EN}$ pins as described in the previous paragraph. For paired enables, connect EN and $\overline{EN}$ high (for the lowest current in SHDN mode, if SHDN is used) and tie EN1 and EN2 together, and EN3 and EN4 together. For individual channel enables, again connect EN and $\overline{EN}$ high, and drive the appropriate ENX (active high) for the particular channel. All six enable pins incorporate pull-up resistors to V_{CC}, but unused enable pins of any type should be externally connected high, rather than being left floating. Connecting to V_{CC} is the best choice, but V_L may be utilized as long as SHDN power isn't a primary concern (for each V_L connected input, I_{CC} increases by $(V_{CC} - V_L)/600k\Omega$). If V_{CC} or V_L transients might exceed 7V, then inserting a series resistor between the input(s) and the supply limits the current that will flow if the input's ESD protection starts conducting.

Wide Supply Range

The ISL32X7XE design operates with a wide range of supply voltages from 3.0V to 5.5V, and the receivers meet the RS-485 specs for that full supply voltage range.

5.5V TOLERANT LOGIC PINS

Logic input pins (enables, SHDNEN) contain no ESD nor parasitic diodes to V_{CC} (nor to V_L), so they withstand input voltages exceeding 5.5V regardless of the V_{CC} and V_L voltages (see Figure 6).

Logic Supply (V_L Pin, ISL32177E and ISL32277E)

Note: If powered from separate supplies, power up V_{CC} before powering up the V_L supply.

The ISL32177E and ISL32277E include a V_L pin that powers the logic inputs (enables, SHDNEN) and the RO outputs. These pins interface with "logic" devices such as UARTs, ASICs, and µcontrollers, and today most of these devices use power supplies significantly lower than 3.3V. Thus, a 5V or 3.3V RO output level from an ISL32X77E IC might seriously overdrive and damage the logic device input (Figure 4). Similarly, the logic device's low V_{OH} might not exceed the V_{IH} of the ISL32X77E's 3.3V or 5V powered enable input. Connecting the ISL32X77E's V_L pin to the power supply of the logic device - as shown in Figure 4 - limits the ISL32X77E's V_{OH} to V_L, and reduces its logic input switching points to values compatible with the logic device's output levels. Tailoring the logic pin input switching points and RO output levels to the supply voltage of the UART, ASIC, or µcontroller eliminates the need for a level shifter/translator between the two ICs.

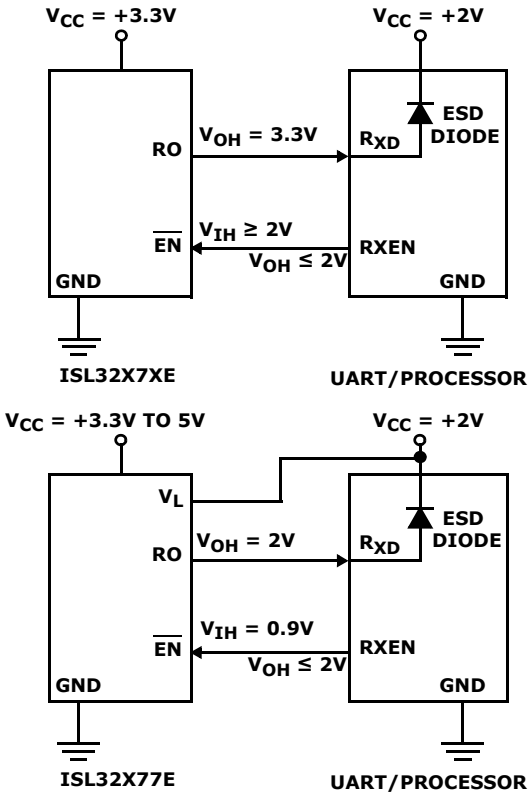


FIGURE 4. USING V_L PIN TO ADJUST LOGIC LEVELS

V_L can be anywhere from V_{CC} down to 1.4V, but the data rate drops off dramatically below V_L = 1.6V. Table 2 indicates typical V_{IH} and V_{IL} values (applicable to both speed grades) for various V_L settings, and also lists the ISL32177E's typical data rate versus V_L. The ISL32277E typically runs at 20Mbps for $V_L \geq 1.6V$, and drops to 10Mbps to 15Mbps at V_L=1.4V. Prop delays, skews, and transition times increase at lower V_L, as shown in Figures 17 through 29.

TABLE 2. TYPICAL V_{IH}, V_{IL} AND DATA RATE vs. V_L FOR V_{CC} = 3.3V OR 5V

V_L (V)	V_{IH} (V)	V_{IL} (V)	ISL32177E DATA RATE (Mbps)
1.4	0.55	0.5	25
1.6	0.6	0.55	50
1.8	0.8	0.7	65
2.3	1	0.9	70
2.7	1.1	1	75
3.3	1.3	1.2	80

Neglecting the RO I_{OH} currents, the quiescent V_L supply current (I_L) is typically less than 1µA for enable input voltages at ground or V_L, as shown in Figure 6. Enable pin pull-up resistors connect to V_{CC}, so the current due to a low enable input adds to I_{CC} rather than to I_L.

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (EN, $\overline{EN}$, ENX) is unable to ensure that the RS-485 Rx outputs are kept disabled. If the equipment is connected to the bus, a receiver activating prematurely during power up may generate RO transitions that could cause interrupts. To avoid this scenario, this family incorporates a "Hot Plug" function. During power up, circuitry monitoring V_{CC} ensures that the Rx outputs remain disabled for a period of time, regardless of the state of the enables. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

ESD Protection

All pins on these devices include class 3 (>8kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM, and ±16.5kV IEC 61000-4-2. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

IEC 61000-4-2 Testing

The IEC 61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The A and B RS-485 pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. These Quad receivers survive ±8kV contact discharges on the RS-485 pins.

Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Networks operating at 80Mbps are limited to lengths much less than 100' (30m), while a 20Mbps version can operate at full data rates with lengths up to 200' (60m).

Any of these ICs may be used at slower data rates over longer cables, but there are some limitations for the 80Mbps versions. The 80Mbps Rx is optimized for high speed operation, so its output may glitch if the Rx input differential transition times are too slow. Keeping the transition times below 500ns, which equates to a Tx driving a 1000' (305m) CAT 5 cable, yields excellent performance over the full operating temperature range.

Twisted pair is the cable of choice for RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

When using these receivers, proper termination is imperative to minimize reflections. Short networks using slew rate limited transmitters need not be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on a bus with multiple receivers) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at

both ends. Stubs connecting a transmitter or receiver to the main cable should be kept as short as possible.

Low Power Shutdown Mode

These BiCMOS receivers all use a fraction of the power required by their bipolar counterparts, but they also include a shutdown (SHDN) feature that reduces the already low quiescent ICC to a microamp trickle. These devices enter shutdown only when all four receivers disable (see "Truth Tables" on page 4) for at least 600ns. The ISL32X73E types enter SHDN whenever EN is low and $\overline{EN}$ is high. ISL32X75E types enter SHDN only if both EN12 and EN34 are low. Note that the ISL32X75E enable times increase significantly when enabling from the SHDN condition.

The ISL32X77E enter the low power SHDN mode if SHDNEN is high, and if all four Rx are disabled for at least 600ns. This is accomplished by driving EN low and $\overline{EN}$ high, or by driving all four ENX inputs low. Enable times increase if the IC was in SHDN, so if enable time is more important than SHDN supply current, tying the SHDNEN pin low defeats the low power SHDN feature. In this mode, the supply current drops to 1mA to 2mA when all four Rx are disabled, but the enable time of any Rx remains below 200ns.

Remember that all enable pins have pull-up resistors on them, so each pin that is low during SHDN adds up to 15µA to the SHDN supply current. The SHDN supply current entries in the "Electrical Specifications" table on page 9 include the resistor currents of the pins indicated to be in the low state.

Typical Performance Curves

C_L= 15pF, V_{CC} = V_L = 3.3V or 5V, T_A = +25°C; Unless Otherwise Specified. V_L Notes Apply To The ISL32177E And ISL32277E Only.

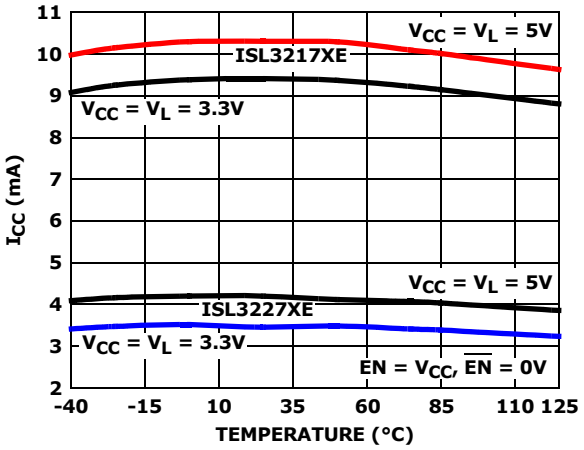


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE

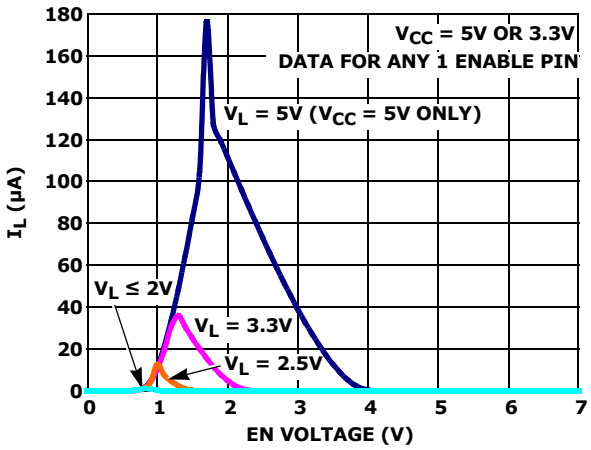


FIGURE 6. V_L SUPPLY CURRENT vs ENABLE PIN VOLTAGE (ISL32X77E ONLY)

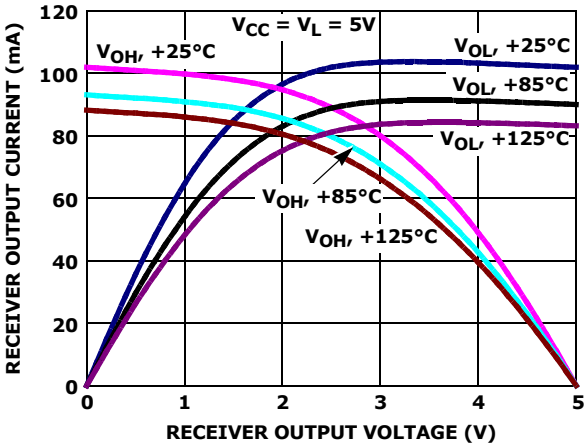


FIGURE 7. ISL3217XE RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

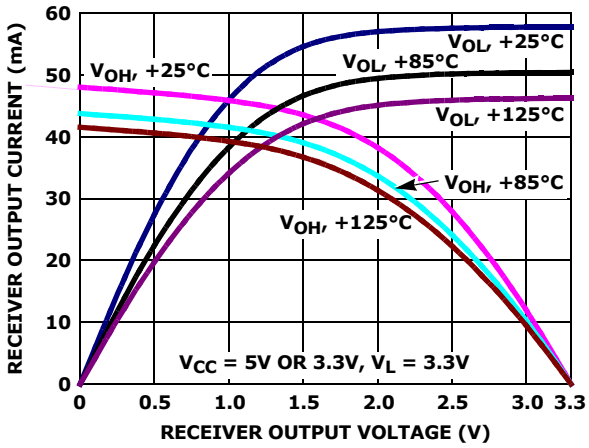


FIGURE 8. ISL3217XE RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

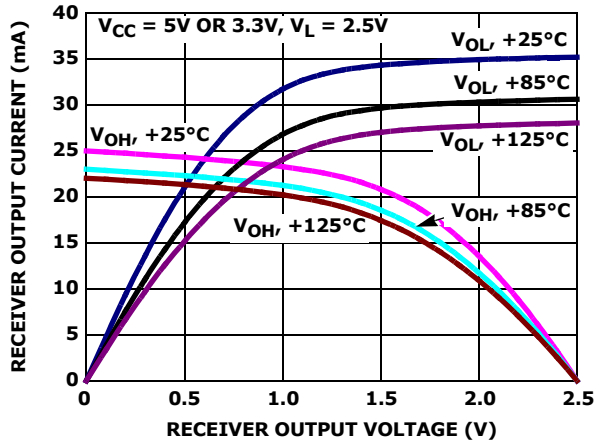


FIGURE 9. ISL32177E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

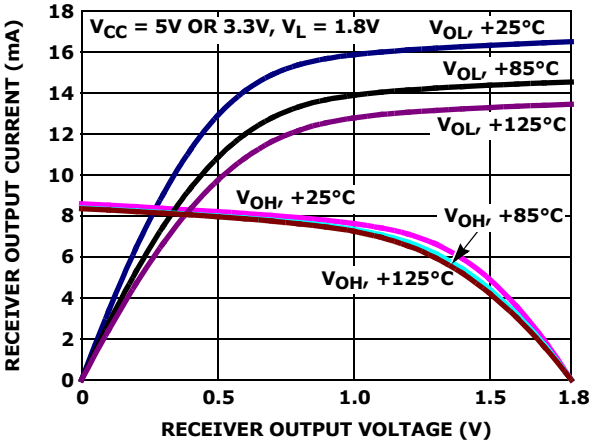


FIGURE 10. ISL32177E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Typical Performance Curves

C_L= 15pF, V_{CC} = V_L = 3.3V or 5V, T_A = +25°C; Unless Otherwise Specified. V_L Notes Apply To The ISL32177E And ISL32277E Only.

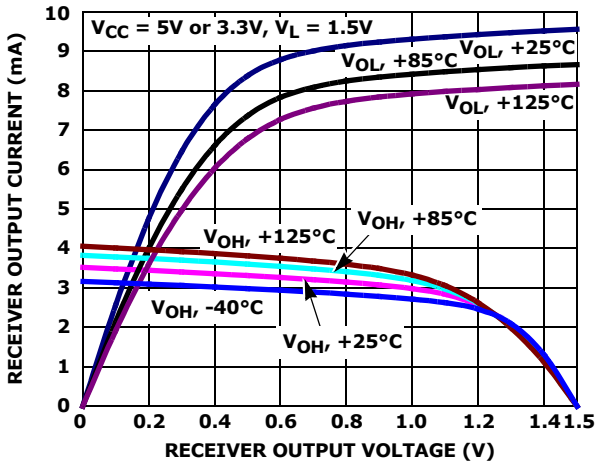


FIGURE 11. ISL32177E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

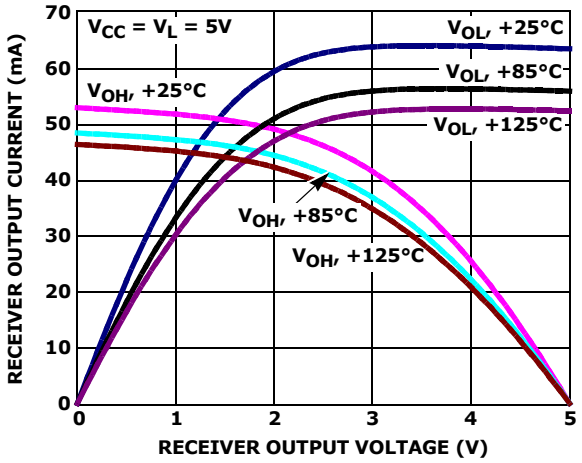


FIGURE 12. ISL3227XE RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

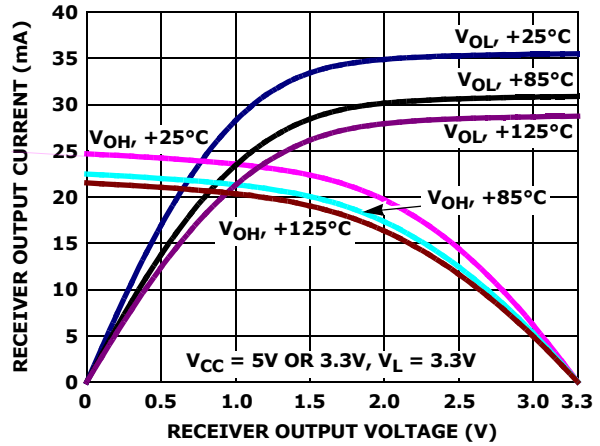


FIGURE 13. ISL3227XE RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

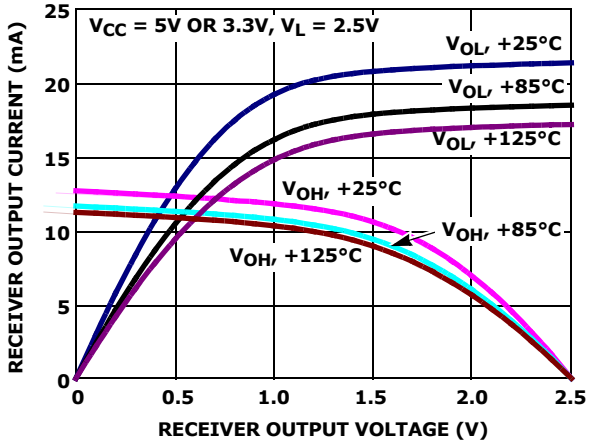


FIGURE 14. ISL32277E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

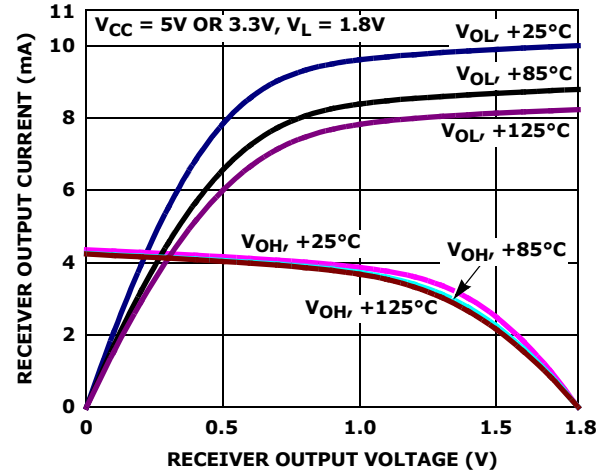


FIGURE 15. ISL32277E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

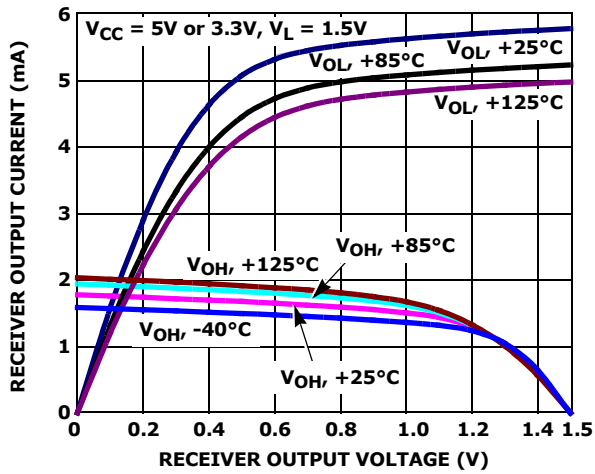


FIGURE 16. ISL32277E RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Typical Performance Curves

C_L= 15pF, V_{CC} = V_L = 3.3V or 5V, T_A = +25°C; Unless Otherwise Specified. V_L Notes Apply To The ISL32177E And ISL32277E Only.

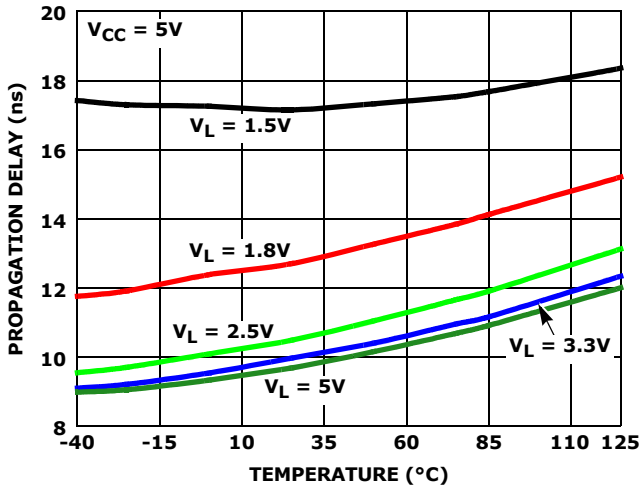


FIGURE 17. ISL3217XE RECEIVER PROPAGATION DELAY vs TEMPERATURE

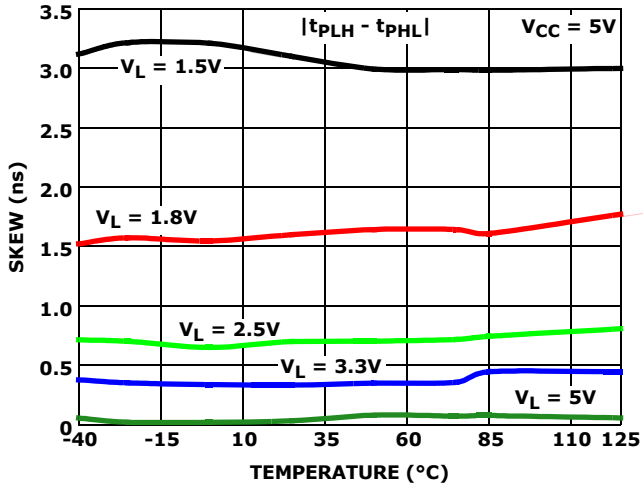


FIGURE 18. ISL3217XE RECEIVER SKEW vs TEMPERATURE

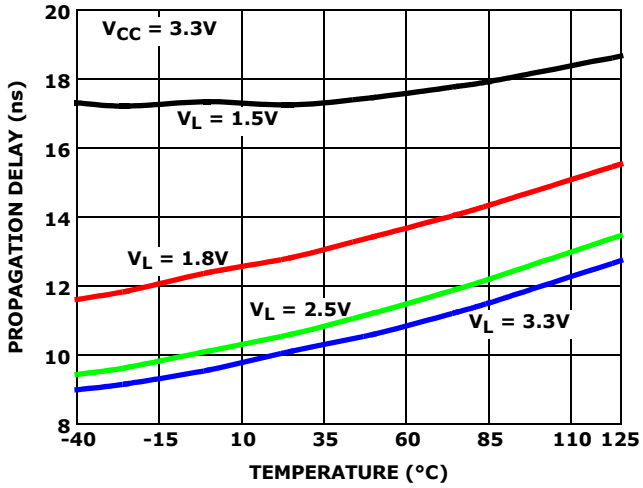


FIGURE 19. ISL3217XE RECEIVER PROPAGATION DELAY vs TEMPERATURE

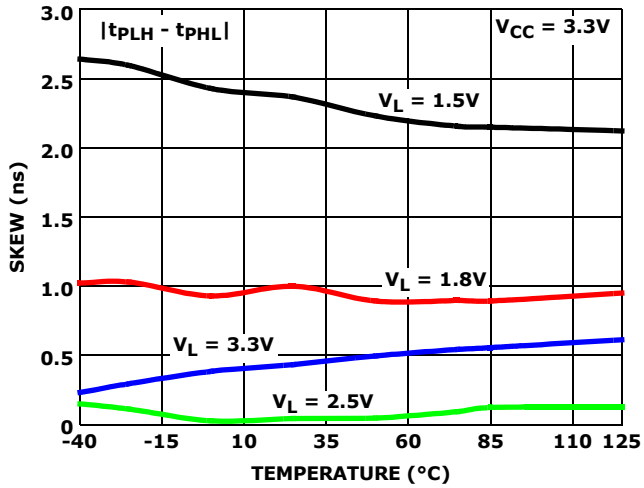


FIGURE 20. ISL3217XE RECEIVER SKEW vs TEMPERATURE

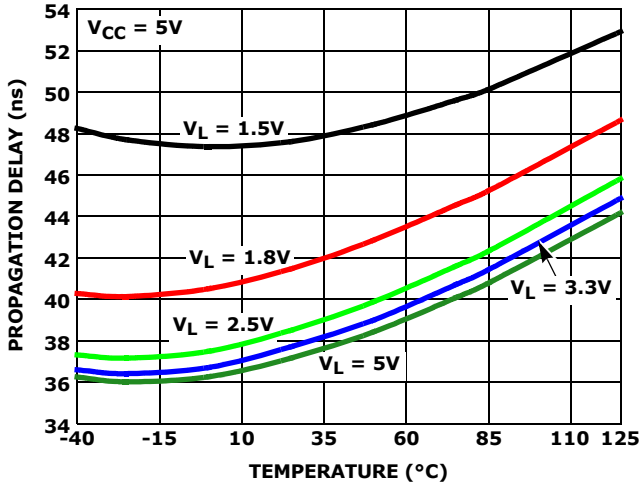


FIGURE 21. ISL3227XE RECEIVER PROPAGATION DELAY vs TEMPERATURE

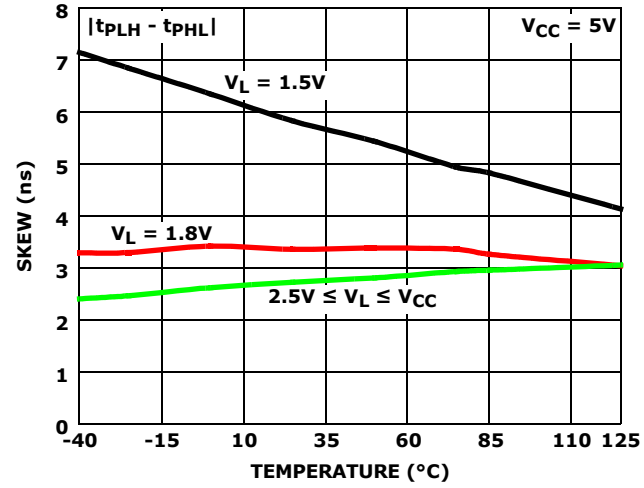


FIGURE 22. ISL3227XE RECEIVER SKEW vs TEMPERATURE

Typical Performance Curves

C_L= 15pF, V_{CC} = V_L = 3.3V or 5V, T_A = +25°C; Unless Otherwise Specified. V_L Notes Apply To The ISL32177E And ISL32277E Only.

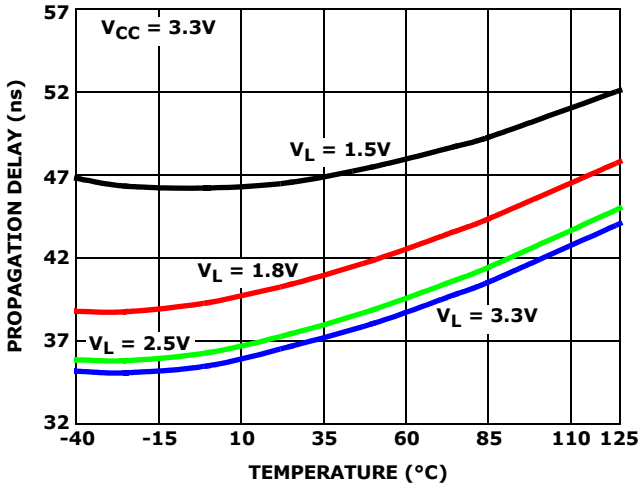


FIGURE 23. ISL3227XE RECEIVER PROPAGATION DELAY vs TEMPERATURE

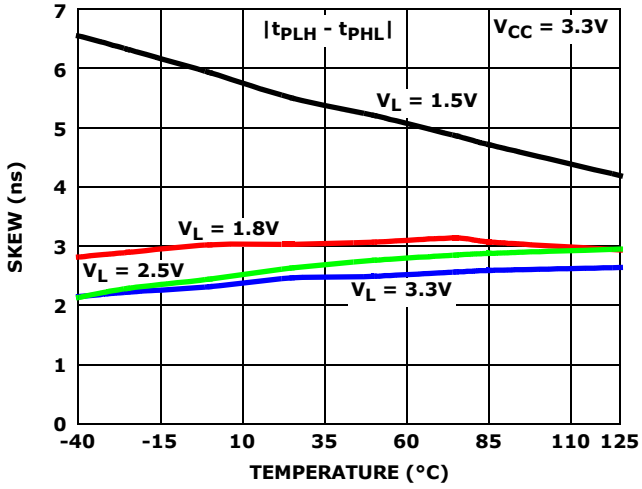


FIGURE 24. ISL3227XE RECEIVER SKEW vs TEMPERATURE

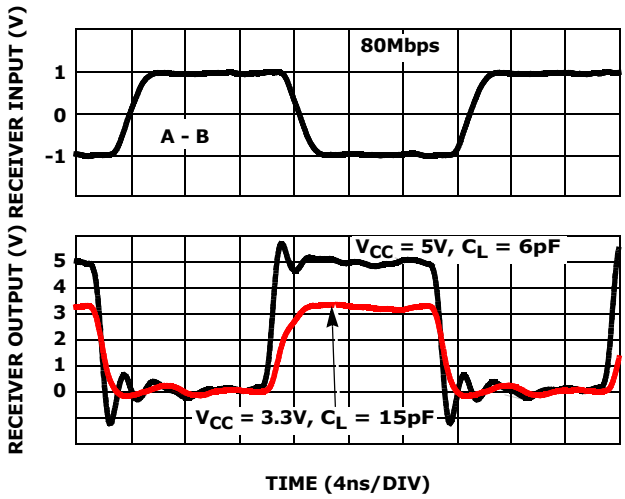


FIGURE 25. ISL3217XE RECEIVER WAVEFORMS

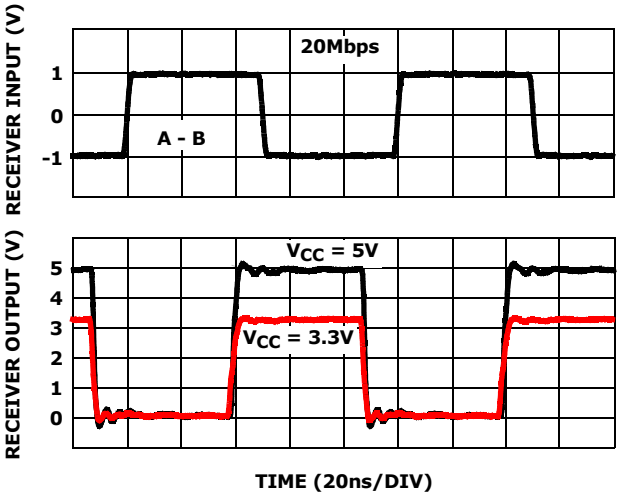


FIGURE 26. ISL3227XE RECEIVER WAVEFORMS

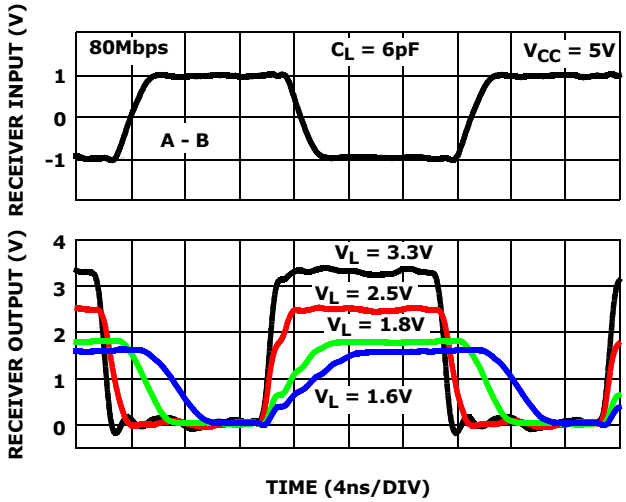


FIGURE 27. ISL32177E RECEIVER WAVEFORMS

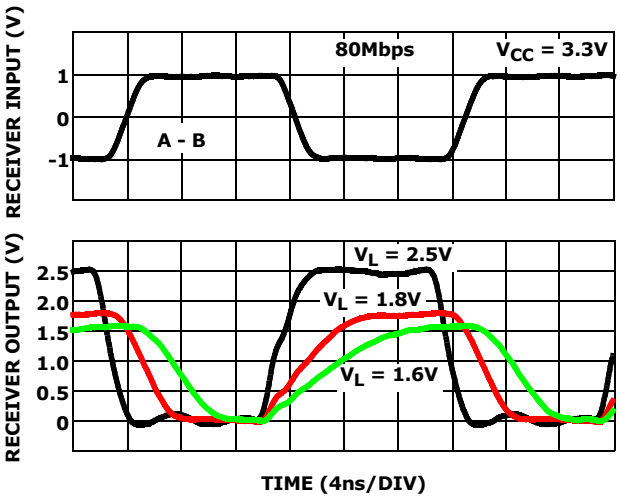


FIGURE 28. ISL32177E RECEIVER WAVEFORMS

Typical Performance Curves

C_L= 15pF, V_{CC} = V_L = 3.3V or 5V, T_A = +25°C; Unless Otherwise Specified. V_L Notes Apply To The ISL32177E And ISL32277E Only.

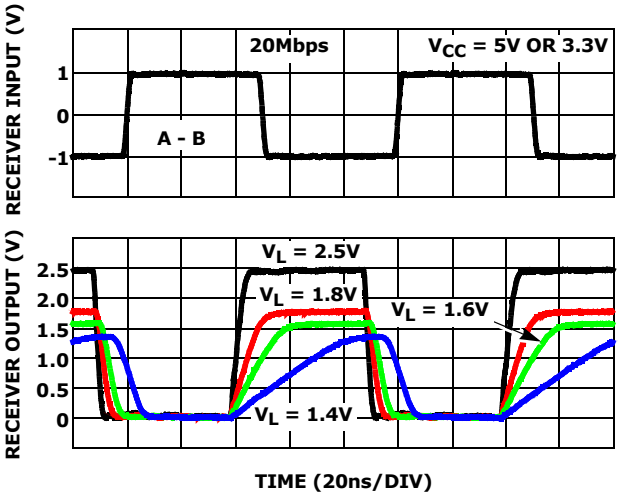


FIGURE 29. ISL32277E RECEIVER WAVEFORMS

Die Characteristics

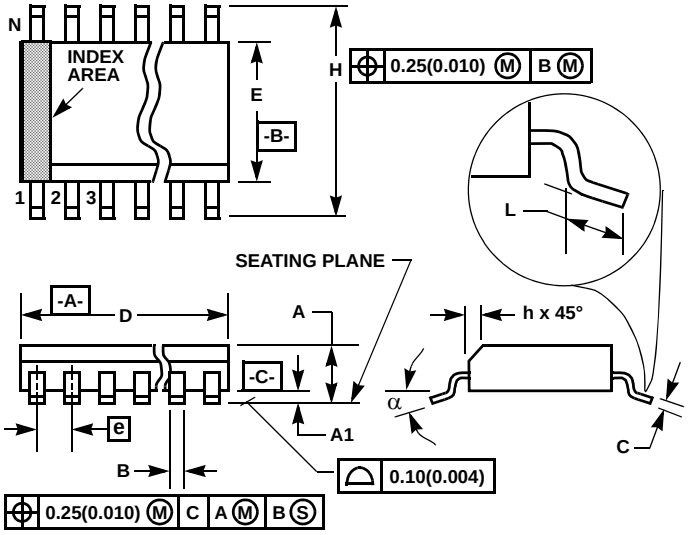
SUBSTRATE AND QFN THERMAL PAD POTENTIAL (POWERED UP):

GND

PROCESS:

Si Gate BiCMOS

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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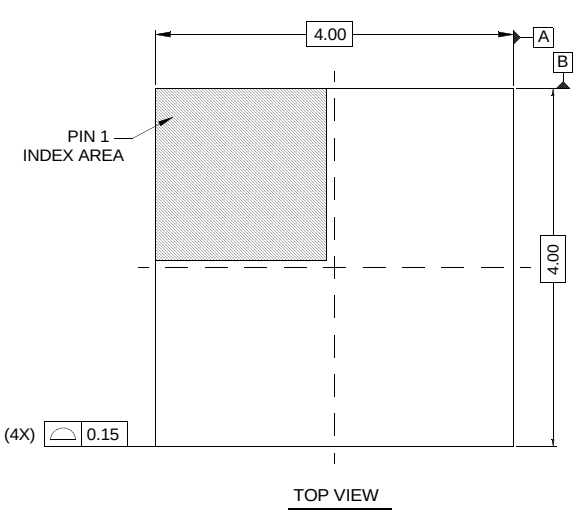
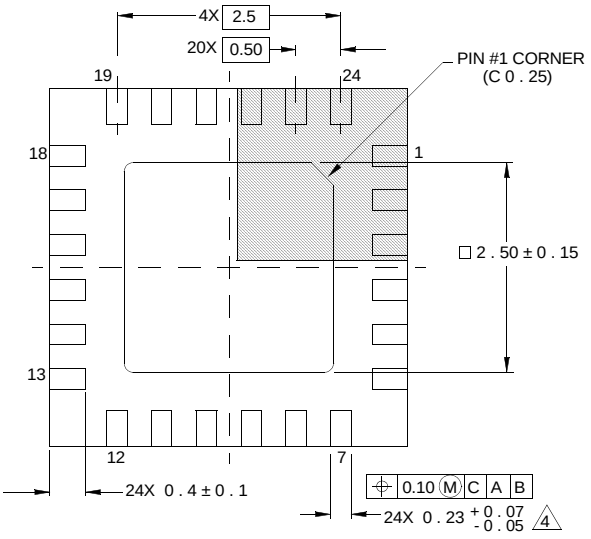
Package Outline Drawing

L24.4x4C

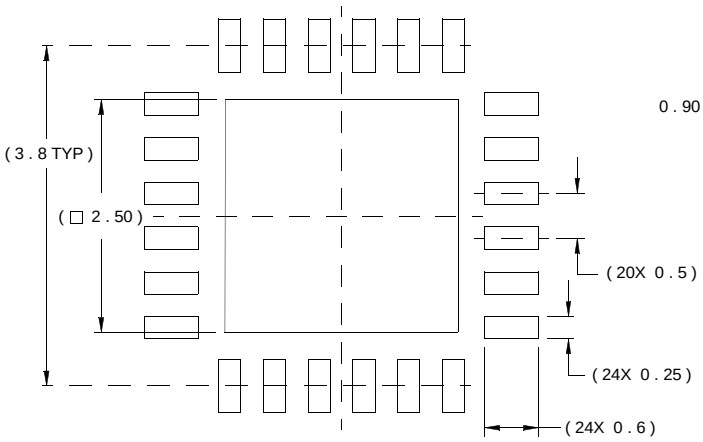
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



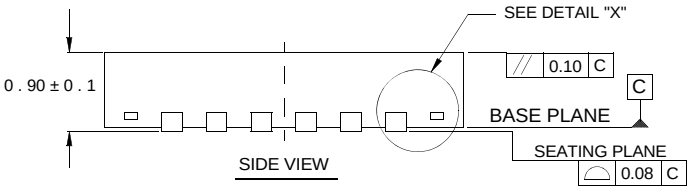
TOP VIEW



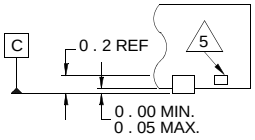
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

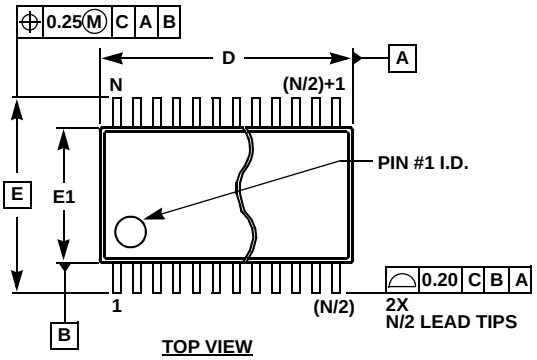


DETAIL "X"

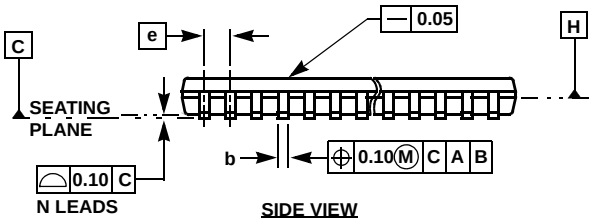
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

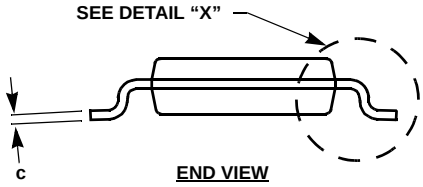
Thin Shrink Small Outline Package Family (TSSOP)



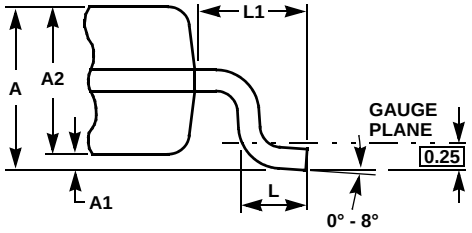
TOP VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

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NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.