PN746X_736X

NFC Cortex-M0 microcontroller

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Product data sheet
COMPANY PUBLIC

1. General description

The PN7462 family is a family of 32-bit ARM Cortex-M0-based NFC microcontrollers offering high performance and low power consumption. It has a simple instruction set and memory addressing along with a reduced code size compared to existing architectures. PN7462 family offers all in one solutions, with features such as NFC, microcontroller, optional contact smart card reader, and software in a single chip. It operates at CPU frequencies of up to 20 MHz.

The family includes the following derivatives to fit every specific need:

- PN7462: NFC microcontroller, 160 kB Flash memory, and an ISO 7816/EMVCo contact interface
- PN7362: NFC microcontroller with 160 kB Flash memory
- PN7360: NFC microcontroller with 80 kB Flash memory

The peripheral complement of the PN7462 family microcontrollers includes 160/80 kB of flash memory, 12 kB of SRAM data memory and 4 kB EEPROM. It also includes one host interface with either high-speed mode I^2C-bus, SPI, USB or high-speed UART, and two master interfaces, SPI and fast-mode plus I^2C-bus. Four general-purpose counter/timers, a random number generator, one CRC coprocessor and up to 21 general-purpose I/O pins are also available.

The PN7462 family NFC microcontrollers offer a one chip solution to build contactless applications. It is equipped with a highly integrated high-power output NFC-IC for contactless communication at 13.56 MHz enabling EMV-compliance on RF level, without additional external active components.

PN7462 family supports the following operating modes:

- ISO/IEC 14443-A and B, MIFARE
- JIS X 6319-4 (comparable with FeliCa scheme)
- ISO/IEC 15693, ICODE, ISO/IEC 18000-3 mode 3
- NFC protocols - tag reader/writer, P2P
- ISO/IEC 14443- type A card emulation
- EMVCo compliance

By integrating an ISO/IEC 7816 interface on a single chip in the PN7462, it provides a solution for dual interface smart card readers. PN7462 contact interface offers a high level of security for the card by performing current limiting, short-circuit detection, ESD

protection as well as supply supervision. An additional UART output is also implemented to address applications where more than one contact card slot is needed. It enables an easy connection to multiple smart card slot interfaces like TDA8026.

The V_{CC} is regulated at 5 V, 3 V, and 1.8 V. PN7462 provides thermal and short-circuit protection on all card contacts. It also provides automatic activation and deactivation sequences initiated by software or hardware. The sequences are activated or deactivated in the event of short-circuit, card removal, and overheating.

2. Features and benefits

2.1 Integrated contact interface frontend

- Class A, B, and C cards can work on 1.8 V, 3 V, and 5 V supply
- Specific ISO UART, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, and extra guard time register
- DC-to-DC converter for class A support starting at 3 V, and class B support starting at 2.7 V
- Thermal and short-circuit protection on contact cards
- Automatic activation and deactivation sequence, initiated by software or by hardware in case of short-circuit, card removal, overheating, and V_{DD} or V_{DD} drop-out
- Enhanced ESD protection (> 8 kV)
- ISO/IEC 7816 compliant
- EMVCo 4.3 compliant
- Clock generation up to 13.56 MHz
- Synchronous card support
- Possibility to extend the number of contact interfaces, with the addition of slot extenders such as TDA8026

2.2 Integrated contactless interface frontend

- High RF output power frontend IC for transfer speed up to 848 kbit/s
- NFC IP1 and NFC IP2 support
- Full NFC tag support (type 1, type 2, type 3, type 4A and type 4B)
- P2P active and passive, target and initiator
- Card emulation ISO14443 type A
- ISO/IEC 14443 type A and type B
- MIFARE classic card
- ISO/IEC 15693, and ISO/IEC 18000-3 mode 3
- Low power card detection
- Dynamic Power Control (DPC) support
- Compliance with EMV contactless protocol specification
- Compliance with NFC standards

2.3 Cortex-M0 microcontroller

- Processor core

- ARM Cortex: 32-bit M0 processor
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Non-maskable interrupt
- 24-bit system tick timer
- Running frequency of up to 20 MHz
- Clock management to enable low power consumption

- Memory
  - Flash: 160 kB
  - SRAM: 12 kB
  - EEPROM: 4 kB
  - 40 kB boot ROM included, including USB mass storage primary bootloader for code download
- Debug option
  - Serial Wire Debug (SWD) interface
- Peripherals
  - *Host interface:*
  - USB 2.0 full speed with USB 3.0 hub connection capability
  - HSUART for serial communication, supporting standards speeds from 9600 baud to 115200 baud, and faster speed up to 1.288 Mbit/s
  - SPI with half duplex and full duplex capability with speeds up to 7 Mbit/s
  - I^2C supporting standard mode, fast mode and high-speed mode with multiple address support
  - *Master interface:*
  - SPI with half duplex capability from 1 Mbit/s to 6.78 Mbit/s
  - I^2C supporting standard mode, fast mode, fast mode plus and clock stretching
- Up to 21 General-Purpose I/O (GPIO) with configurable pull-up/pull-down resistors
- GPIO1 to GPIO12 can be used as edge and level sensitive interrupt sources
- Power
  - Two reduced power modes: standby mode and hard power-down mode
  - Supports suspend mode for USB host interface
  - Processor wake-up from hard power-down mode, standby mode, suspend mode via host interface, contact card interface, GPIOs, RF field detection
  - Integrated PMU to adjust internal regulators automatically, to minimize the power consumption during all possible power modes
  - Power-on reset
  - RF supply: external, or using an integrated LDO (TX LDO, configurable with 3 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V)
  - Pad voltage supply: external 3.3 V or 1.8 V, or using an integrated LDO (3.3 V supply)
  - Integrated contact interface voltage regulation for 1.8 V, 3 V, and 5 V card supply, including a DC-to-DC converter for supporting class A and class B cards
- Timers
  - Four general-purpose timers
  - Programmable WatchDog Timer (WDT)
- CRC coprocessor

- Random number generator
- Clocks
  - Crystal oscillator at 27.12 MHz
  - Dedicated PLL at 48 MHz for the USB
  - Integrated HFO 20 MHz and LFO 365 kHz
- General
  - HVQFN64 package
  - Temperature range: −40 °C to +85 °C

3. Applications

- Physical access control
- Gaming
- USB NFC reader, including dual interface smart card readers
- Home banking, payment readers EMVCo compliant
- High integration devices
- NFC applications

4. Quick reference data

Table 1. Quick reference data

Operating range: −40 °C to +85 °C unless specified; contact interface: $V_{DDP(VBUSP)} = V_{DDP(VBUS)}$; contactless interface: internal LDO not used

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS	card emulation, passive target (PLM)	2.3	-	5.5	V
		all RF modes; class B and class C contact interface support	2.7	-	5.5	V
		all RF modes; class A, class B and class C contact interface support	3	-	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	1.8 V	1.65	1.8	1.95	V
		3.3 V	3	3.3	3.6	V
$I_{DDP(VBUS)}$	power supply current on pin VBUS	in hard power-down mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; RST_N = 0	-	12	18	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 3.3 V; external PVDD LDO used	-	18	-	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; internal PVDD LDO used	-	55	-	µA
		suspend mode, USB interface; $V_{DDP(VBUS)}$ = 5.5 V; external PVDD supply; T = 25 °C	-	120	250	µA

Table 1. Quick reference data *...continued*

Operating range: −40 °C to +85 °C unless specified; contact interface: $V_{DDP(VBUSP)} = V_{DDP(VBUS)}$; contactless interface: internal LDO not used

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(TVDD)}$	TVDD supply current	on pin TVDD_IN; maximum supported current by the contactless interface	-	-	250	mA
V_{CC}	supply voltage	contact card				
		class A; I_{CC} < 60 mA	4.75	5	5.25	V
		class B; I_{CC} < 50 mA	2.85	3	3.15	V
		class C; I_{CC} < 30 mA	1.71	1.8	1.89	V
I_{CC}	supply current	contact card				
		class A cards	-	-	60	mA
		class B cards	-	-	55	mA
		class C cards	-	-	35	mA
P_{max}	maximum power dissipation		-	-	1050	mW
T_{amb}	ambient temperature	JEDEC PCB	−40	-	+85	°C

5. Ordering information

The PN7462 family includes the following products:

PN7462AU: Full feature set and memory available

PN7362AU: Full memory available, no contact interface

PN7360AU: Memory limited to 80 kB, and no contact interface.

The table below lists the ordering information for these three products.

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7462AUHN	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7362AUHN	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7360AUHN	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4

6. Block diagram

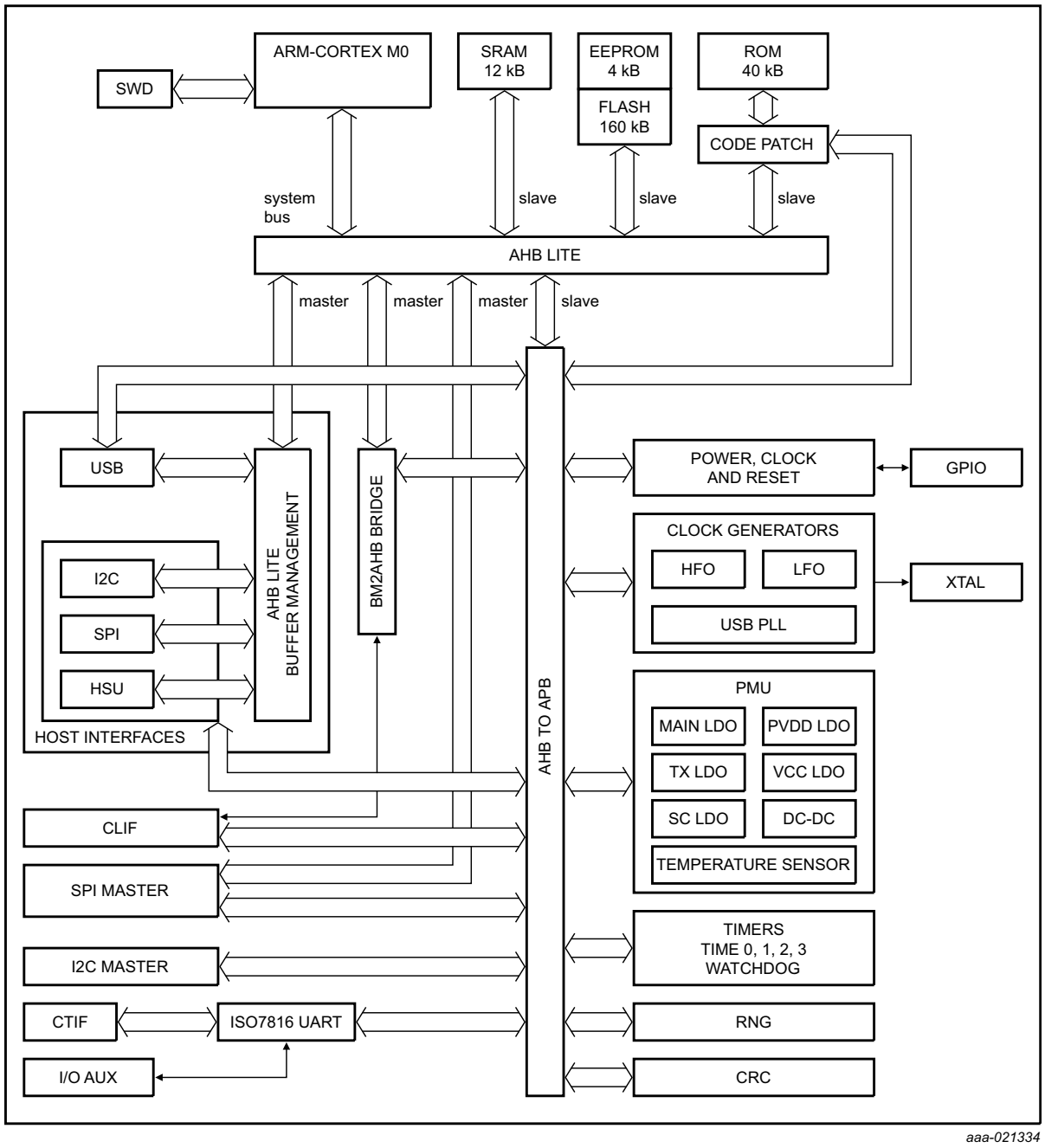
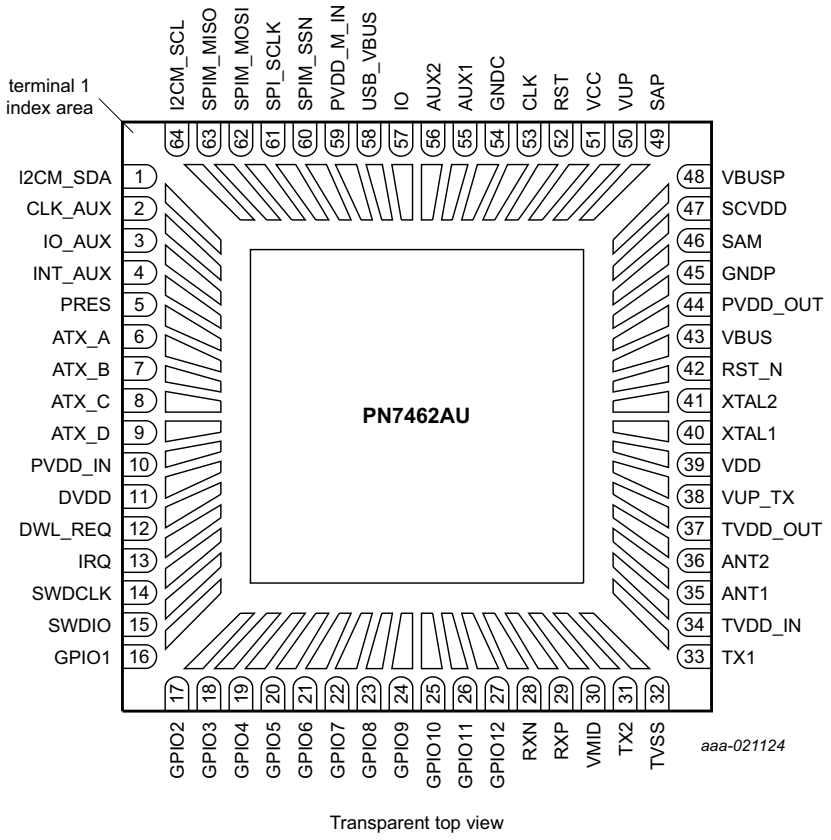


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
I2CM_SDA	1	I^2C-bus serial data I/O master/GPIO13
CLK_AUX	2	auxiliary card contact clock/GPIO14
IO_AUX	3	auxiliary card contact I/O/GPIO15
INT_AUX	4	auxiliary card contact interrupt/GPIO16
PRES	5	card presence
ATX_A	6	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/HSUART RX
ATX_B	7	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX
ATX_C	8	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/HSUART RTS
ATX_D	9	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS
PVDD_IN	10	pad supply voltage input
DVDD	11	digital core logic supply voltage input

Table 3. Pin description *...continued*

Symbol	Pin	Description
DWL_REQ	12	entering in download mode
IRQ	13	interrupt request output
SWDCLK	14	SW serial debug line clock
SWDIO	15	SW serial debug line input/output
GPIO1	16	general-purpose I/O/SPI master select2 output
GPIO2	17	general-purpose I/O
GPIO3	18	general-purpose I/O
GPIO4	19	general-purpose I/O
GPIO5	20	general-purpose I/O
GPIO6	21	general-purpose I/O
GPIO7	22	general-purpose I/O
GPIO8	23	general-purpose I/O
GPIO9	24	general-purpose I/O
GPIO10	25	general-purpose I/O
GPIO11	26	general-purpose I/O
GPIO12	27	general-purpose I/O
RXN	28	receiver input
RXP	29	receiver input
VMID	30	receiver reference voltage input
TX2	31	antenna driver output
TVSS	32	ground for antenna power supply
TX1	33	antenna driver output
TVDD_IN	34	antenna driver supply voltage input
ANT1	35	antenna connection for load modulation in card emulation and P2P passive target modes
ANT2	36	antenna connection for load modulation in card emulation and P2P passive target modes
TVDD_OUT	37	antenna driver supply, output of TX_LDO
VUP_TX	38	supply of the contactless TX_LDO
VDD	39	1.8 V regulator output for digital blocks
XTAL1	40	27.12 MHz clock input for crystal
XTAL2	41	27.12 MHz clock input for crystal
RST_N	42	reset pin
VBUS	43	main supply voltage input of microcontroller
PVDD_OUT	44	output of PVDD_LDO for pad voltage supply
GNDP	45	ground for the contact interface
SAM	46	DC-to-DC converter connection
SCVDD	47	input LDO for DC-to-DC converter
VBUSP	48	main supply for the contact interface
SAP	49	DC-to-DC converter connection
VUP	50	reserved; connected to GND through a decoupling capacitance
VCC	51	card supply output of contact interface
RST	52	reset pin of contact interface

Table 3. Pin description *...continued*

Symbol	Pin	Description
CLK	53	clock pin of contact interface
GNDC	54	ground pin of contact interface
AUX1	55	C4 card I/O pin of contact interface
AUX2	56	C8 card I/O pin of contact interface
IO	57	card I/O
USB_VBUS	58	used for USB VBUS detection
PVDD_M_IN	59	pad supply voltage input for master interfaces
SPIM_SSN	60	SPI master select 1 output/GPIO17
SPI_SCLK	61	SPI master clock output/GPIO18
SPIM_MOSI	62	SPI master data output/GPIO19
SPIM_MISO	63	SPI master data input/GPIO20
I2CM_SCL	64	I^2C-bus serial clock output master/GPIO21

8. Functional description

8.1 ARM Cortex-M0 microcontroller

The PN7462 is an ARM Cortex-M0-based 32-bit microcontroller, optimized for low-cost designs, high energy efficiency, and simple instruction set.

The CPU operates on an internal clock, which can be configured to provide frequencies such as 20 MHz, 10 MHz, and 5 MHz.

The peripheral complement of the PN7462 includes a 160 kB flash memory, a 12 kB SRAM, and a 4 kB EEPROM. It also includes one configurable host interface (fast-mode plus and high-speed I^2C, SPI, HSUART, and USB), two master interfaces (fast-mode plus I^2C, SPI), four timers, 12 general-purpose I/O pins, one ISO/IEC 7816 contact card interface, and one 13.56 MHz contactless interface.

8.2 Memories

8.2.1 On-chip flash programming memory

The PN7462 contains 160 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into two instances of 80 kB each, with each sector consisting of individual pages of 64 bytes.

8.2.1.1 Memory mapping

The flash memory mapping is described in Figure 3.

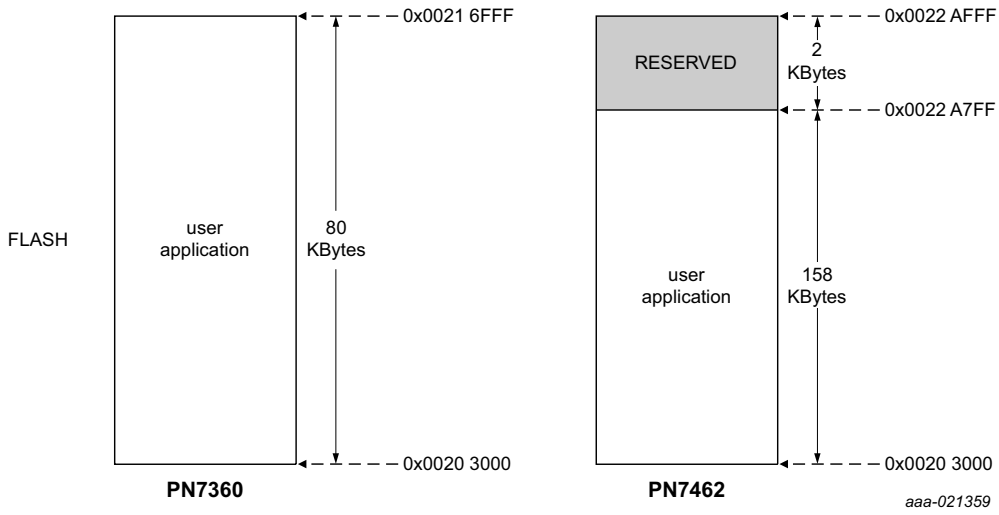


Fig 3. Flash memory mapping

8.2.2 EEPROM

The PN7462 embeds 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory.

The EEPROM can be programmed using In-System Programming (ISP).

8.2.2.1 Memory mapping

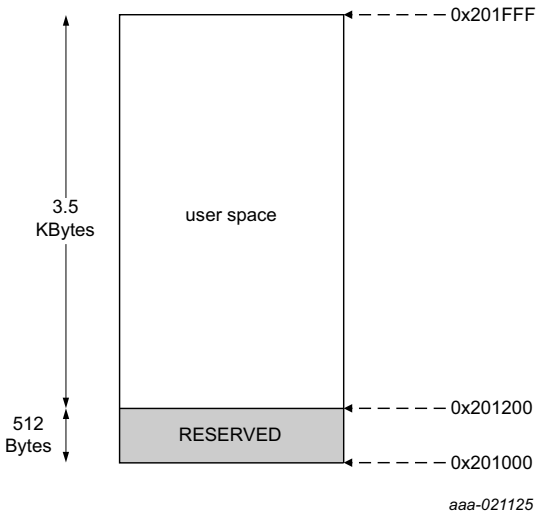


Fig 4. EEPROM memory mapping

8.2.3 SRAM

The PN7462 contains a total of 12 kB on-chip static RAM memory.

8.2.3.1 Memory mapping

The SRAM memory mapping is shown in Figure 5.

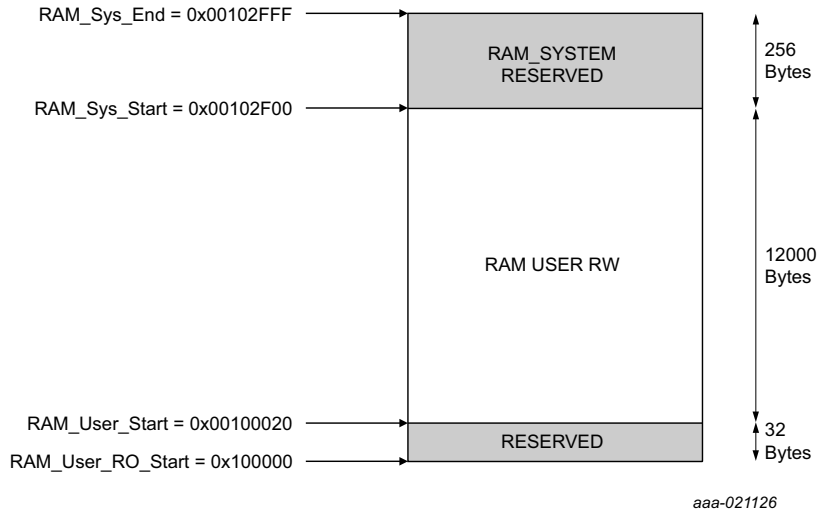


Fig 5. SRAM memory mapping

8.2.4 ROM

The PN7462 contains 40 kB of on-chip ROM memory. The on-chip ROM contains bootloader, USB mass storage primary download and the following Application Programming Interfaces (APIs):

- In-Application Programming (IAP) support for flash
- Lifecycle management of debug interface, code write protection of flash memory and USB mass storage primary download
- USB descriptor configuration
- Configuration of time-out and source of pad supply

8.2.5 Memory map

The PN7462 incorporates several distinct memory regions. Figure 6 shows the PN7462 memory map, from the user program perspective, following reset.

The APB peripheral area is 512 kB in size, and is divided to allow up to 32 peripherals. Only peripherals from 0 to 15 are accessible. Each peripheral is allocated 16 kB, which simplifies the address decoding for the peripherals. APB memory map is described in Figure 7.

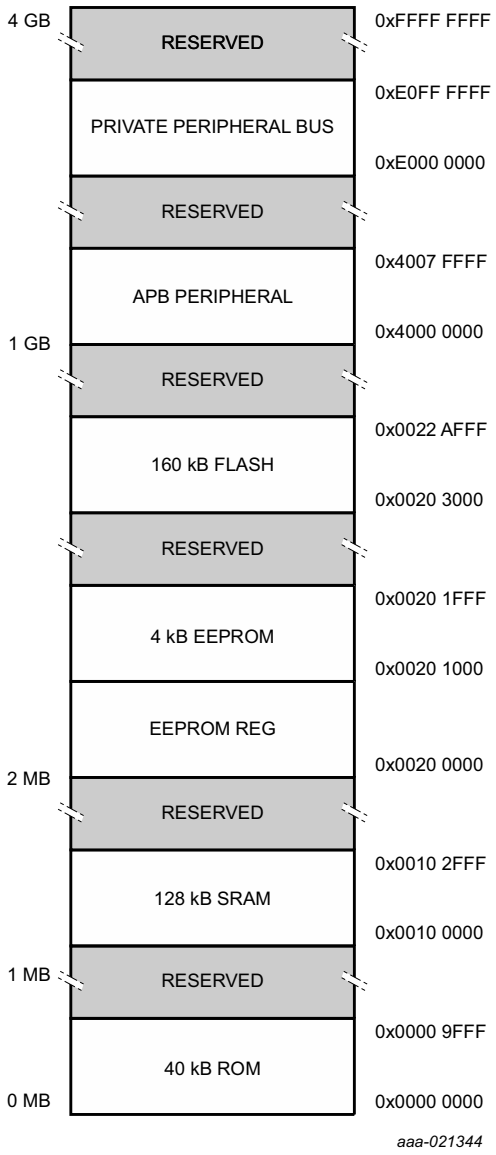


Fig 6. PN7462 memory map

APB ID	APB IF name	Connected IP	
16 to 31	Reserved		0x4004 8000
15	Reserved		0x4004 0000
14	Reserved		0x4003 C000
13	SPIMASTER_APB	SPI Master IF	0x4003 8000
12	I2CMASTER_APB	I2C Master IF	0x4003 4000
11	Reserved		0x4003 0000
10	USB_APB	HostIF (USB) IP	0x4002 C000
9	PCR_APB	PowerClockResetModule IP	0x4002 8000
8	HOST_APB	HostIF (I2C/SPI/HSU/BufMgt) IP	0x4002 4000
7	TIMERS_APB	Timer IP	0x4002 0000
6	RNG_APB	RNG IP	0x4001 C000
5	CTUART_APB	Contact UART IP	0x4001 8000
4	CLOCKGEN_APB	Clock Gen module	0x4001 4000
3	CRC_APB	CRC IP	0x4001 0000
2	PMU_APB	PMU modules	0x4000 C000
1	CL_APB	Contactless IP	0x4000 8000
0	Reserved		0x4000 4000
			0x4000 0000

aaa-021127

Fig 7. APB memory map

8.3 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 includes a Nested Vectored Interrupt Controller (NVIC). The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.3.1 NVIC features

- System exceptions and peripheral interrupts control
- Support 32 vectored interrupts
- Four interrupt priority levels with hardware priority level masking
- One Non-Maskable Interrupt (NMI) connected to the watchdog interrupt
- Software interrupt generation

8.3.2 Interrupt sources

The following table lists the interrupt sources available in the PN7462 microcontroller.

Table 4. Interrupt sources

EIRQ#	Source	Description
0	timer 0/1/2/3	general-purpose timer 0/1/2/3 interrupt
1	-	reserved
2	CLIF	contactless interface module interrupt
3	EECTRL	EEPROM controller
4	-	reserved
5	-	reserved
6	host IF	TX or RX buffer from I^2C, SPI, HSU, or USB module
7	contact IF	ISO7816 contact module interrupt

Table 4. Interrupt sources *…continued*

EIRQ#	Source	Description
8	-	reserved
9	PMU	power management unit (temperature sensor, over current, overload, and VBUS level)
10	SPI master	TX or RX buffer from SPI master module
11	I^2C master	TX or RX buffer from I^2C master module
12	PCR	high temperature from temperature sensor 0 and 1; interrupt to CPU from PCR to indicate wake-up from suspend mode; out of standby; out of suspend; event on GPIOs configured as inputs
13	PCR	interrupt common GPIO1 to GPIO12
14	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO1
15	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO2
16	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO3
17	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO4
18	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO5
19	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO6
20	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO7
21	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO8
22	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO9
23	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO10
24	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO11
25	PCR	interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO12
26	-	reserved
27	-	reserved
28	-	reserved
29	-	reserved
30	-	reserved
31	-	reserved
NMI[1]	WDT	watchdog interrupt is connected to the non-maskable interrupt pin

[1] The NMI is not available on an external pin.

8.4 GPIOs

The PN7462 has 12 general-purpose I/O (GPIO) with configurable pull-up and pull-down resistors, plus nine additional GPIOs multiplexed with SPI master, I^2C-bus master and AUX pins.

Pins can be dynamically configured as inputs or outputs. GPIO read/write are made by the FW using dedicated registers that allow reading, setting or clearing inputs. The value of the output register can be read back, as well as the current state of the input pins.

8.4.1 GPIO features

- Dynamic configuration as input or output
- 3.3 V and 1.8 V signaling
- Programmable weak pull-up and weak pull-down
- Independent interrupts for GPIO1 to GPIO12
- Interrupts: edge or level sensitive
- GPIO1 to GPIO12 can be programmed as wake-up sources
- Programmable spike filter (3 ns)
- Programmable slew rate (3 ns and 10 ns)
- Hysteresis receiver with disable option

8.4.2 GPIO configuration

The GPIO configuration is done through the PCR module (power, clock, and reset).

8.4.3 GPIO interrupts

GPIO1 to GPIO12 can be programmed to generate an interrupt on a level, a rising or falling edge or both.

8.5 CRC engine 16/32 bits

The PN7462 has a configurable 16/32-bit parallel CRC co-processor.

The 16-bit CRC is compliant to X.25 (CRC-CCITT, ISO/IEC 13239) standard with a generator polynome of:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

The 32-bit CRC is compliant to the ethernet/AAL5 (IEEE 802.3) standard with a generator polynome of:

$$g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

CRC calculation is performed in parallel, meaning that one CRC calculation is performed in one clock cycle. The standard CRC 32 polynome is compliant with FIPS140-2.

Note: No final XOR calculation is performed.

Following are the CRC engine features:

- Configurable CRC preset value
- Selectable LSB or MSB first

- CRC 32 calculation based on 32-bit, 16-bit, and 8-bit words
- CRC16 calculation based on 32-bit, 16-bit, and 8-bit words
- Supports bit order reverse

8.6 Random Number Generator (RNG)

The PN7462 integrates a random number generator. It consists of an analog True Random Number Generator (TRNG), and a digital Pseudo Random Number Generator (PRNG). The TRNG is used for loading a new seed in the PRNG.

The random number generator features:

- 8-bit random number
- Compliant with FIPS 140-2
- Compliant with BSI AIS20 and SP800-22

8.7 Master interfaces

8.7.1 I²C master interface

The PN7462 contains one I²C master and one I²C slave controller. This chapter describes the master interface. For more information on the I²C slave controller, refer to Section 8.8.2.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). Each device has a unique address. The device can operate either as a receive-only device (such as LCD driver) or a transmitter with the capability to both receive and send information (such as memory).

8.7.1.1 I²C features

The I²C master interface supports the following features:

- Standard I²C compliant bus interface with open-drain pins
- Standard-mode, fast mode and fast mode plus (up to 1 Mbit/s).
- Support I²C master mode only.
- Programmable clocks allowing versatile rate control.
- Clock stretching
- 7-bit and 10-bit I²C slave addressing
- LDM/STM instruction support
- Maximum data frame size up to 1024 bytes

8.7.2 SPI interface

The PN7462 contains one SPI master controller and one SPI slave controller.

The SPI master controller transmits the data from the system RAM to the SPI external slaves. Similarly, it receives data from the SPI external slaves and stores them into the system RAM. It can compute a CRC for received frames and automatically compute and append CRC for outgoing frames (optional feature).

8.7.2.1 SPI features

The SPI master interface provides the following features:

- SPI master interface: synchronous, half-duplex
- Supports Motorola SPI frame formats only (SPI block guide V04.0114 (Freescale) specification)
- Maximum SPI data rate of 6.78 Mbit/s
- Multiple data rates such as 1, 1.51, 2.09, 2.47, 3.01, 4.52, 5.42 and 6.78 Mbit/s
- Up to two slave select with selectable polarity
- Programmable clock polarity and phase
- Supports 8-bit transfers only
- Maximum frame size: 511 data bytes payload + 1 CRC byte
- Optional 1 byte CRC calculation on all data of TX and RX buffer
- AHB master interface for data transfer

8.8 Host interfaces

The PN7462 embeds four different interfaces for host connection: USB, HSUART, I^2C, and SPI.

The four interfaces share the buffer manager and the pins; see Table 5.

Table 5. Pin description for host interface

Name	SPI	I^2C	USB	HSU
ATX_A	NSS_S	SCL_S	-	HSU_RX
ATX_B	MOSI_S	SDA_S	-	HSU_TX
ATX_C	MISO_S	I^2C_ADR0	DP	HSU_RTS_N
ATX_D	SCK_S	I^2C_ADR1	DM	HSU_CTS_N

The interface selection is done by configuring the Power Clock Reset (PCR) registers.

Note: The host interface pins should not be kept floating.

8.8.1 High-speed UART

The PN7462 has a high-speed UART which can operate in slave mode only.

Following are the HSUART features:

- Standard bit-rates are 9600, 19200, 38400, 57600, 115200, and up to 1.288 Mbit/s
- Supports full duplex communication
- Supports only one operational mode: start bit, 8 data bits (LSB), and stop bits
- The number of “stop bits” programmable for RX and TX is 1 stop bit or 2 stop bits
- Configurable length of EOF (1-bit to 122-bits)

Table 6. HSUART baudrates

Bit rate (kBd)
9.6
19.2
38.4
57.6
115.2
230.4
460.8
921.6
1288 K

8.8.2 I²C host interface controller

The PN7462 contains one I²C master and one I²C slave controller. This section describes the slave interface used for host communication. For more information on the I²C master controller, refer to Section 8.7.1.

The I²C-bus is bidirectional and uses only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). I²C standard mode (100 kbit/s), fast mode (400 kbit/s and up to 1 Mbit/s), and high-speed mode (3.4 Mbit/s) are supported.

8.8.2.1 I²C host interface features

The PN7462 I²C slave interface supports the following features:

- Support slave I²C bus
- Standard mode, fast mode (extended to 1 Mbit/s support), and high-speed modes
- Supports 7-bit addressing mode only
- Selection of the I²C address done by two pins
  - It supports multiple addresses
  - The upper bits of the I²C slave address are hard-coded. The value corresponds to the NXP identifier for I²C blocks. The value is 01010XXb.
- General call (software reset only)
- Software reset (in standard mode and fast mode only)

Table 7. I²C interface addressing

I²C_ADR1	I²C_ADR0	I²C address (R/W = 0, write)	I²C address (R/W = 0, read)
0	0	0 × 28	0 × 28
0	1	0 × 29	0 × 29
1	0	0 × 2A	0 × 2A
1	1	0 × 2B	0 × 2B

8.8.3 SPI host/Slave interface

The PN7462 host interface can be used as SPI slave interface.

The SPI slave controller operates on a four wire SSI: Master In Slave Out (MISO), Master Out Slave In (MOSI), Serial ClocK (SCK), and Not Slave Select (NSS). The SPI slave select polarity is fixed to positive polarity.

8.8.3.1 SPI host interface features

The SPI host/slave interface has the following features:

- SPI speeds up to 7 Mbit/s
- Slave operation only
- 8-bit data format only
- Programmable clock polarity and phase
- SPI slave select polarity selection fixed to positive polarity
- Half-duplex in HDLL mode
- Full-duplex in native mode

If no data is available, the MISO line is kept idle by making all the bits high (0xFF). Toggling the NSS line indicates a new frame.

Note: Programmable echo-back operation is not supported.

Table 8. SPI configuration

connection
CPHA switch: Clock phase: Defines the sampling edge of MOSI data • CPHA = 1: Data are sampled on MOSI on the even clock edges of SCK, after NSS goes low • CPHA = 0: Data are sampled on MOSI on the odd clock edges of SCK, after NSS goes low
CPOL switch: Clock polarity • IFSEL1 = 0: The clock is idle low, and the first valid edge of SCK is a rising one • IFSEL1 = 0: The clock is idle high, and the first valid edge of SCK is a falling one

8.8.4 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and up to 127 peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of devices. The host controller initiates all transactions. The PN7462 USB interface consists of a full-speed device controller with on-chip PHY (physical layer) for device functions.

8.8.4.1 Full speed USB device controller

The PN7462 embeds a USB device peripheral, compliant with USB 2.0 specification, full speed. It is interoperable with USB 3.0 host devices.

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer.

The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

Following are the USB interface features:

- Fully compliant with USB 2.0 specification (full speed)
- Dedicated USB PLL available
- Supports 14 physical (7 logical) endpoints including one control endpoint
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types
- Single or double buffering allowed
- Support wake-up from suspend mode on USB activity and remote wake-up
- Soft-connect supported

8.9 Contact interface

The PN7462 integrates an ISO/IEC 7816 interface to enable the communication with a contact smart card. It does not require addition of an external contact frontend for reading payment cards, SAM for secure applications, etc. It offers a high level of security for the card by performing current limitation, short-circuit detection, ESD protection as well as supply supervision.

PN7462 also offers the possibility to extend the number of contact interfaces available. It uses an I/O auxiliary interface to connect a slot extension (TDA8035 - 1 slot, TDA8020 - 2 slots, and TDA8026 - 5 slots).

- Class A (5 V), class B (3 V), and class C (1.8 V) smart card supply
- Protection of smart card
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7, and C8)
- Compliant with ISO/IEC 7816 and EMVCo 4.3 standards

8.9.1 Contact interface features and benefits

- Protection of the smart card
  - Thermal and current limitation in the event of short-circuit (pins I/O, V_{CC})
  - V_{CC} regulation: 5 V, 3 V, and 1.8 V
  - Automatic deactivation initiated by hardware in the event of a short-circuit, card take-off, overheating, falling of PN7462 supply
  - Enhanced card-side ElectroStatic Discharge (ESD) protection of greater than 8 kV
- Support of class A, class B, and class C contact smart cards
- DC-to-DC converter for V_{CC} generation to enable support of class A and class B cards with low input voltages
- Built-in debouncing on card presence contact
- Compliant with ISO/IEC 7816 and EMVCo 4.3 standards
- Card clock generation up to 13.56 MHz using external crystal oscillator (27.12 MHz); provides synchronous frequency changes of f_{XTAL} / 2, f_{XTAL} / 3, f_{XTAL} / 4, f_{XTAL} / 5, f_{XTAL} / 6, f_{XTAL} / 8, and f_{XTAL} / 16

- Specific ISO/IEC UART with APB access for automatic convention processing, variable baudrate through frequency or division ratio programming, error management at character level for T = 0 and extra guard time register
  - FIFO 1 character to 32 characters in both reception and transmission mode
  - Parity error counter in reception mode and transmission mode with automatic retransmission
  - Cards clock stop (at HIGH or LOW level)
  - Automatic activation and deactivation sequence through a sequencer
  - Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO/IEC 7816 and EMV
  - Versatile 24-bit time-out counter for Answer To Reset (ATR) and waiting times processing
  - Specific Elementary Time Unit (ETU) counter for Block Guard Time (BGT); 22 ETU in T = 1 and 16 ETU in T = 0
  - Supports synchronous cards

8.9.2 Voltage supervisor

The PN7462 integrates a voltage monitor to ensure that sufficient voltage is available for the contact interface; see Section 8.15.4 and Section 9.1.3.

In order to provide the right voltage needed for the various ISO/IEC 7816 contact card classes (A, B, or C), the following voltages are needed:

- $V_{DDP(VBUSP)}$ > 2.7 V for support of class B and class C contact cards
- $V_{DDP(VBUSP)}$ > 3 V for support of class A contact cards
- **Remark:** To support class A cards, DC-to-DC converter is used in doubler mode. To support class B cards with $V_{DDP(VBUSP)}$ < 3.9 V, DC-to-DC converter is used in doubler mode. To support class B cards with $V_{DDP(VBUSP)}$ > 3.9 V, DC-to-DC converter is used in follower mode.

Figure 8 shows the classes that are supported, depending on $V_{DDP(VBUSP)}$.

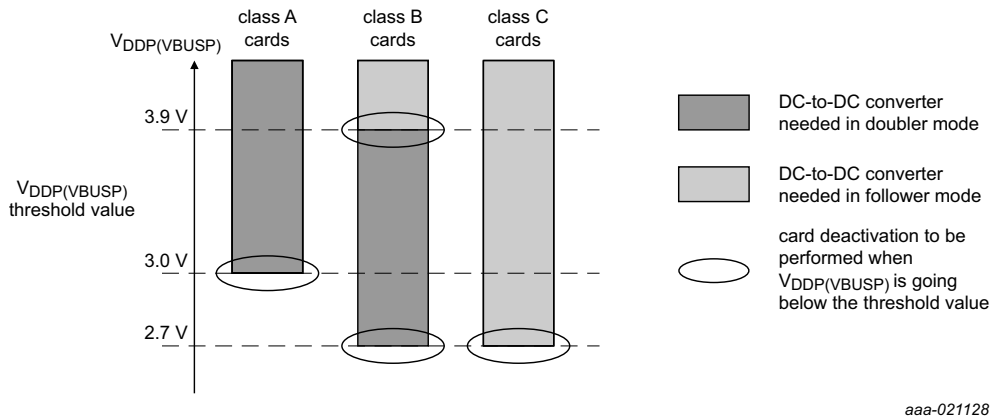


Fig 8. $V_{DDP(VBUS)}$, supported contact cards classes, and card deactivation

When the $V_{DDP(VBUSP)}$ is going below the threshold value, in the one of the conditions indicated below, a card deactivation is performed:

- Class A card activated, and $V_{DDP(VBUSP)}$ going below 3 V
- Class B card activated, and $V_{DDP(VBUSP)}$ going below 3.9 V (DC-to-DC converter in follower mode)
- Class B card activated, and $V_{DDP(VBUSP)}$ going below 2.7 V (DC-to-DC converter in doubler mode)
- Class C card activated, and $V_{DDP(VBUSP)}$ going below 2.7 V

The VBUSP voltage monitor can be configured so that an automatic “card deactivation” sequence is performed automatically when $V_{DDP(VBUSP)}$ is going below the threshold value.

8.9.3 Clock circuitry

The card clock is generated from the crystal oscillator, connected on the pin XTAL1 and XTAL2.

The card frequency is configured through the contact interface registers. The following value can be chosen: f_{XTAL} / 2, f_{XTAL} / 3, f_{XTAL} / 4, f_{XTAL} / 5, f_{XTAL} / 6, f_{XTAL} / 8, and f_{XTAL} / 16.

It is possible to put the card clock to a logical level 0 or 1 (clock stop feature).

The duty cycle on the pin CLK is between 45 % and 55 %, for all the available clock dividers.

8.9.4 I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

I/O is referenced to V_{CC}. To enter in the idle state, the I/O line is pulled HIGH via a 10 kΩ resistor (I/O to V_{CC}).

The active pull-up feature ensures fast LOW to HIGH transitions. At the end of the active pull-up pulse, the output voltage depends on the internal pull-up resistor and the load current.

The maximum frequency on these lines is 1.5 MHz.

8.9.5 VCC regulator

VCC regulator delivers up to 60 mA for class A cards (0 V to 5 V). It also delivers up to 55 mA for class B cards (0 V to 3 V) and up to 35 mA for class C cards (from 0 V to 1.8 V).

The VCC has an internal overload detection at approximately 110 mA for class A and B, and 90 mA for class C.

This detection is internally filtered, allowing the card to draw spurious current pulses as defined in EMVCo specification, without causing a deactivation. The average current value must remain below the maximum.

8.9.6 Activation sequence

The presence of a contact card is indicated to PN7462 through PRESN signal. If all supply conditions are met, the PN7462 may start an activation sequence. Figure 9 shows the activation sequence.

The sequencer clock is based on the crystal oscillator: $f_{seq} = f_{XTAL}/10$. When the contact interface is active, the period for activation phases is: $T = 64/f_{seq} = 23.6\ \mu s$.

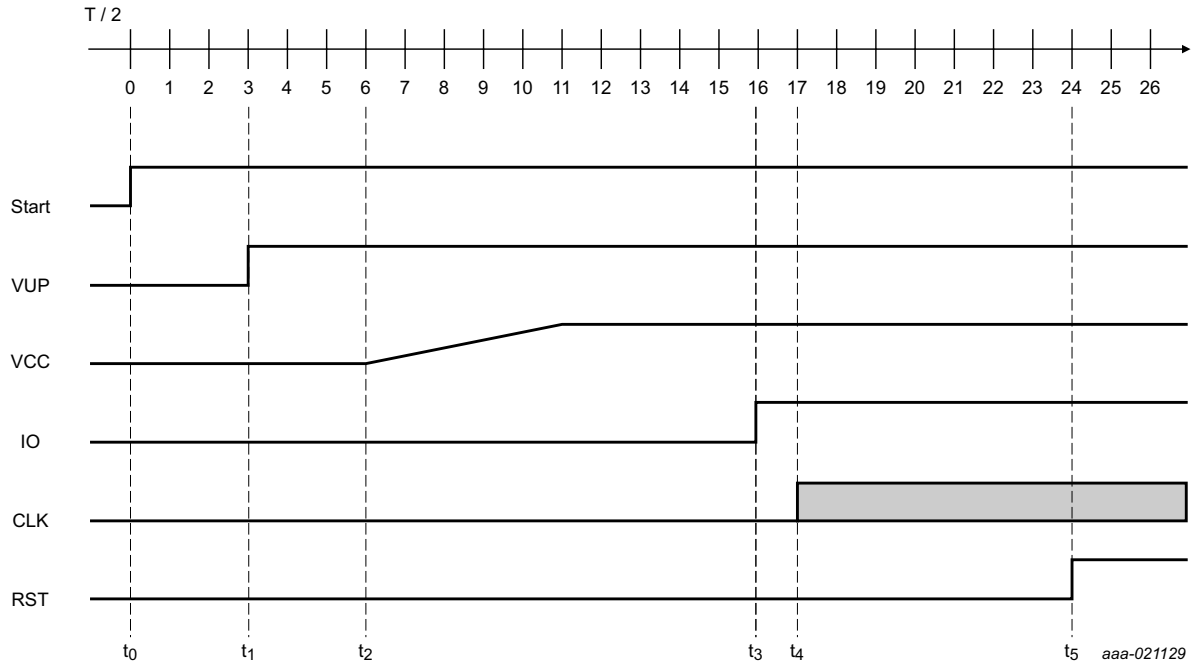


Fig 9. Contact interface - activation sequence

Once the activation sequence is triggered, the following sequence takes place:

- Contact LDOs and DC-to-DC converter (when relevant) starts at t_1
- VCC starts rising from 0 to the required voltage (5 V, 3 V, and 1.8 V) at t_2
- IO rises to VCC at t_3
- CLK starts at t_4
- RST pin is enabled at t_5

8.9.7 Deactivation sequence

When triggered by the PN7462, the deactivation following sequence takes place:

- Card reset (pin RST) status goes LOW
- Clock (CLK) stopped at LOW level
- Pin IO falls to 0 V
- VCC falls to 0 V

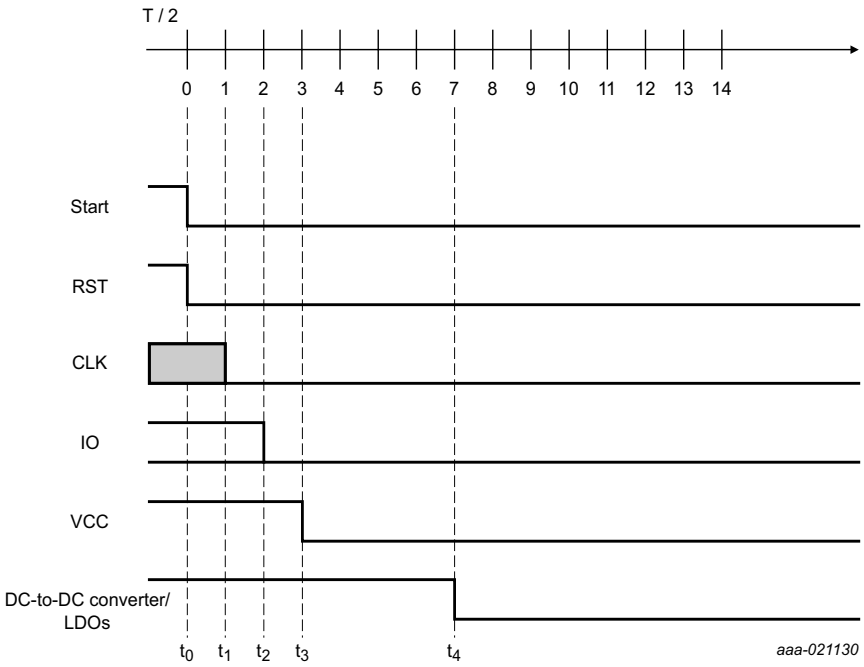


Fig 10. Deactivation sequence for contact interface

The deactivation sequence is performed in the following cases:

- Removal of card; generated automatically by the PN7462
- Overcurrent detection on pin VCC; generated automatically by the PN7462
- Overcurrent detection on pin IO; generated automatically by the PN7462
- Detection for overheating; generated automatically by the PN7462
- Pin VBUSP going below relevant voltage threshold (optional); part of the pin VBUSP monitor
- Reset request through software

8.9.8 I/O auxiliary - connecting TDA slot extender

To address applications where multiple ISO/IEC 7816 interfaces are needed, the PN7462 integrates the possibility to connect contact slot extenders like TDA8026, TDA8020 or TDA8035.

The following pins are available:

- INT_AUX
- CLK_AUX
- IO_AUX

For more details about the connection, refer to the slot extender documentation.

8.10 Contactless interface - 13.56 MHz

The PN7462 embeds a high power 13.56 MHz RF frontend. The RF interface implements the RF functionality like antenna driving, the receiver circuitry, and all the low-level functionalities. It helps to realize an NFC forum or an EMVCo compliant reader.

The PN7462 allows different voltages for the RF drivers. For information related to the RF interface supply, refer Section 8.15.

The PN7462 uses an external oscillator, at 27.12 MHz. It is a clock source for generating RF field and its internal operation.

Key features of the RF interface are:

- ISO/IEC 14443 type A & B compliant
- MIFARE functionality, including MIFARE classic encryption in read/write mode
- ISO/IEC 15693 compliant
- NFC Forum - NFCIP-1 & NFC IP2 compliant
  - P2P, active and passive mode
  - reading of NFC forum tag types 1, 2, 3, 4, and 5
- FeliCa
- ISO/IEC 18000-3 mode 3
- EMVCo contactless 2.3.1 and 2.5[1]
  - RF level can be achieved without the need of booster circuitry (for some antenna topologies the EMV RF-level compliance might physically not be achievable)
- Card mode - enabling the emulation of an ISO/IEC 14443 type A card
  - Supports Passive Load Modulation (PLM) and Active Load Modulation (ALM)
- Low Power Card Detection (LPCD)
- Adjustable RX-voltage level

A minimum voltage of 2.3 V helps to use card emulation, and P2P passive target functionality in passive load modulation.

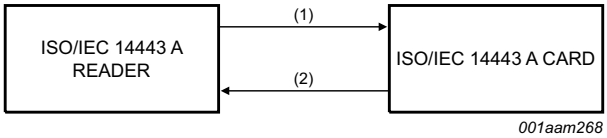
A voltage above 2.7 V enables all contactless functionalities.

8.10.1 RF functionality

8.10.1.1 ISO/IEC14443 A/MIFARE functionality

The physical level of the communication is shown in Figure 11.

1. EMVCo contactless 2.5 compliance pending



(1) Reader to Card: 100 % ASK; modified miller coded; transfer speed 106 kbit/s to 848 kbit/s

(2) Card to Reader: Subcarrier load modulation Manchester coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 11. ISO/IEC 14443 A/MIFARE read/write mode communication diagram

The physical parameters are described in Table 9.

Table 9. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader to card (send data from the PN7462 to a card) f_c = 13.56 MHz	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified miller encoding	modified miller encoding	modified miller encoding	modified miller encoding
	bit rate (kbit/s)	f_c / 128	f_c / 64	f_c / 32	f_c / 16
card to reader (PN7462 receives data from a card)	card side modulation	sub carrier load modulation	sub carrier load modulation	sub carrier load modulation	sub carrier load modulation
	subcarrier frequency	f_c / 16	f_c / 16	f_c / 16	f_c / 16
	bit encoding	manchester encoding	BPSK	BPSK	BPSK

Figure 12 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

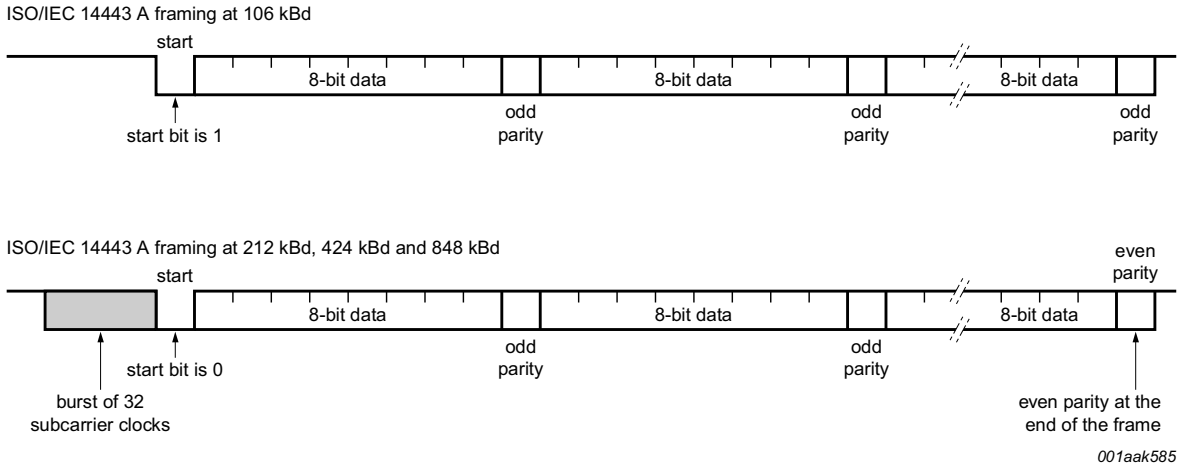
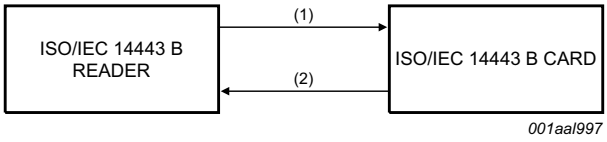


Fig 12. Data coding and framing according to ISO/IEC 14443 A card response

The internal CRC coprocessor calculates the CRC value based on the selected protocol. In card mode for higher baudrates, the parity is automatically inverted as end of communication indicator.

8.10.1.2 ISO/IEC14443 B functionality

The physical level of the communication is shown in Figure 13.



(1) Reader to Card: NRZ; transfer speed 106 kbit/s to 848 kbit/s

(2) Card to reader: Subcarrier load modulation manchester coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 13. ISO/IEC 14443 B read/write mode communication diagram

The physical parameters are described in Table 10.

Table 10. Communication overview for ISO/IEC 14443 B reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
reader to card (send data from the PN7462 to a card) f_c = 13.56 MHz	reader side modulation	10 % ASK	10 % ASK	10 % ASK	10 % ASK
	bit encoding	NRZ	NRZ	NRZ	NRZ
	bit rate [kbit/s]	128/f_c	64/f_c	32/f_c	16/f_c
card to reader (PN7462 receives data from a card)	card side modulation	sub carrier load modulation	sub carrier load modulation	sub carrier load modulation	sub carrier load modulation
	sub carrier frequency	f_c / 16	f_c / 16	f_c / 16	f_c / 16
	bit encoding	BPSK	BPSK	BPSK	BPSK

8.10.1.3 FeliCa functionality

The FeliCa mode is a general reader/writer to card communication scheme, according to the FeliCa specification. The communication on a physical level is shown in Figure 14.

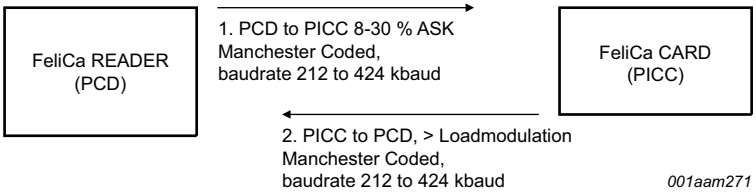


Fig 14. FeliCa read/write communication diagram

The physical parameters are described in Table 11.

Table 11. Communication overview for FeliCa reader/writer

Communication direction	Signal type	Transfer speed FeliCa	FeliCa higher transfer speeds
		212 kbit/s	**424 kbit/s**
reader to card (send data from the PN7462 to a card) f_c = 13.56 MHz	reader side modulation	8 % to 30 % ASK	8 % to 30 % ASK
	bit encoding	manchester encoding	manchester encoding
	bit rate	f_c / 64	f_c / 32
card to reader (PN7462 receives data from a card)	card side modulation	load modulation	load modulation
	bit encoding	manchester encoding	manchester encoding

Note: The PN7462 does not manage FeliCa security aspects.

PN7462 supports FeliCa multiple reception cycles.

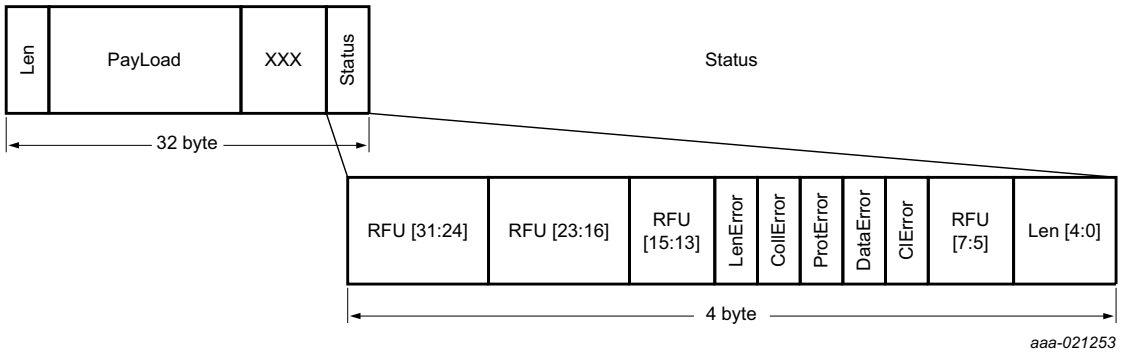
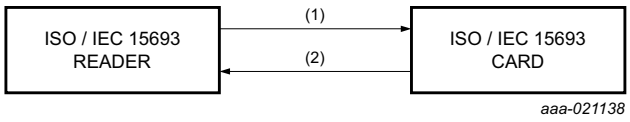


Fig 15. Multiple reception cycles - data format

8.10.1.4 ISO/IEC 15693 functionality

The physical level of the communication is shown in Figure 16.



(1) Reader to Card: 1/256 and 1/4 encoding

(2) Card to Reader: Manchester coding

Fig 16. ISO/IEC 15693 read/write mode communication diagram

The physical parameters are described in Table 12.

Table 12. Communication overview for ISO/IEC 15693 reader/writer reader to label

Communication direction	Signal type	Transfer speed	
		f_c / 8192 kbit/s	**f_c / 512 kbit/s**
reader to label (send data from the PN7462 to a card)	reader side modulation	10 % to 30 % ASK or 100 % ASK	10 % to 30 % ASK or 90 % to 100 % ASK
	bit encoding	1/256	1/4
	bit length	4.833 µs	302.08 µs

Table 13. Communication overview for ISO/IEC 15693 reader/writer label to reader

Communication direction	Signal type	Transfer speed			
		6.62 kbit/s	13.24 kbit/s[1]	26.48 kbit/s	52.96 kbit/s
label to reader (PN7462 receives data from a card) f_c = 13.56 MHz	card side modulation	not supported	not supported	single (dual) sub carrier load modulation ASK	single sub carrier load modulation ASK
	bit length (µs)	-	-	37.76	18.88
	bit encoding	-	-	manchester coding	manchester coding
	subcarrier frequency (MHz)	-	-	f_c / 32	f_c / 32

[1] Fast inventory (page) read command only (ICODE proprietary command).

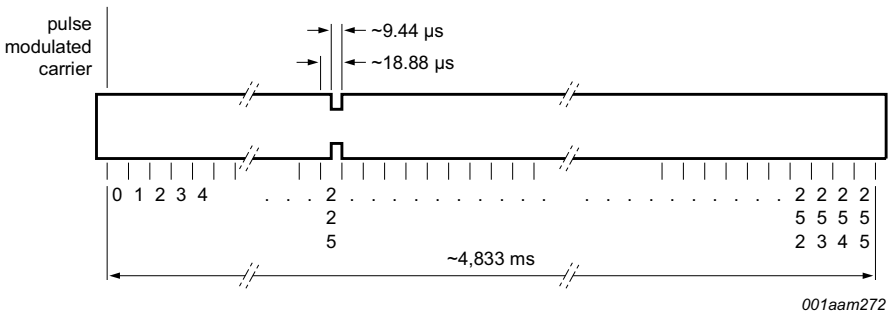


Fig 17. Data coding according to ISO/IEC 15693 standard mode reader to label

8.10.1.5 ISO/IEC18000-3 mode 3 functionality

The ISO/IEC 18000-3 mode 3 is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18000-3 standard.

PN7462 supports the following features:

- TARI = 9.44 µs or 18.88 µs
- Downlink: Four subcarrier pulse manchester and two subcarrier pulse manchester
- Subcarrier: 423 kHz (f_c / 32) with DR = 0 and 847 kHz (f_c / 16) with DR = 1

8.10.1.6 NFCIP-1 modes

The NFCIP-1 communication differentiates between an active and a passive communication mode.

- In active communication mode, both initiator and target use their own RF field to transmit data
- In passive communication mode, the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field
- The initiator generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- In passive communication mode, the target responds to initiator command in load modulation scheme. In active communication mode, it uses a self-generated and self-modulated RF field.

PN7462 supports NFCIP-1 standard. PN7462 supports active and passive communication mode at transfer speeds of 106 kbit/s, 212 kbit/s, and 424 kbit/s, as defined in the NFCIP-1 standard.

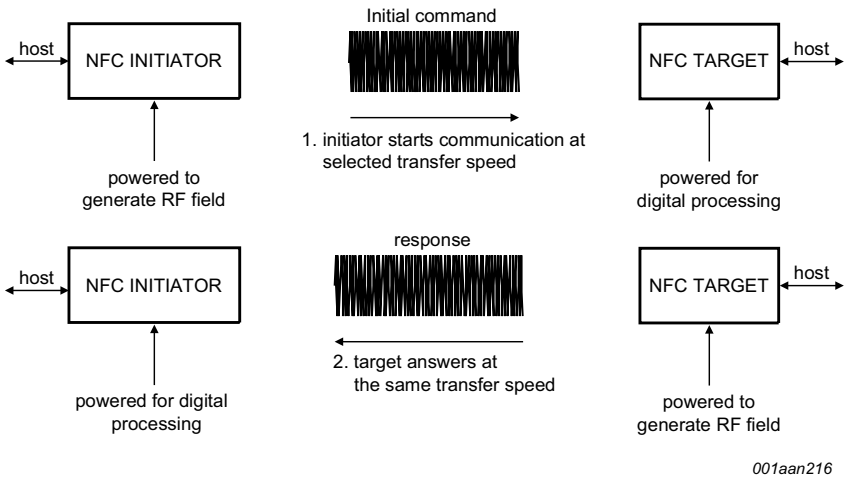


Fig 18. Active communication mode

Table 14. Communication overview for active communication mode

Communication direction	Transfer speed		
	106 kbit/s	212 kbit/s	424 kbit/s
initiator to target	according to ISO/IEC 14443 A 100 % ASK, modified miller coded	according to FeliCa, 8-30 % ASK manchester coded	according to FeliCa, 8-30 % ASK manchester coded
target to initiator			

Note: Transfer speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

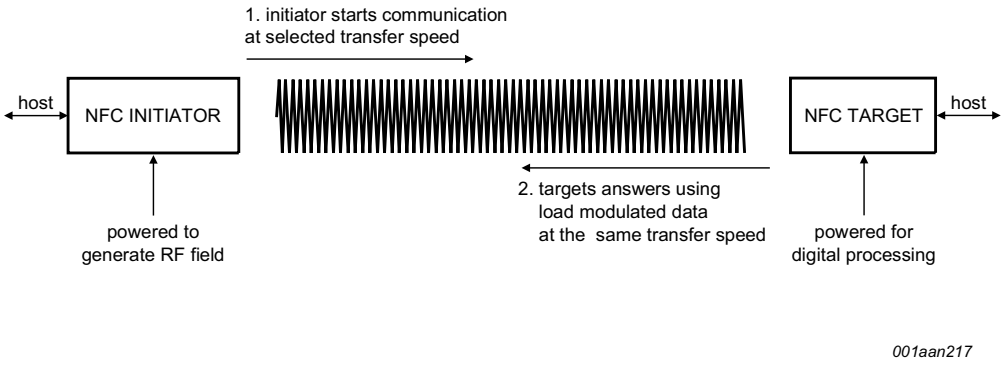


Fig 19. Passive communication mode

Table 15. Communication overview for passive communication mode

Communication direction	Transfer speed		
	106 kbit/s	212 kbit/s	424 kbit/s
initiator to target	according to ISO/IEC 14443 A 100 % ASK, modified miller coded	according to FeliCa, 8-30 % ASK manchester coded	according to FeliCa, 8-30 % ASK manchester coded
target to initiator	according to ISO/IEC 14443 A @106 kB modified miller coded	according to FeliCa, > 12 % ASK manchester coded	according to FeliCa, > 12 % ASK manchester coded

The NFCIP-1 protocol is managed in the PN7462 customer application firmware.

Note: Transfer speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

ISO/IEC14443 A card operation mode: PN7462 can be addressed as a ISO/IEC 14443 A card. It means that PN7462 can generate an answer in a load modulation scheme according to the ISO/IEC 14443 A interface description.

Note: PN7462 component does not support a complete card protocol. The PN7462 customer application firmware handles it.

The following table describes the physical layer of a ISO/IEC14443 A card mode:

Table 16. ISO/IEC14443 A card operation mode

Communication direction	ISO/IEC 14443 A (transfer speed: 106 kbit per second)	
reader/writer to PN7462	modulation on reader side	100 % ASK
	bit coding	modified miller
	bit length	$128/f_c$
PN7462 to reader/writer	modulation on PN7462 side	sub carrier load modulation
	subcarrier frequency	f_c / 16
	bit coding	manchester coding

NFCIP-1 framing and coding: The NFCIP-1 framing and coding in active and passive communication mode is defined in the NFCIP-1 standard.

PN7462 supports the following data rates:

Table 17. Framing and coding overview

Transfer speed	Framing and coding
106 kbit/s	according to the ISO/IEC 14443 A/MIFARE scheme
212 kbit/s	according to the FeliCa scheme
424 kbit/s	according to the FeliCa scheme

NFCIP-1 protocol support: The NFCIP-1 protocol is not elaborated in this document. The PN7462 component does not implement any of the high-level protocol functions. These high-level protocol functions are implemented in the microcontroller. For detailed explanation of the protocol, refer to the NFCIP-1 standard. However, the datalink layer is according to the following policy:

- Speed shall not be changed while there is continuous data exchange in a transaction.

- Transaction includes initialization, anticollision methods, and data exchange (in a continuous way means no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz, the following general rules to start NFCIP-1 communication are defined:

1. By default, NFCIP-1 device is in target mode. It means that its RF field is switched off.
2. The RF level detector is active.
3. Only if the application requires, the NFCIP-1 device switches to initiator mode.
4. An initiator shall only switch on its RF field if the RF level detector does not detect external RF field during a time of T_{IDT}.
5. The initiator performs initialization according to the selected mode.

8.10.2 Low-Power Card Detection (LPCD)

The low-power card detection is an energy saving feature of the PN7462. It detects the presence of a card without starting a communication. Communication requires more energy to power the card and takes time, increasing the energy consumption.

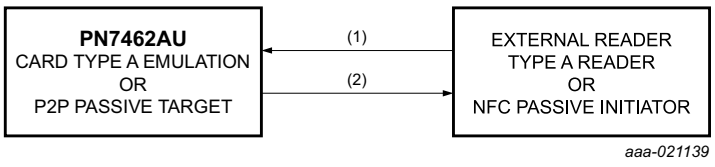
It is based on antenna detuning detection. When a card comes close to the reader, it affects the antenna tuning, which is detected by PN7462.

The sensitivity can be varied for adjusting to various environment and applications constraints.

Remark: Reader antenna detuning may have multiple sources such as cards and metal near the antenna. Hence it is important to adjust the sensitivity with care to optimize the detection and power consumption. As the generated field is limited, distance for card detection might be reduced compared to normal reader operation. Performances depend on the antenna and the sensitivity used.

8.10.3 Active Load Modulation (ALM)

When PN7462 is used in card emulation mode or P2P passive target mode, it modulates the field emitted by the external reader or NFC passive initiator.



(1) Type A reader or NFC passive initiator generate the RF and sends commands

(2) PN7462 modulates the field of reader for sending its answer

Fig 20. Communication in card emulation of NFC passive target

To modulate the field, PN7462 has two possibilities:

- Passive Load Modulation (PLM): The PN7462 modifies the antenna characteristics, which is detected by the reader through antenna coupling.

- Active Load Modulation (ALM): The PN7462 generates a small field, in phase opposition with the field emitted by the reader. This modulation is detected by the reader reception stage.

The modulation type to use depends on the external reader and the antenna of PN7462 and the application.

8.10.4 Contactless interface

8.10.4.1 Transmitter (TX)

The transmitter is able to drive an antenna circuit connected to outputs TX1 and TX2 with a 13.56 MHz carrier signal. The signal delivered on pins TX1 and pin TX2 is a 13.56 MHz carrier, modulated by an envelope signal for energy and data transmission. It can be used to drive an antenna directly, using a few passive components for matching and filtering. For a differential antenna configuration, either TX1 or TX2 can be configured to put out an inverted clock. 100 % modulation and several levels of amplitude modulation on the carrier can be performed to support 13.56 MHz carrier-based RF-reader/writer protocols. The standards ISO/IEC14443 A and B, FeliCa and ISO/IEC18092 define the protocols.

PN7462 transmitter facilitates 10 % and 100 % amplitude modulation, as per the RF standards supported.

The PN7462 embeds an overshoot and undershoot protection. It is used to configure additional signals on the transmitter output, for controlling the signal shape at the antenna output.

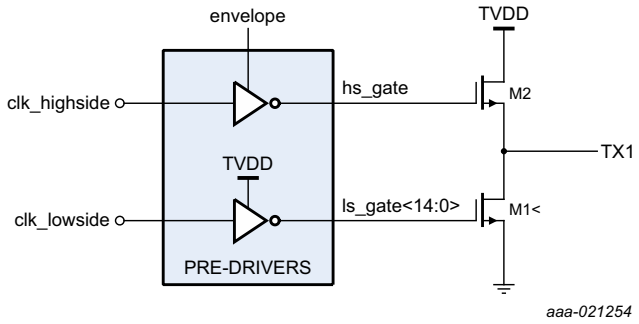


Fig 21. PN7462 output driver

8.10.4.2 Receiver (RX)

In reader mode, the response of the PICC device is coupled from the PCB antenna to the differential input RXP/RXN. The reader mode receiver extracts this signal by first removing the carrier in passive mixers (direct conversion for I and Q). It then filters and amplifies the baseband signal before converting to digital values. The conversion to digital values is done with two separate ADCs, for I and Q channels. Both I and Q channels have a differential structure, which improves the signal quality.

The I/Q mixer mixes the differential input RF-signal down to the baseband. The mixer has a bandwidth of 2 MHz.

The down-mixed differential RX input signals are passed to the BBA and a band-pass filter. For considering all the protocols (type A/B, FeliCa), the high-pass cut-off frequency of BBA is configured between 45 kHz and 250 kHz. The configuration is done in four different steps. The low-pass cut-off frequency is greater than 2 MHz.

The output of band-pass filter is further amplified with a gain factor which is configurable between 30 dB and 60 dB. The baseband amplifier (BBA)/ADC I-channel and Q-channel can be enabled separately. It is required for ADC-based card mode functionality as only the I-channel is used in this case.

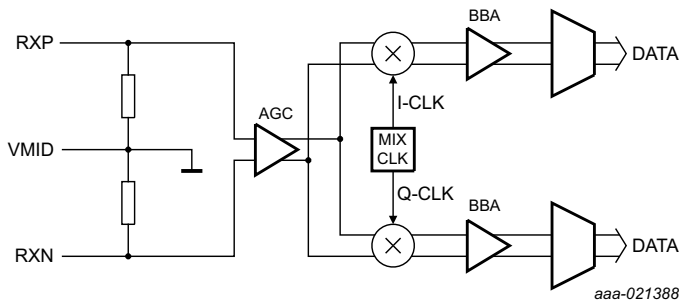


Fig 22. Receiver block diagram

VMID: A resistive divider between AVDD and GND generates VMID. The resistive divider is connected to the VMID pin. An external blocking capacitor of typical value 100 nF is connected.

Automatic Gain Control (AGC): The contactless interface AGC is used to control the amplitude of 13.56 MHz sine-wave input signal received. The signal is received at the antenna connected between the pins RXP and RXN. A comparator is used to compare the peak value of the input signal with a reference voltage.

A voltage divider circuit is used to generate the reference voltage. An external resistor (typically 3.3 kΩ) is connected to the RX input, which forms a voltage divider with an on-chip variable resistor. The voltage divider circuit so formed has a 10-bit resolution.

Note: The comparator monitors the RXP signal only.

By varying the on-chip resistor, the amplitude of the input signal can be modified. The value of on-chip resistor is increased or decreased, depending on the output of the sampled comparator. The on-chip resistor value is adjusted until the peak of the input signal matches the reference voltage. Thus, the AGC circuit automatically controls the amplitude of the RX input.

The internal amplitude controlling resistor in the AGC has a default value of 10 KΩ. It means that, when the resistor control bits in AGC_VALUE_REG <9:0> are all 0, the resistance is 10 KΩ. As the control bits are increased, resistors are switched in parallel to the 10 KΩ resistor. It lowers the resultant resistance value to 5 kΩ (AGC_VALUE_REG <9:0>, all bits set to 1).

Mode detector: The mode detector is a functional block of the PN7462 which senses for an RF field generated by another device. The mode detector facilitates to distinguish between type A and Felica target mode. The host responds depending on the recognized protocol generated by an initiator peer device.

Note: The PN7462 emulates type A cards and peer-to-peer active target modes according to ISO / IEC18092.

8.10.5 Dynamic Power Control (DPC)

The PN7462 supports the Dynamic Power Control (DPC) feature.

The dynamic power controls the RF output current dependent on the loading condition of the antenna.

A lookup table is used to configure the output voltage and to control the transmitter current. In addition to the control of the transmitter current, wave shaping settings can be controlled as well, depending on the selected protocol and the measured antenna load.

8.11 Timers

The PN7462 includes two 12-bit general-purpose timers (on LFO clock domain) with match capabilities. It also includes two 32-bit general-purpose timers (on HFO clock domain) and a WatchDog Timer (WDT).

The timers and WDT can be configured through software via a 32-bit APB slave interface.

Table 18. Timer characteristics

Name	Clock source	Frequency	Counter length	Resolution	Maximum delay	Chaining
Timer 0	LFO/2	182.5 kHz	12-bit	300 µs	1.2 s	No
Timer 1	LFO/2	182.5 kHz	12-bit	300 µs	1.2 s	Yes
Timer 2	HFO	20 MHz	32-bit	50 ns	214 s	No
Timer 3	HFO	20 MHz	32-bit	50 ns	214 s	No
Watchdog	LFO/128	2.85 kHz	10-bit	21.5 ms	22 s	No

8.11.1 Features of timer 0 and timer 1

- 12-bit counters
- One match register per timer, no capture registers and capture trigger pins are needed
- One common output line gathering the four timers (Timer 0, Timer 1, Timer 2, and Timer 3)
- Interrupts
- Timer 0 and timer 1 can be concatenated (multiplied)
- Timer 0 and timer 1 have two count modes: single-shot or free-running
- Timer 0 and timer 1 time-out interrupts can be individually masked
- Timer 0 and timer 1 clock source is LFO clock (LFO/2 = 182.5 kHz)

Remark: The timers are dedicated for RF communication.

8.11.2 Features of timer 2 and timer 3

- 32-bit counters
- 1 match register per timer, no capture registers and capture trigger pins are needed
- 1 common output line gathering four timers (Timer 0, Timer 1, Timer 2, and Timer 3)
- Interrupts
- Timer 2 and timer 3 have two count modes: single-shot and free-running
- Timer 2 and timer 3 time-out interrupts can be individually masked
- Timer 2 and timer 3 clock source is the system clock

8.12 System tick timer

The PN7462 microcontroller includes a system tick timer (SYSTICK) that generates a dedicated SYSTICK exception at a fixed time interval (10 ms).

8.13 Watchdog timer

If the microcontroller enters an erroneous state, the watchdog timer resets the microcontroller. When the watchdog timer is enabled, if the user program fails to “feed” (reload) the watchdog timer within a predetermined time, it generates a system reset.

The watchdog timer can be enabled through software. If there is a watchdog timeout leading to a system reset, the timer is disabled automatically.

- 10-bit counter
- Based on a 2.85 kHz clock
- Triggers an interrupt when a predefined counter value is reached
- Connected to the ARM subsystem NMI (non-maskable interrupt)
- If the watchdog timer is not periodically loaded, it resets PN7462

8.14 Clocks

The PN7462 clocks are based on the following clock sources:

- 27.12 MHz external quartz
- 27.12 MHz crystal oscillator
- Internal oscillator: 20 MHz High Frequency Oscillator (HFO)
- Internal oscillator: 365 kHz Low Frequency Oscillator (LFO)
- Internal PLL at 48 MHz for the USB interface

Figure 23 indicates the clocks used by each IP.

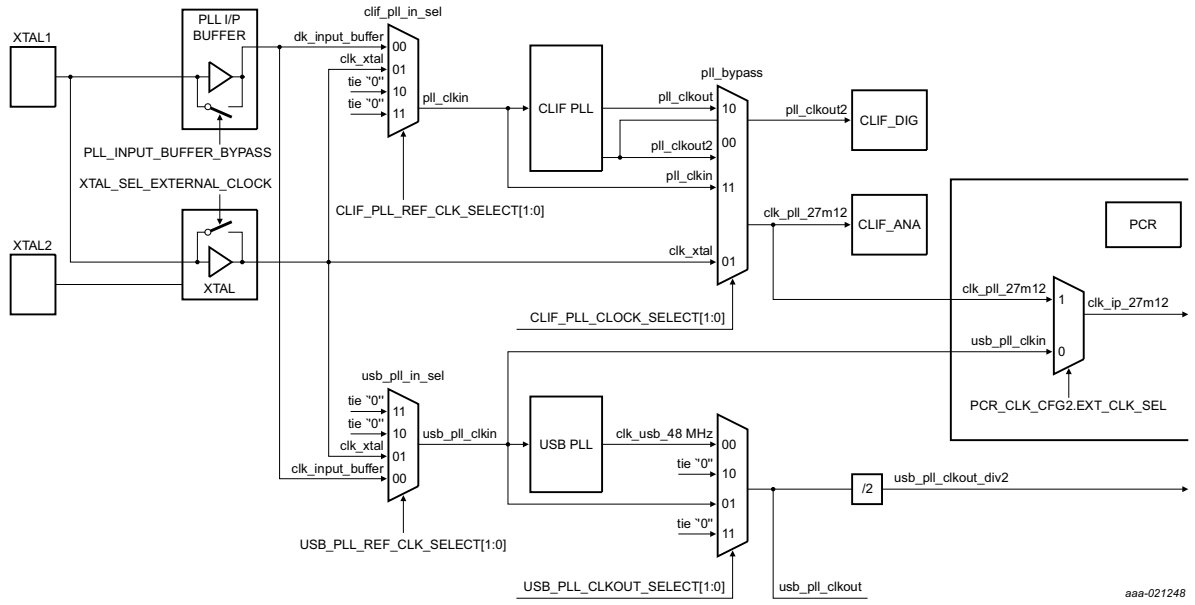


Fig 23. Clocks and IP overview

8.14.1 Quartz oscillator (27.12 MHz)

The 27.12 MHz quartz oscillator is used as a reference for all operations where the stability of the clock frequency is important for reliability. It includes contactless interface, contact interface, SPI and I^2C master interfaces, USB PLL for the USB interface, and HSUART.

Regular and low-power crystals can be used. Figure 24 shows the circuit for generating stable clock frequency. The quartz and trimming capacitors are off-chip.

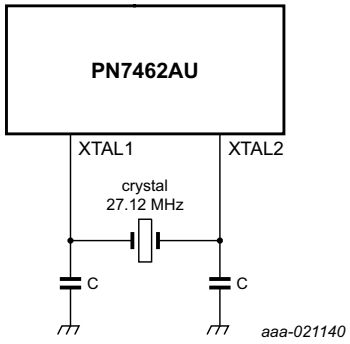


Fig 24. Crystal oscillator connection

Table 19 describes the levels of accuracy and stability required on the crystal.

Table 19. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC and FCC compliancy		27.12		MHz
Δf_{xtal}	crystal frequency accuracy	[1]	–50		+50	ppm
ESR	equivalent series resistance			50	100	Ω
C_L	load capacitance			10		pF
P_{drive}	drive power				100	µW

[1] This requirement is according to FCC regulations requirements. The frequency should be +/– 14 kHz to meet ISO/IEC 14443 and ISO/IEC 18092.

8.14.2 USB PLL

The PN7462 integrates a dedicated PLL to generate a low-noise 48 MHz clock, by using the 27.12 MHz from the external crystal. The 48 MHz clock generated is used as the USB main clock.

Following are the USB PLL features:

- Low-skew, peak-to-peak cycle-to-cycle jitter, 48 MHz output clock
- Low power in active mode, low power-down current
- On-chip loop filter, external RC components not needed

8.14.3 High Frequency Oscillator (HFO)

The PN7462 has an internal low-power High Frequency Oscillator (HFO) that generates a 20 MHz clock. The HFO is used to generate the system clock. The system clock default value is 20 MHz, and it can be configured to 10 MHz and 5 MHz for reducing power consumption.

8.14.4 Low Frequency Oscillator (LFO)

The PN7462 has an internal low-power Low Frequency Oscillator (LFO) that generates a 365 kHz clock. The LFO is used by EEPROM, POR sequencer, contactless interface, timers, and watchdog.

8.14.5 Clock configuration and clock gating

In order to reduce the overall power consumption, the PN7462 facilitates adjustment of system clock. It integrates clock gating mechanisms.

The system clock can be configured to the following values: 20 MHz, 10 MHz, and 5 MHz.

The clock of the following blocks can be activated or deactivated, depending on the peripherals used:

- Contactless interface
- Contact interface
- Host interfaces
- I^2C master interface
- SPI master interface
- CRC engine

- Timers
- Random generator
- System clock
- EEPROM
- Flash memory

8.15 Power management

8.15.1 Power supply sources

The PN7462 is powered using the following supply inputs:

- VBUS: main supply voltage for internal analog modules, digital logic and memories
- VBUSP: supply voltage for the contact interface
- TVDD_IN: supply for the contactless interface
- PVDD_IN: pad voltage reference and supply of the host interface (HSU, USB, I^2C, and SPI) and the GPIOs
- PVDD_M_IN: pad voltage reference and supply for the master interface (SPI and I^2C)
- DVDD: supply for the internal digital blocks

8.15.2 PN7462 Power Management Unit (PMU)

The integrated Power Management Unit (PMU) provides supply for internal analog modules, internal digital logic and memories, pads. It also provides supply voltages for the contactless and contact interface.

It automatically adjusts internal regulators to minimize power consumption during all possible power states.

The power management unit embeds a mechanism to prevent the IC from overheat, overconsumption, or overloading the DC-to-DC converter:

- TXLDO 5 V monitoring
- VCC current limiter
- DC-to-DC converter current overload
- SCVDD current overload
- Temperature sensor

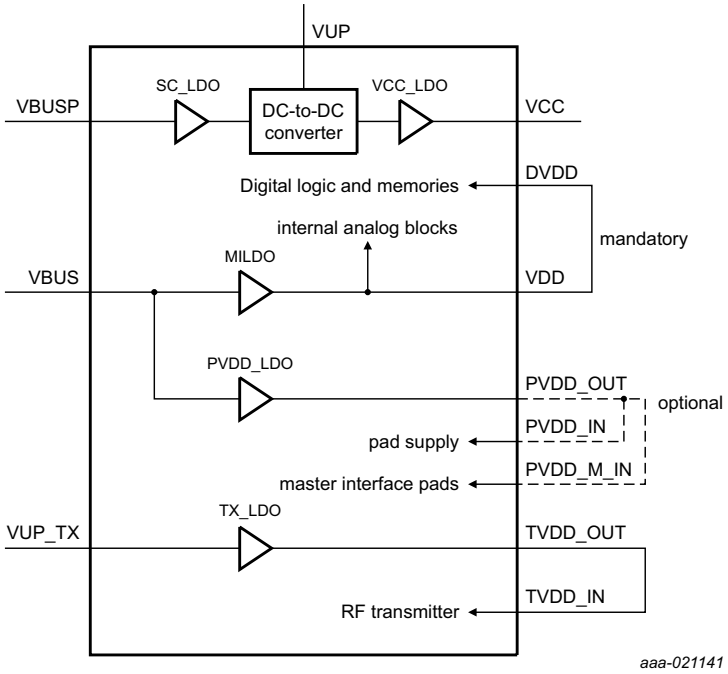


Fig 25. PN7462 LDOs and power pins overview

PN7462 embeds five Low Drop-Out regulators (LDO) for ensuring the stability of power supply, while the application is running.

- MLDO (main LDO): It provides1.8 V supply for internal analog, digital and memory modules
- TXLDO: This LDO can be used to supply the RF transmitter
- PVDD_LDO: PVDD_LDO provides 3.3 V that can be used for all pads supply
- SCLDO: This LDO provides a 2.4 V output to be used for contact card supply. The main aim is to be able to address class B operation when the voltage available is below 3.9 V. It is achieved by providing a stable input voltage to the internal DC-to-DC converter.
- VCC_LDO: the VCC_LDO provides the supply for the contact smart card

Some are used while some are optional, like the TX_LDO which is proposed for the RF interface. It is up to the application designer to decide whether LDOs should be used.

8.15.2.1 Main LDO

The Main LDO (MLDO) provides a 1.8 V supply for all internal, digital and memory modules. It takes input from VBUS. MLDO includes a current limiter that avoids damage to the output transistors.

Output supply is available on VDD pin which must be connected externally to the DVDD pin.

Following are the main LDO features:

- Main Low-Drop-Out (MLDO) voltage regulator powered by VBUS (external supply)

- Current limiter to avoid damaging the output transistors

8.15.2.2 PVDD_LDO

The PVDD_LDO provides 3.3 V supply, that can be used for all digital pads. It may also be used to provide 3.3 V power to external components, avoiding an external LDO. It is supplied by VBUS, and requires a minimum voltage of 4 V to be functional. It delivers a maximum of 30 mA.

The output pin for PVDD_LDO is PVDD_OUT.

PVDD_LDO is used to provide the necessary supply to PVDD_IN and PVDD_M_IN (pad supply for master interfaces).

When an external supply is used, PVDD_OUT must be connected to the ground. When the LDO output is connected to the ground, the PN7462 chip switches off the PVDD_LDO.

The PVDD LDO has a low-power mode, which is used automatically by the PN7462 when the chip is in standby mode or suspend mode. It facilitates supply to HOST pads and GPIOS, and to detect wake-up signals coming from these interfaces.

Following are the PVDD_LDO features:

- Low-Drop-Out voltage regulator powered by $V_{DDP(VBUS)}$ (external supply)
- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance when the LDO is powered up
- Current limiter to avoid damaging the output transistors

Note: When PVDD_LDO is used, there must not be any load current drawn from PVDD_LDO during the soft start of the PVDD_LDO.

8.15.2.3 Contact interface - SCLDO LDO

The SCLDO provides a regulated voltage to the DC-to-DC converter, to enable class B operation when $V_{DDP(VBUS)}$ is in between 2.7 V to 3.9 V.

Following are the contact interface features:

- Current limiter for short circuit protection
- Supports soft-start mode to limit the inrush current during the initial charge of the external capacitance when the LDO is powered up

8.15.2.4 Contact interface DC-to-DC converter

The PN7462 includes a DC-to-DC converter that supports class A and class B cards, when the input voltage $V_{DDP(VBUSP)}$ is not sufficient.

The DC-to-DC converter is a capacitance voltage doubler. It takes power from the SCLDO. The DC-to-DC converter can be bypassed. Its output (VUP) is regulated between 3.3 V to 5.5 V.

The DC-to-DC converter can work in the following modes:

- Follower mode: This mode is used when $V_{DDP(VBUSP)}$ is high enough to provide the desired power to the VCC LDO

- Doubler mode: This mode is used when $V_{DDP(VBUSP)}$ is not high enough to supply the requested V_{CC} output

The doubler mode is used in the following conditions:

- Class A cards support
- Class B cards support, when $V_{DDP(VBUSP)}$ is less than 3.9 V

For class C cards, the DC-to-DC converter is always in a follower mode.

An external capacitor (470 nF) should be connected between SAM and SAP pins, to ensure the functioning of the DC-to-DC converter.

Table 20. SCLDO and DC-to-DC converter modes

Supported card	$V_{DDP(VBUSP)}$	SCLCO mode	DC-to-DC converter mode
Class A	> 3 V	follower mode	doubler mode
Class B	2.7 V < $V_{DDP(VBUSP)}$ < 3.9 V	LDO mode	doubler mode
Class B	> 3.9 V	follower mode	follower mode
Class C	> 2.7 V	follower mode	follower mode

8.15.2.5 VCC LDO

The VCC LDO supplies contact interface supply V_{CC}.

Following are the VCC LDO features:

- Low drop-out voltage regulator
- Current limiter for chip and card protection
- Automatic deactivation in case of overload

8.15.2.6 TXLDO

The PN7462 consists of an internal transmitter supply LDO. The TXLDO can be used to maintain a constant output voltage for the RF interface.

The TX LDO is designed to protect the chip from voltage ripple introduced by the power supply on the pin VUP_TX. It is powered through the pin VUP_TX.

The programmable output voltages are: 3.0 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V.

For a given output voltage, VUP_TX shall always be higher than 0.3 V. In other words, to supply a 3 V output, the minimum voltage to be applied on VUP_TX is 3.3 V. If the voltage is not sufficient, then the voltage at the pin TVDD_OUT follows the voltage at the pin VUP_TX, lowered of 0.3 V.

When it is not used, TVDD_OUT shall be connected to TVDD_IN, and TX_LDO shall be turned off.

Following are the TXLDO features:

- Low-Drop-Out (TXLDO) voltage regulator
- Current load up to 180 mA

- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance
- Current limiter to avoid damaging the output transistors

8.15.3 Power modes

The PN7462 offers four different power modes, that enable the user to optimize its energy consumption. They are:

- Hard power-down mode
- Standby mode
- USB suspend mode
- Active mode

8.15.3.1 Active mode

In active mode, all functionalities are available and all IPs can be accessed. It is possible to configure the various clocks (IP clock, system clock) using register settings so that chip consumption is reduced. If IPs are not used, they can be disabled.

8.15.3.2 Standby mode

In standby mode, only a reduced part of the digital and the analog is active. It reduces the chip power consumption. The possible wake-up sources are still powered.

The LFO clock is used to lower the energy needs.

Active part in standby mode: Main LDO is active, in a low-power mode, plus all configured wake-up sources.

Depending on the application requirements, it is possible to configure PVDDL_LDO in active mode, low-power mode or shut down mode when PN7462 is going to standby mode. PVDD_LDO is active in a low-power mode by default.

Entering in standby mode: The application code triggers standby mode. Before entering in standby mode, the PN7462 manages the deactivation of the contact card.

The PN7462 has two internal temperature sensors. If these sensors detect an overheat, the PN7462 is put into standby mode by the application firmware. The chip leaves the standby mode when both temperature sensors indicate that the temperature has come below the configured limit.

Limitations: Standby mode is not possible in the following cases:

- A host communication is in progress
- A wake-up condition is fulfilled. For example, external RF field presence is a wake-up source, and PN7462 detects a field
- The RF field detector is a possible wake-up source, and the RF field detector is disabled
- PVDD is **not** present

8.15.3.3 Suspend mode

In suspend mode, clock sources are stopped except LFO. It reduces the chip power consumption.

Entering in suspend mode: An interrupt indicates to the application firmware when no activity has been detected on the USB port for more that 3 ms. The application code triggers the suspend mode.

Before entering in suspend mode, the PN7462 manages automatically, the deactivation of the contact card.

Limitations: Suspend mode is prevented in the following cases:

- A host communication is in progress
- A wake-up condition is fulfilled. For example, external RF field presence is a wake-up source, and PN7462 detects a field
- The RF field detector is a possible wake-up source, and the RF field detector is disabled
- No voltage at pin PVDD

8.15.3.4 Wake-up from standby mode and suspend mode

PN7462 can be woken-up from standby mode, and suspend mode, using the following means:

- Host Interface: SPI, HSUART, I^2C, and USB if already selected before standby mode (SPI, HSUART, and I^2C) or suspend mode (USB).
- RF field detection (presence of a reader or an NFC device in reader mode or P2P initiator)
- GPIO
- Contact card insertion, contact card removal
- Interrupt generated on the auxiliary UART interface, through the interrupt pin
- Wake-up counter, for example to timely check for the presence of any contact or contactless card
- Current overconsumption on the PVDD_OUT, voltage above 5 V on TVDD_IN
- Temperature sensor: When the PN7462 goes in to standby mode because of over-heating, and when the temperature goes below the sensor configured value, PN7462 wakes-up automatically. Each temperature sensor can be configured separately.

It is possible to configure the sources as enabled or disabled.

8.15.3.5 Hard Power-Down (HPD) mode

The PN7462 Hard Power-Down (HPD), reduces the chip power consumption, by powering down most of the chip blocks. All clocks and LDOs are turned off, except the main LDO which is set in low-power mode.

Entering in HPD mode: If the RST_N pin is set to low, the PN7462 enters in to Hard Power Down (HPD) mode. It also enters in to HPD mode if the $V_{DDP(VBUS)}$ goes below the critical voltage necessary for the chip to work (2.3 V) and the auto HPD feature is enabled.

Exiting the HPD mode: The PN7462 leaves the HPD mode, when both RST_N pin is set to high level and the $V_{DDP(VBUS)}$ voltage is above 2.3 V.

8.15.4 Voltage monitoring

The voltage monitoring mode detects whether the voltage is within the operational conditions to enable a proper operation of the RF interface or the contact interface. The following power supplies are monitored: VBUS (two voltage monitors), VBUS_P (one voltage monitor).

Section 9.1.2 discusses about the minimum voltages necessary for contactless interface operation and Section 9.1.3 for the contact interface operation.

Table 21. Threshold configuration for voltage monitor

Voltage monitor	Threshold 1	Threshold 2	Threshold 3
VBUSMON1	2.3 V	2.7 V	n.a.[1]
VBUSMON2	2.7 V	4.0 V	n.a.[1]
VBUSP	2.7 V	3.0 V	3.9 V

[1] n.a. means not applicable.

8.15.4.1 VBUS monitor

The PN7462 includes up to two levels (2.3 V or 2.7 V) for monitoring the voltage on the VBUS pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the PCR. This signal may be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels (2.3 V or 2.7 V) can be selected to cause a forced Hard Power-Down (HPD) of chip.

8.15.4.2 VBUSP monitor

The PN7462 includes three levels (2.7 V, 3.0 V, and 3.9 V) for monitoring the voltage on the VBUSP pin.

When the voltage falls below the selected threshold value, and CT automatic deactivation is enabled in the PCR system register, hardware automatically de-activates the CT interface. An interrupt signal is also asserted to the PCR. This signal can be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Software must check VBUSP monitor levels by reading dedicated status registers before starting card activation sequence.

8.15.4.3 PVDD LDO supply monitor

The PN7462 includes up to two levels (VBUS2: 2.7 V or 4.0 V) for monitoring the voltage on the PVDD LDO input supply. If supply voltage is 4.0 V or above, PVDD LDO can be enabled. The software has to check whether the voltage is sufficient before enabling the LDO.

8.15.5 Temperature sensor

The PN7462 power management unit provides temperature sensors, associated to the TX_LDO and the contact interface DC-to-DC converter. It detects problems that would result in high power consumption and heating, which could damage the chip and the user device.

Triggering levels are configurable. Following temperatures can be chosen: 135 °C, 130 °C, 125 °C, and 120 °C. By default, the temperature sensor is set to 120 °C.

When one of the temperature sensors detects an increase in temperature above the configured level, an interrupt is generated. The application can then decide to go into standby or suspend mode. The PN registers indicate which temperature sensor generated the interrupt.

When the temperature goes below the configured threshold temperature, PN7462 wakes up automatically.

8.16 System control

8.16.1 Reset

PN7462 has six possible sources for reset. The list of sources is described in Table 22.

Table 22. Reset sources

Source	Description
software - PCR	soft reset from the PCR peripheral
software - ARM	software reset form the ARM processor
I^2C interface	I^2C Standard 3.0 defines a method to reset the chip via an I^2C command[1]
watchdog	reset the chip if the watchdog threshold is not periodically reloaded
VBUS voltage	power-on reset sequence; if the voltage is above 2.3 V, reset the chip

[1] This feature can be disabled.

The watchdog reset, I^2C reset and soft resets from PCR and ARM processor resets the chip except the PCR and the ARM debug interface. The Power-On Reset (POR) resets the complete chip including the PCR and ARM debug interface.

Upon reset, the processor executes the first instruction at address 0, which is initially the reset vector mapped from the boot block. At that point, all the processor and peripheral registers are initialized to predetermined values.

8.16.2 Brown-Out Detection (BOD)

The PN7462 includes up to two levels for monitoring the voltage on the VBUS pin. If this voltage falls below one of the selected voltages (2.3 V or 2.7 V), the BOD asserts an interrupt signal to the PCR. This signal can be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels (2.3 V and 2.7 V) can be selected to cause a forced Hard Power-Down (HPD) of the chip.

8.16.3 APB interface and AHB-Lite

All APB peripherals are connected to one APB bus.

The AHB-Lite connects the AHB masters. The AHB masters include the CPU bus of the ARM Cortex-M0, host interface, contactless interface, SPI interface to the flash memory. It also includes EEPROM memory, SRAM, ROM, and AHB to APB bridge.

8.16.4 External interrupts

PN7462 enables the use of 12 GPIOs as edge or level sensitive inputs (GPIO1 to GPIO12).

8.17 SWD debug interface

The Cortex-M0 processor-based devices use serial wire ARM CoreSight™ Debug technology. The PN7462 is configured to support four break points and two watch points.

The SWD interface can be disabled for having code (or data) read/write access protection. A dedicated SWD disable bit is available in the protected area of the EEPROM memory. Once the SWD interface is disabled, it is not possible to enable it anymore.

8.17.1 SWD interface features

- Run control of the processor allowing to start and stop programs
- Single step one source or assembler line
- Set breakpoints while the processor is running
- Read/write memory contents and peripheral registers on-the-fly
- “Printf” like debug messages through the SWD interface

9. Application design-in information

9.1 Power supply connection

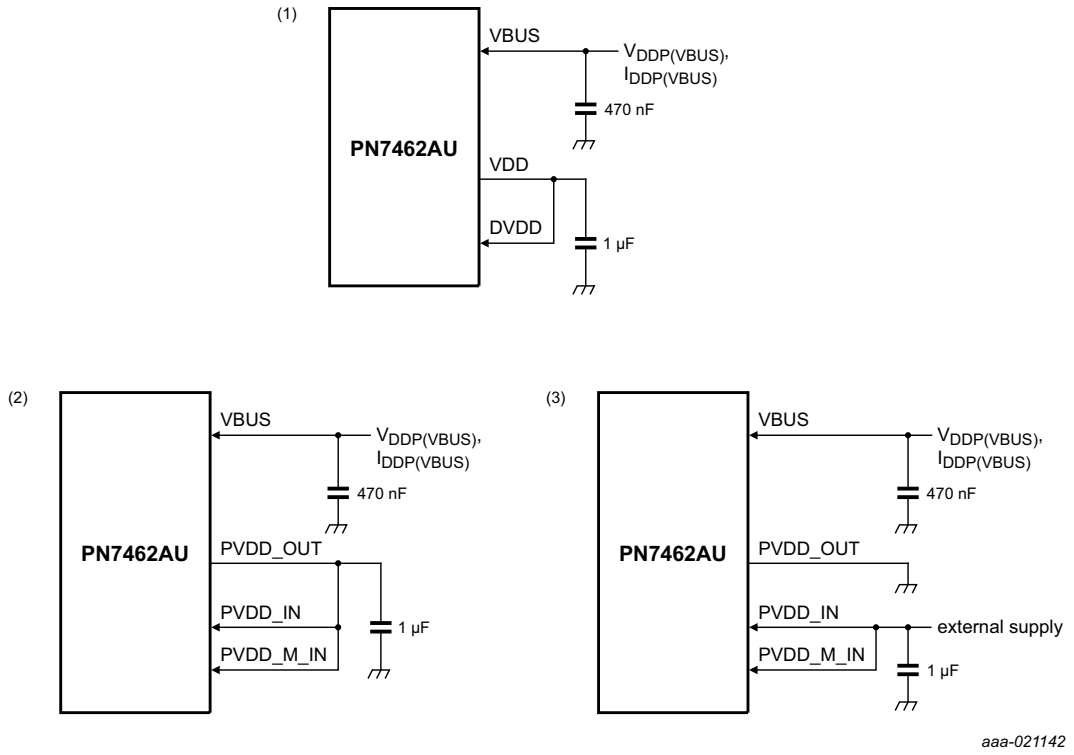
The following table indicates the power sources for all the PN7462 power inputs.

Table 23. Power supply connection

Power inputs	Power sources	Comment
VBUS	external source	chosen according to the expected performances (contact interface and Class A/B/C support, RF power when TX_LDO is used, global power consumption)
VBUSP	external source; connected to VBUS	VBUSP is connected to VBUS, with the addition of a decoupling capacitor
TVDD_IN	external supply or using the TX_LDO	external supply can be used (up to 5.5 V) to increase RF power
PVDD_IN	external supply or using PVDD_LDO	PVDD_LDO can be used, when $V_{DDP(VBUS)}$ > 4 V. It makes a regulated 3.3 V supply available to GPIO and host interface pads, without the addition of an external LDO
		for 1.8 V, external supply is used
PVDD_M_IN	external supply or using PVDD_LDO	PVDD_LDO can be used, when $V_{DDP(VBUS)}$ > 4 V. It makes a regulated 3.3 V supply available to GPIO and host interface pads, without the addition of an external LDO
		external supply is used for 1.8 V
DVDD	connected to the VDD output	VDD provides 1.8 V stabilized supply, out of the MAIN_LDO

[1] When external supply and PVDD_OUT are not used, PVDD_OUT must be connected to the ground, with a ground resistance of less than 10 Ω.

9.1.1 Powering up the microcontroller



(1) Powering up the microcontroller and the digital blocks (DVDD).

(2) Two possibilities for powering the pad interfaces (PVDD_IN and PVDD_M_IN).

Remark: The capacitance must be chosen so that the capacitance value is correct at 5 V

Fig 26. Powering up the PN7462 microcontroller

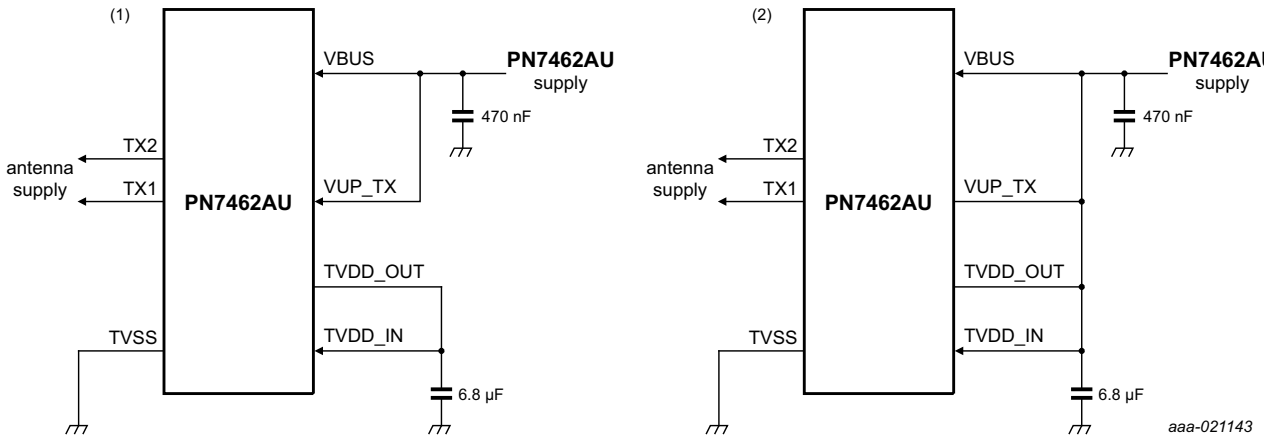
The schematics in Figure 26 describe the power supply of the chip ($V_{DDP(VBUS)}$), including the digital blocks supply (DVDD). It indicates two possibilities to supply the pads, using the internal LDO, or using an external supply. The internal LDO requires that $V_{DDP(VBUS)} > 4$ V. It avoids the requirement of a separate LDO when $V_{DDP(VBUS)}$ has a sufficient voltage.

Power supply is available to pads through PVDD_IN (host interface). Similarly, power supply is available to master interface pads through PVDD_M_IN. When PVVD _LDO is used, maximum total current available from PVDD_OUT for the pads supply is 30 mA.

When an external source is used for PVDD_IN and PVDD_M_IN, PVDD_OUT must be connected to the ground, with a ground resistance of less than 10 Ω.

9.1.2 Powering up the contactless interface

Powering of contactless interface is done though TVDD_IN. Internal LDO (TXLDO) or external supply can be used.

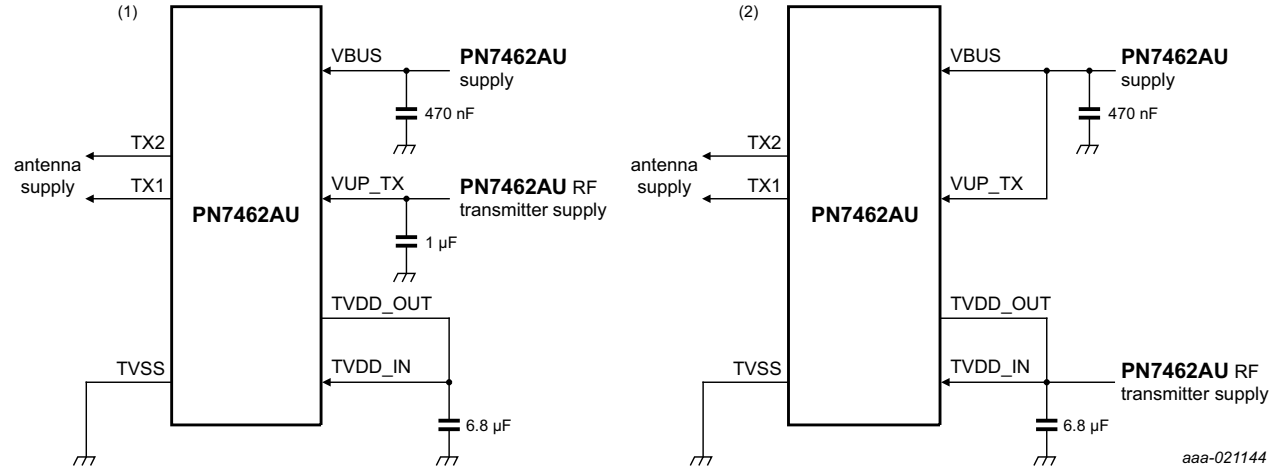


The capacitance value must be chosen so that the capacitance value is correct at 5 V.

(1) Using TXLDO

(2) Without using TXLDO

Fig 27. Powering up the contactless interface using a single power supply



The capacitance value must be chosen so that the capacitance value is correct at 5 V.

(1) Using TXLDO.

(2) Without using TXLDO.

Fig 28. Powering up the contactless interface using an external RF transmitter supply

Note: The TVDD_OUT pin must not be left floating. It should be at the same voltage as the TVDD_IN pin.

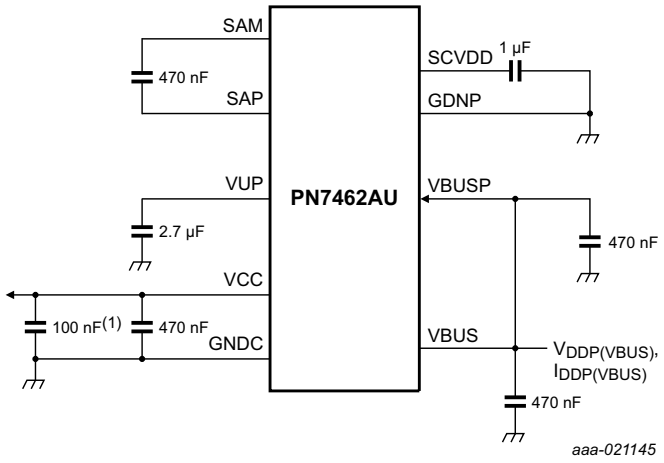
The power design must be designed properly to be able to deliver a clean power supply voltage

In any case (external TVDD or internal TX_LDO internal supply), TVDD_IN supply must be stable before turning on the RF field. The capacitor shall be 6.8 µF or higher (up to 10 µF)

Every noise level on top of the supply voltage can disturb the RF communication performance of the PN7462. Therefore, special attention must be paid to the filtering circuit.

When powering up the device through the USB interface, TVDD capacitor shall be such that the maximum capacitance on VBUS is as per the USB specification.

9.1.3 Powering up the contact interface



(1) The capacitances values must be chosen so that the capacitance values are correct at 5.6 V.

Fig 29. Powering up the contact interface

Contact interface is powered through VBUSP. VBUSP must be connected to VBUS, as per the schematic in Figure 29.

In order to provide the right voltage needed for the various ISO/IEC 7816 contact card classes (A, B, or C), the following voltages are needed:

- $V_{DDP(VBUSP)}$ > 2.7 V: Support of class B and class C contact cards
- $V_{DDP(VBUSP)}$ > 3 V: Support of class A contact cards

Remark: To support class A cards, DC-to-DC converter is used. To support class B cards with $V_{DDP(VBUSP)}$ < 3.9 V, DC-to-DC converter is used.

Figure 30 indicates the method to connect the pins related to contact interfaces, when no contact interface is used.

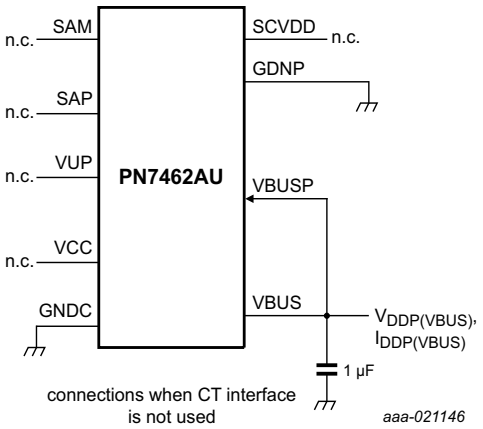
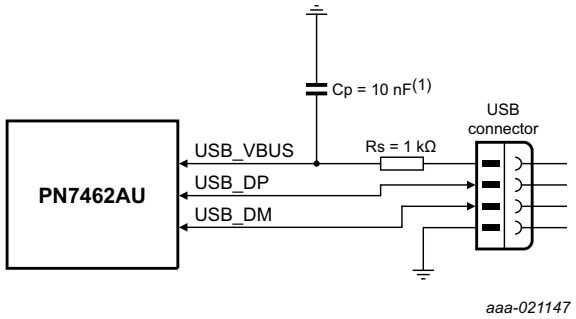


Fig 30. Contact interface power supply connection when contact interface is not used

9.2 Connecting the USB interface



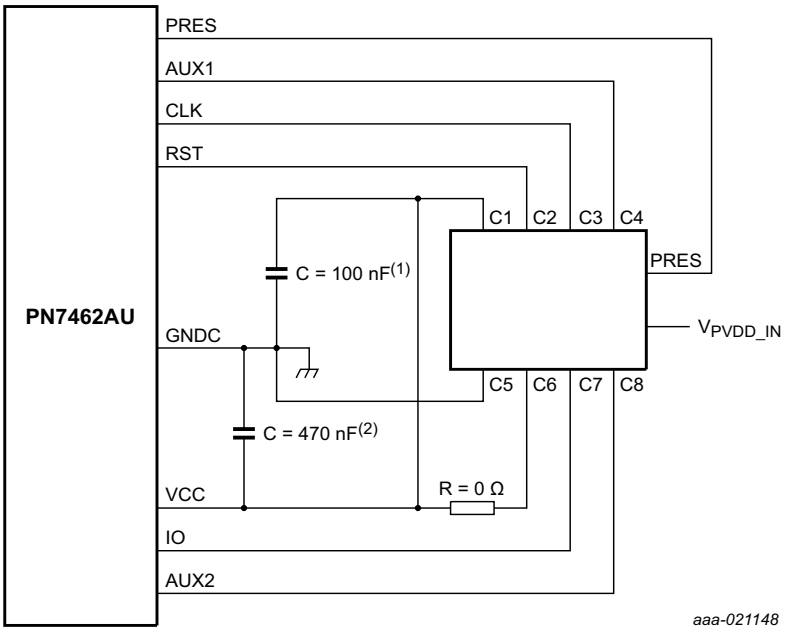
(1) C_p is optional.

Fig 31. USB interface on a bus-powered device

When the USB interface is not used, the USB_VBUS pin shall be connected to the ground.

9.3 Connecting the contact interface

The following diagrams indicate the method to connect the contact interface, when the contact interface is used, and when it is not used.



(1) To place close to C1 (VCC) pin of the card connector, with good connection to the ground.

(2) Place close to VCC pin, with good connection to GNDC.

Fig 32. Connecting the contact interface

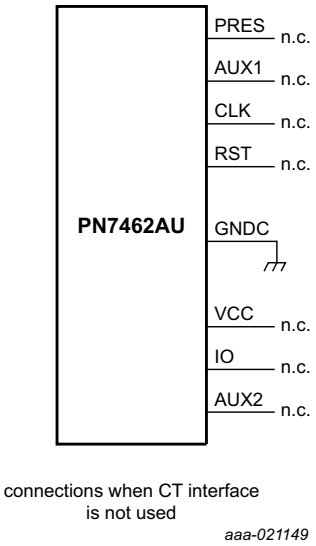


Fig 33. Connection of contact interface when not used

9.4 Connecting the RF interface

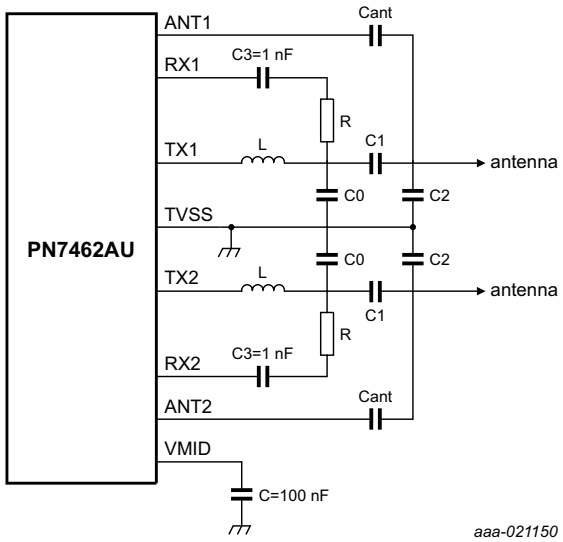


Fig 34. RF interface - example of connection to an antenna

10. Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)			
		on card pins IO, RST, VCC, AUX1, CLK, AUX2, PRESN [1]	–12	+12	kV
		on all pins except contact interface pins [1]	–2	+2	kV
		Charged Device Model (CDM)			
		on all pins [1]	–1	+1	kV
T_{stg}	storage temperature	non-operating	–55	+150	°C
$T_{j(max)}$	maximum junction temperature		-	+125	°C
P_{tot}	total power dissipation	reader mode; $V_{DDP(VBUS)}$ = 5.5 V	-	1050	mW

[1] EIA/JESD22-A114-D.

Table 25. Limiting values for GPIO1 to GPIO12

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage		–0.3	4.2	V

Table 26. Limiting values for I²C master pins (i2cm_sda, i2cm_scl)

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage		–0.3	4.2	V

Table 27. Limiting values for SPI master pins (spim_nss, spim_miso, spim_mosi and spi_clk)

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage		–0.3	4.2	V

Table 28. Limiting values for host interfaces atx_a, atx_b, atx_c, atx_d in all configurations (USB, HSUART, SPI and I^2C)

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage		–0.3	4.2	V

Table 29. Limiting values for crystal oscillator

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	high-level input voltage	XTAL1, XTAL2	0	2.2	V

Table 30. Limiting values for power supply

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS	[1]	–0.3	6	V
$V_{DDP(VBUSP)}$	power supply voltage on pin VBUSP	[1]	–0.3	6	V
pin supply voltage for host interface and GPIOs (on pin PVDD_IN)					
$V_{DD(PVDD)}$	PVDD supply voltage	on pin PVDD_IN; power supply for host interfaces and GPIOs [1]	–0.3	4.2	V
pin supply voltage for master interfaces (on pin PVDD_M_IN)					
$V_{DD(PVDD)}$	PVDD supply voltage	on pin PVDD_M_IN; power supply for master interfaces [1]	–0.3	4.2	V
RF interface LDO (pin VUP_TX)					
$V_{I(LDO)}$	LDO input voltage	for RF interface LDO [1]	–0.3	6	V
RF transmitter (pin TVDD_IN)					
$V_{DD(TVDD)}$	TVDD supply voltage	for RF interface transmitter [1]	–0.3	6	V

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

Table 31. Limiting values for contact interface

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	high-level input voltage	on card pins IO, RST, AUX1, AUX2, CLK	–0.3	5.75	V

Table 32. Protection and limitations for contact interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Olim}	output current limit on IO, C4, C8	class A, B, C	5	8	15	mA
I_{sd}	shutdown current	on pin V_{CC} = 5 V	70	85	110	mA
		on pin V_{CC} = 3 V (doubler mode)	75	90	110	mA
		on pin V_{CC} = 3 V (follower mode)	75	90	110	mA
		on pin V_{CC} = 1.8 V	60	70	90	mA

Table 33. Limiting values for RF interface

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage	on pins RXN and RXP	0	2.2	V

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

11. Recommended operating conditions

Table 34. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	JDEC PCB – 0.5	–40	25	85	°C
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS	external PVDD supply, card emulation and passive target (PLM)	2.3	-	5.5	V
		external PVDD supply, reader mode, NFC initiator and passive/active target mode (ALM and PLM)	2.7	-	5.5	V
		internal PVDD_LDO supply, reader mode, NFC initiator and passive/active target mode (ALM and PLM)	4	-	5.5	V
$V_{DDP(VBUSP)}$	power supply voltage on pin VBUSP	class B and class C contact card	2.7	-	5.5	V
		class A, class B, and class C contact card	3	-	5.5	V
host interface and GPIOs pin power supply (pin PVDD_IN)						
$V_{DD(PVDD)}$	PVDD supply voltage	for digital pins				
		1.8 V pin supply	1.65	1.8	1.95	V
		3.3 V pin supply	3	3.3	3.6	V
SPI master and I^2C master interfaces pin power supply (on pin PVDD_M_IN)						
$V_{DD(PVDD)}$	PVDD supply voltage	for master pins				
		1.8 V pin supply	1.65	1.8	1.95	V
		3.3 V pin supply	3	3.3	3.6	V
RF interface LDO (pin VUP_TX)						
$V_{I(LDO)}$	LDO input voltage	TX_LDO supply for powering up RF interface	3	5	5.5	V
RF interface transmitter						
$I_{DD(TVDD)}$	TVDD supply current	on pin TVDD_IN	-	-	250	mA

12. Thermal characteristics

Table 35. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a four-layer JEDEC PCB	40	°K/W

13. Characteristics

13.1 Static characteristics

Table 36. Static characteristics for RST_N input pin

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		1.1	-	$V_{DDP(VBUS)}$	V
V_{IL}	low-level input voltage		0	-	0.4	V
I_{IH}	high-level input current	$V_i = V_{DDP(VBUS)}$	-	-	1	µA
I_{IL}	low-level input current	V_i = 0 V	−1	-	-	µA
C_{in}	input capacitance		-	5	-	pF

Table 37. Static characteristics for IRQ input pin

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	V_{PVDD_IN} − 0.4	-	V_{PVDD_IN}	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
$R_{pull-down}$	extra pull down	extra pull-down is activated in HDP	0.45	-	0.8	MΩ

Table 38. Static characteristics for DWL_REQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage	V_{PVVD_IN} = 1.8 V	0.65 × V_{PVVD_IN}	-	-	V
V_{IL}	high-level input voltage	V_{PVVD_IN} = 1.8 V	-	-	0.35 × V_{PVVD_IN}	V
V_{IH}	high-level input voltage	V_{PVVD_IN} = 3.3 V	2	-	-	V
V_{IL}	high-level input voltage	V_{PVVD_IN} = 3.3 V	-	-	0.8	V
I_{IH}	high-level input current	V_I = PVDD_IN	-	-	1	µA
I_{IL}	low-level input current	V_I = 0 V	−1	-	-	µA
C_L	load capacitance		-	5	-	pF

13.1.1 GPIO static characteristics

Table 39. Static characteristics for GPIO1 to GPIO21

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	V_{PVDD_IN} − 0.4	-	V_{PVDD_IN}	V
V_{OL}	low-level output voltage	I_{OH} < 3 mA	0	-	0.4	V
V_{IH}	high-level input voltage	V_{PVDD_IN} = 3.3 V	2	-	-	V
		V_{PVDD_IN} = 1.8 V	0.65 × V_{PVDD_IN}	-	-	V

Table 39. Static characteristics for GPIO1 to GPIO21 *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	low-level input voltage	V_{PVDD_IN} = 3.3 V	-	-	0.8	V
		V_{PVDD_IN} = 1.8 V	-	-	0.35 × V_{PVDD_IN}	V
V_{hys}	hysteresis voltage	V_{PVDD_IN} = 1.8 V and V_{PVDD_IN} = 3.3 V	0.1 × V_{PVDD_IN}	-	-	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{PVDD_IN}; on-chip pull-up/pull-down resistors disabled	-	-	1000	nA
R_{pd}	pull-down resistance	V_{PVDD_IN} = 3.3 V	65	90	120	kΩ
		V_{PVDD_IN} = 1.8 V	65	90	120	kΩ
R_{pu}	pull-up resistance	V_{PVDD_IN} = 3.3 V	65	90	120	kΩ
		V_{PVDD_IN} = 1.8 V	65	90	120	kΩ
I_{OSH}	short circuit current output high	Drive high; cell connected to ground; V_{PVDD_IN} = 3.3 V	-	-	58	mA
		Drive low; cell connected to PVDD_IN; PVDD_IN = 1.8 V	-	-	30	mA
I_{OSL}	short circuit current output low	V_{OH} = V_{PVDD_IN} = 3.3 V	-	-	54	mA
		V_{OH} = V_{PVDD_IN} = 1.8 V	-	-	37	mA
I_{IL}	low-level input current	V_I = 0 V	−1	-	-	µA
I_{IH}	high-level input current	V_I = V_{PVDD_IN}	-	-	1	µA
I_{OH}	high-level output current	V_{OH} = V_{PVDD_IN}	-	-	3	mA
I_{OL}	low-level output current	V_{OL} = 0 V	-	-	3	mA

13.1.2 Static characteristics for I²C master

Table 40. Static characteristics for I²CM_SDA, I²CM_SCL - S

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	0.7 × $V_{PVDD\_M\_IN}$	-	$V_{PVDD\_M\_IN}$	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	10	pF
V_{IH}	High-level input voltage		0.7 × $V_{PVDD\_M\_IN}$	-	-	V
V_{IL}	low-level input voltage		-	-	0.3 × $V_{PVDD\_M\_IN}$	V
I_{IH}	high-level input current	V_I = $V_{PVDD\_M\_IN}$	-	-	1	µA
I_{IL}	low-level input current	V_I = 0 V	−1	-	-	µA
C_{in}	input capacitance		-	5	-	pF

13.1.3 Static characteristics for SPI master

Table 41. Static characteristics for SPIM_MOSI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	$V_{PVDD\_M\_IN}$ − 0.4	-	$V_{PVDD\_M\_IN}$	V
V_{OL}	low-level output voltage	I_{OL}< 3 mA	0	-	0.4	V
C_L	load Capacitance		-	-	20	pF

Table 42. Static characteristics for SPIM_NSS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	$V_{PVDD\_M\_IN}$ − 0.4	-	$V_{PVDD\_M\_IN}$	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load Capacitance		-	-	20	pF

Table 43. Static characteristics for SPIM_MISO

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 1.8 V	0.65 × $V_{PVDD\_M\_IN}$	-	-	V
V_{IL}	low-level input voltage	$V_{PVDD\_M\_IN}$ = 1.8 V	-	-	0.35 × $V_{PVDD\_M\_IN}$	V
V_{IH}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 3.3 V	2	-	-	V
V_{IL}	low-level input voltage	$V_{PVDD\_M\_IN}$ = 3.3 V	-	-	0.8	V
I_{IH}	high-level input current	V_i = $V_{PVDD\_M\_IN}$	-	-	1	µA
I_{IL}	low-level input current	V_i = 0 V	–1	-	-	µA
C_{in}	input capacitance		-	5	-	pF

Table 44. Static characteristics for SPI_SCLK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	$V_{PVDD\_M\_IN}$ − 0.4	-	$V_{PVDD\_M\_IN}$	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF

13.1.4 Static characteristics for host interface

Table 45. Static characteristics for ATX_ used as SPI_NSS, ATX_ used as I^2CADR0, ATX_ used as SPI_SCK, ATX_ used as SPI_MOSI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage	V_{PVDD_IN} = 1.8 V	0.65 × $V_{PVDD\_M\_IN}$	-	-	V
V_{IL}	low-level input voltage	V_{PVDD_IN} = 1.8 V	-	-	0.35 × $V_{PVDD\_M\_IN}$	V
V_{IH}	high-level input voltage	V_{PVDD_IN} = 3.3 V	2	-	-	V
V_{IL}	low-level input voltage	V_{PVDD_IN} = 3.3 V	-	-	0.8	V
I_{IH}	high-level input current	V_i = V_{PVDD_IN}	-	-	1	µA
I_{IL}	low-level input current	V_i = 0 V	–1	-	-	µA
C_{in}	input capacitance		-	5	-	pF

Table 46. Static characteristics of ATX_ used as I^2CSDA, ATX_ used as I^2CSCL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	0.7 × V_{PVDD_IN}	-	V_{PVDD_IN}	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	10	pF
V_{IH}	high-level input voltage		0.7 × V_{PVDD_IN}	-	-	V
V_{IL}	low-level input voltage		-	-	0.3 × V_{PVDD_IN}	V
I_{IH}	high-level input current	V_i = V_{PVDD_IN}	-	-	1	µA
I_{IL}	low-level input current	V_i = 0 V	–1	-	-	µA
C_{in}	Input capacitance		-	5	-	pF

Table 47. Static characteristics of ATX_ used as SPIMISO

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	V_{PVDD_IN} – 0.4	-	V_{PVDD_IN}	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF

Table 48. USB characteristics

Data are given for T_{amb} = –40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	0 V < V_i < 3.3 V	–10	-	10	µA
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS		4	-	5.5	V
V_{DI}	differential input sensitivity voltage	(D+) – (D–)	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		0.8	-	2	V
V_{OL}	low-level output voltage	for low-speed or full-speed; R_L of 1.5 kΩ to 3.6 V	-	-	0.3	V
V_{OH}	high-level output voltage	driven; for low- speed or full-speed; R_L of 15 kΩ to GND	2.8	-	V_{PVDD_IN}	V
C_{trans}	transceiver capacitance	pin to GND	-	15		pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	28	-	44	Ω
V_{CRS}	output signal crossover voltage		1.3	-	2	V

Table 49. Static characteristics of HSU_TX and HSU RTS pin

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	high-level output voltage	I_{OH} < 3 mA	V_{PVDD_IN} − 0.4	-	V_{PVDD_IN}	V
V_{OL}	low-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF

Table 50. Static characteristics of HSU_RX, HSU_CTS

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 1.8 V	0.65 × V_{PVDD_IN}	-	-	V
V_{IL}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 1.8 V	-	-	0.35 × V_{PVDD_IN}	V
V_{IH}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 3.3 V	2	-	-	V
V_{IL}	high-level input voltage	$V_{PVDD\_M\_IN}$ = 3.3 V	-	-	0.8	V
I_{IH}	high-level input current		-	-	1	µA
I_{IL}	low-level input current		−1	-	-	µA
C_L	load capacitance		-	5	-	pF

13.1.5 Clock static characteristics

Table 51. Static characteristics of XTAL pin (XTAL1, XTAL2)

T_{amb} = −40 °C to +85 °C

Symbol	Parameter[1]	Conditions	Min	Typ[2]	Max	Unit
Input clock characteristics on XTAL1 when using PLL						
V~i(p-p)	peak-to-peak input voltage		0.2	-	1.65	V
XTAL pin characteristics XTAL PLL input						
I_{IH}	high-level input current	V_i = V_{DD}	-	-	1	µA
I_{IL}	low-level input current	V_i = 0 V	−1	-	-	µA
V_i	input voltage		-	-	V_{DD}	V
V_{AL}	input voltage amplitude		200	-	-	mV
C_{in}	input capacitance	all power modes	-	2	-	pF
Pin characteristics for 27.12 MHz crystal oscillator						
C_{in}	input capacitance	pin XTAL1	-	2	-	pF
C_{in}	input capacitance	pin XTAL2	-	2	-	pF

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

13.1.6 Static characteristics - power supply

Table 52. Static characteristics for power supply

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDP(VBUSP)}$	power supply current on pin VBUSP	external supply current for contact interface, in operating mode	-	-	200	mA
pin supply: PVDD_LDO						
$V_{O(LDO)}$	LDO output voltage	$V_{DDP(VBUS)}$ >= 4.0 V, $I_{PVDDOUT}$ <= 30 mA	3	3.3	3.6	V
$I_{DD(PVDD\_OUT)}$	maximum supply current	for pin PVDD_OUT	-	-	30	mA
pin supply for host interface and GPIOs (on pin PVDD_IN)						
$I_{DD(PVDD)}$	PVDD supply current		-	-	25	mA
pin supply for master interfaces (on pin PVDD_M_IN)						
$I_{DD(PVDD)}$	PVDD supply current		-	-	25	mA
contactless interface: TX_LDO (pins VUP_TX, TVDD_OUT)						
$V_{I(LDO)}$	LDO input voltage		3	-	5.5	V
$I_{L(LDO)(max)}$	maximum LDO load current		-	-	180	mA
$V_{O(LDO)}$	LDO output voltage	DC output voltage (target: 3.0 V) 5.5 V > $V_{I(LDO)}$ > 3.3 V	2.8	3	3.25	V
		DC output voltage (target: 3.0 V) 3.3 V > $V_{I(LDO)}$ > 2.7 V	-	$V_{I(LDO)}$ − 0.3	-	V
		DC output voltage (target: 3.3 V) 5.5 V > $V_{I(LDO)}$ > 3.6 V	3.1	3.3	3.55	V
		DC output voltage (target: 3.3 V) 3.6 V > $V_{I(LDO)}$ > 2.7 V	-	$V_{I(LDO)}$ − 0.3	-	V
		DC output voltage (target: 3.6 V) 5.5 V > $V_{I(LDO)}$ > 3.9 V	3.4	3.6	3.95	V
		DC output voltage (target: 3.6 V) 3.9 V > $V_{I(LDO)}$ > 2.7 V	-	$V_{I(LDO)}$ − 0.3	-	V
		DC output voltage (target: 4.5 V) 5.5 V > $V_{I(LDO)}$ > 5.0 V	4.3	4.5	4.9	V
		DC output voltage (target: 4.7 V) 5.5 V > $V_{I(LDO)}$ > 5.0 V	4.55	4.75	5.2	V
$I_{O(LDO)}$	LDO output current	$V_{I(LDO)}$ = 5.5 V	-	-	180	mA
Contactless interface: RF transmitter (on pin TVDD_IN)						
$I_{DD(TVDD)}$	TVDD supply current	maximum current supported by the RF transmitter	-	-	250	mA
Contact Interface: smart card power supply (pin VCC)						
C_{dec}	decoupling capacitance	connected on pin VCC (220 nF + 220 nF 10 %)	396	570	1000	nF

Table 52. Static characteristics for power supply *...continued*

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	class A; I_{CC} < 60 mA	4.75	5	5.25	V
		class B; I_{CC} < 50 mA	2.85	3	3.15	V
		class C; I_{CC} < 30 mA	1.71	1.8	1.89	V
		class A; current pulses of 40 nA with I_{CC} < 200 mA, t_w < 400 ns	4.6	-	5.4	V
		class B; current pulses of 40 nA with I_{CC} < 200 mA, t_w < 400 ns	2.76	-	3.24	V
		class C; current pulses of 12 nA with I_{CC} < 200 mA, t_w < 400 ns	1.66	-	1.94	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	350	mV
SR	slew rate on pin VCC	5 V, class A cards	0.02	-	0.025	V/µs
		3 V, class B cards	0.012	-	0.015	V/µs
		1.8 V, class C cards	0.0072	-	0.009	V/µs
I_{CC}	supply current	class A	-	-	60	mA
		class B	-	-	55	mA
		class C	-	-	35	mA
		Pin VCC shorted to ground	-	-	110	mA
Contact interface: DC-to-DC converter						
V_{SAP}	SAP (DC-to-DC converter) - high-level output voltage	$V_{DDP(VBUSP)}$ = 5 V, V_{CC} = 5 V; I_{CC} < 60 mA DC	-	-	9	V
		$V_{DDP(VBUSP)}$ = 5 V, V_{CC} = 3 V; I_{CC} < 55 mA DC	-	-	5	V
		$V_{DDP(VBUSP)}$ = 5 V, V_{CC} = 1.8 V; I_{CC} < 35 mA DC	-	-	5	V
		$V_{DDP(VBUSP)}$ = 3.3 V, V_{CC} = 5 V; I_{CC} < 60 mA DC	-	-	9	V
		$V_{DDP(VBUSP)}$ = 3.3 V, V_{CC} = 3 V; I_{CC} < 55 mA DC	-	-	9	V
		$V_{DDP(VBUSP)}$ = 3.3 V, V_{CC} = 1.8 V; I_{CC} < 35 mA DC	-	-	3.3	V
V_{UP}	V_{UP} - high-level output voltage	Class A; $V_{DDP(VBUSP)}$ = 3 V to 5 V, I_{CC} < 60 mA	5.35	-	5.9	V
		Class B; I_{CC} < 55 mA	3.53	-	5.5	V
		Class C, $V_{DDP(VBUSP)}$ = 2.7 V to 5.5 V, I_{CC} < 35 mA DC	2.4	-	5.5	V
C_{SAPSAM}	DC-to-DC converter capacitance	connected between SAP and SAM with $V_{DDP(VBUSP)}$ = 3 V	300	470	600	nF
C_{VUP}	DC-to-DC converter capacitance	connected on pin VUP	1.5	2.7	4.7	µF
Voltage detector for the DC-to-DC converter						
V_{det}	detection voltage	on pin VBUSP for doubler selection, follower/doubler for class B card	3.775	3.9	4.2	V

Table 53. Static characteristics for voltage monitors

T_{amb} = −40 °C to +80 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(th)HL}$	negative-going threshold voltage	VBUS monitor;				
		set to 2.3 V	2.15	2.3	2.45	V
		set to 2.7 V	2.6	2.75	2.95	V
		set to 4.0 V	3.6	3.8	3.9	V
V_{hys}	hysteresis voltage	VBUS monitor				
		set to 2.3 V	100	150	200	mV
		set to 2.7 V	100	150	200	mV
		set to 4.0 V	40	80	100	mV
$V_{(th)HL}$	negative-going threshold voltage	VBUSP monitor				
		set to 2.7 V	2.45	2.56	2.65	V
		set to 3.0 V	2.68	2.825	2.95	V
		set to 3.9 V	3.7	3.9	4.1	V
V_{hys}	hysteresis voltage	VBUSP monitor				
		set to 2.7 V	12	25	35	mV
		set to 3.0 V	14	30	40	mV
		set to 3.9 V	20	35	55	mV

13.1.7 Static characteristics for power modes

Table 54. Static characteristics for power modes

T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDP(VBUS)}$	power supply current on pin VBUS	active mode; $V_{DDP(VBUS)}$ = 5.5 V, external PVDD, external TVDD, all IP clocks disabled code while(1){} executed from flash;	-	6.5	-	mA
		active mode; $V_{DDP(VBUS)}$ = 5.5 V, external PVDD, external TVDD, all IP clocks enabled code while(1){} executed from flash;	-	8.5	-	mA
		suspend mode; $V_{DDP(VBUS)}$ = 5.5 V, external PVDD, T = 25 °C	-	120	250	µA
		V_{BUS} = 5.5 V, T = 25 °C, internal PVDD LDO, including D+ and D− pull-up	-	360	440	µA
		standby mode; $V_{DDP(VBUS)}$ = 3.3 V; external PVDD supply; T_{amb} = 25 °C	-	18	-	µA
		standby mode; $V_{DDP(VBUS)}$ = 5.5 V; $V_{internal}$ PVDD supply; T_{amb} = 25 °C	-	55	-	µA
		hard power down; $V_{DDP(VBUS)}$ = 5.5 V; RST_N = 0 V; T_{amb} = 25 °C	-	12	18	µA

13.1.8 Static characteristics for contact interface

Table 55. Static characteristics for contact interface

T_{amb} = −40 °C to +80 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Data lines (pins IO, AUX1, AUX2)						
V_o	output voltage on pin IO	inactive mode, no load	0	-	0.1	V
		inactive mode, $I_{I/O}$ = 1 mA	0	-	0.3	V
V_{OL}	low-level output voltage	pin IO Configured as output I_{OL} = 1 mA (class A,B), 500 µA (class C)	0	-	0.15 × V_{CC}	V
		pin IO configure as output, I_{OL} < 15 mA	0	-	0.4	V
V_{OH}	high-level output voltage	pin IO configure as output, I_{OH} < −200 µA, V_{CC} = 5 V, 3 V and 1.8 V; active pull-up	0.9 × V_{CC}	-	V_{CC}	V
		pin IO configure as output, I_{OH} < −20 µA; V_{CC} = 1.8 V	0.8 × V_{CC}	-	V_{CC}	V
		pin IO configure as output, I_{OH} < 15 mA	0	-	0.4	V
V_{IL}	low-level input voltage	pin IO configure as input	0	-	0.2 × V_{CC}	V

Table 55. Static characteristics for contact interface *…continued*

T_{amb} = −40 °C to +80 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	high-level input voltage		0.6 × V_{CC}	-	V_{CC}	V
V_{hys}	hysteresis voltage	on pin IO	20	75	120	mV
I_{IL}	low-level input current	on pin IO; V_{IL} = 0 V	-	-	750	µA
I_{LH}	high-level leakage current	on pin IO; V_{IH} = V_{CC}	-	-	10	µA
R_{pu}	pull-up resistance	connected to V_{CC}	7	10	13	kΩ
Reset output to the card						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o = 1 mA	0	-	0.3	V
V_{OL}	low-level output voltage	I_{OL} = 200 µA, V_{CC} = 5 V and V_{CC} = 3 V	0	-	0.3	V
		I_{OL} = 200 µA, V_{CC} = 1.8 V	0	-	0.1 × V_{CC}	V
V_{OH}	high-level output voltage	I_{OH} = −200 µA	0.9 × V_{CC}	-	V_{CC}	V
Clock output to the card						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o = 1 mA	0	-	0.3	V
V_{OL}	low-level output voltage	I_{OL} = 200 µA	0	-	minimum (0.1 × V_{CC} ; 0.3)	V
V_{OH}	high-level output voltage	I_{OH} = −200 µA	0.9 × V_{CC}	-	V_{CC}	V
Card presence input						
V_{IL}	low-level input voltage		−0.3	-	0.3 × V_{PVDD_IN}	V
V_{IH}	high-level input voltage		0.7 × V_{PVDD_IN}	-	V_{PVDD_IN} + 0.3	V
V_{hys}	hysteresis voltage		0.03 × V_{PVDD_IN}	-	-	V
I_{LL}	low-level leakage current	V_{IL} = 0	-	-	1	µA
I_{LH}	high-level leakage current	V_{IH} = V_{PVDD_IN}	-	-	5	µA

13.1.9 Static characteristics RF interface

Table 56. Static characteristics for RF interface

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
pins ANT1 and ANT2						
Z	impedance	between ANT1 and ANT2; low impedance	-	10	17	Ω
pins RXN and RXP						
$V_{i(dyn)}$	dynamic input voltage	on pins RXN and RXP	-	-	V_{DD} − 0.05	V
C_{in}	input pin capacitance	on pins RXN and RXP	-	12	-	pF
Z	impedance	between pins RX to VMID; reader, card emulation and P2P modes	0	-	15	kΩ
V_{det}	detection voltage	card emulation and target modes; configuration for 19 mV threshold	-	-	30	$mV_{(p-p)}$
pins TX1 and TX2						
V_{OH}	high-level output voltage	pins TX1 and TX2; T_{VDD_IN} = 3.1 V and I_{OH} = 30 mA	V_{TVDD_IN} − 150	-	-	mV
V_{OL}	low-level output voltage	pins TX1 and TX2; T_{VDD_IN} = 3.1; I_{TX} = 30 mA	-	-	200	mV
R_{OL}	low-level output resistance	V_{TX} = V_{TVDD} − 100 mV; CWGsN = 01h	-	-	80	Ω
		V_{TX} = V_{TVDD} − 100 mV; CWGsN = 0Fh	-	-	10	Ω
R_{OH}	high-level output resistance	V_{TX} = V_{TVDD} − 100 mV	-	-	10	Ω

13.2 Dynamic characteristics

Table 57. Dynamic characteristics for IRQ input pin

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	high speed; C_L = 12 pF; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		high speed; C_L = 12 pF; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
t_f	fall time	slow speed; C_L = 12 pF; V_{PVDD_IN} = 3.3 V	3	-	10	ns
		slow speed; C_L = 12 pF; V_{PVDD_IN} = 1.8 V	2	-	10	ns

Table 57. Dynamic characteristics for IRQ input pin *...continued*

Data are given for T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	high speed: C_L = 12 pF; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		high speed: C_L = 12 pF; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
t_r	rise time	slow speed: C_L = 12 pF; V_{PVDD_IN} = 3.3 V	3	-	10	ns
		slow speed: C_L = 12 pF; V_{PVDD_IN} = 1.8 V	2	-	10	ns

13.2.1 Flash memory dynamic characteristics

Table 58. Dynamic characteristics for flash memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	programming time	1 page (64 bytes); slow clock	-	-	2.5	ms
N_{Endu}	endurance		200	500	-	cycles
t_{ret}	retention time		-	20	-	years

13.2.2 EEPROM dynamic characteristics

Table 59. Dynamic characteristics for EEPROM

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	programming time	1 page (64 bytes)	-	2.8	-	ms
N_{Endu}	endurance		300	500	-	kcycles
t_{ret}	retention time		-	20	-	years

13.2.3 GPIO dynamic characteristics

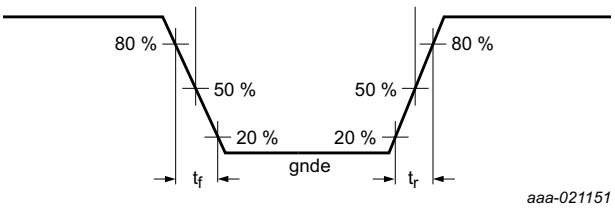


Fig 35. Output timing measurement condition for GPIO

Table 60. Dynamic characteristics for GPIO1 to GPIO21

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	rise time	C_L = 12 pF; PVDD = 1.8 V; slow speed	2.0	10.0	ns
		C_L = 12 pF; PVDD = 1.8 V; fast speed	1.0	3.5	ns
		C_L = 12 pF; PVDD = 3.3 V; slow speed	3.0	10.0	ns
		C_L = 12 pF; PVDD = 3.3 V; fast speed	1.0	3.5	ns
t_f	fall time	C_L = 12 pF; PVDD = 1.8 V; slow speed	2.0	10.0	ns
		C_L = 12 pF; PVDD = 1.8 V; fast speed	1.0	3.5	ns
		C_L = 12 pF; PVDD = 3.3 V; slow speed	3.0	10.0	ns
		C_L = 12 pF; PVDD = 3.3 V; fast speed	1.0	3.5	ns

13.2.4 Dynamic characteristics for I²C master

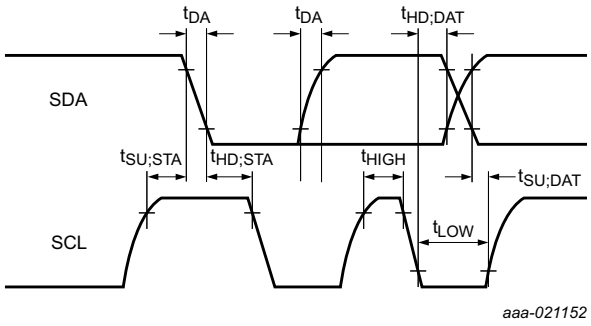


Fig 36. I²C-bus pins clock timing

Table 61. Timing specification for fast mode plus I²C

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	fast mode plus; C_b < 100 pF	0	1	MHz
$t_{SU;STA}$	set-up time for a (repeated) START condition	fast mode plus; C_b < 100 pF	260	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	fast mode plus; C_b < 100 pF	260	-	ns
t_{LOW}	low period of the SCL clock	fast mode plus; C_b < 100 pF	500	-	ns
t_{HIGH}	high period of the SCL clock	fast mode plus; C_b < 100 pF	260	-	ns
$t_{SU;DAT}$	data set-up time	fast mode plus; C_b < 100 pF	50	-	ns
$t_{HD;DAT}$	data hold time	fast mode plus; C_b < 100 pF	0	-	ns
$t_{r(SDA)}$	SDA rise time	fast mode plus; C_b < 100 pF	-	120	ns
$t_{f(SDA)}$	SDA fall time	fast mode plus; C_b < 100 pF	-	120	ns
V_{hys}	hysteresis of schmitt trigger inputs	fast mode plus; C_b < 100 pF	0.1 × $V_{PVDD\_M\_IN}$	-	V

Table 62. Timing specification for fast mode I^2C

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	fast mode; C_b < 400 pF	0	400	kHz
$t_{SU;STA}$	set-up time for a (repeated) START condition	fast mode; C_b < 400 pF	600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	fast mode; C_b < 400 pF	600	-	ns
t_{LOW}	low period of the SCL clock	fast mode; C_b < 400 pF	1.3	-	µs
t_{HIGH}	high period of the SCL clock	fast mode; C_b < 400 pF	600	-	ns
$t_{SU;DAT}$	data set-up time	fast mode; C_b < 400 pF	100	-	ns
$t_{HD;DAT}$	data hold time	fast mode; C_b < 400 pF	0	900	ns
$t_{r(SDA)}$	SDA rise time	fast mode plus; C_b < 100 pF	30	250	ns
$t_{f(SDA)}$	SDA fall time	fast mode plus; C_b < 100 pF	30	250	ns
V_{hys}	hysteresis of schmitt trigger inputs	fast mode; C_b < 400 pF	0.1 × V_{PVDD_IN}	-	V

13.2.5 Dynamic characteristics for SPI

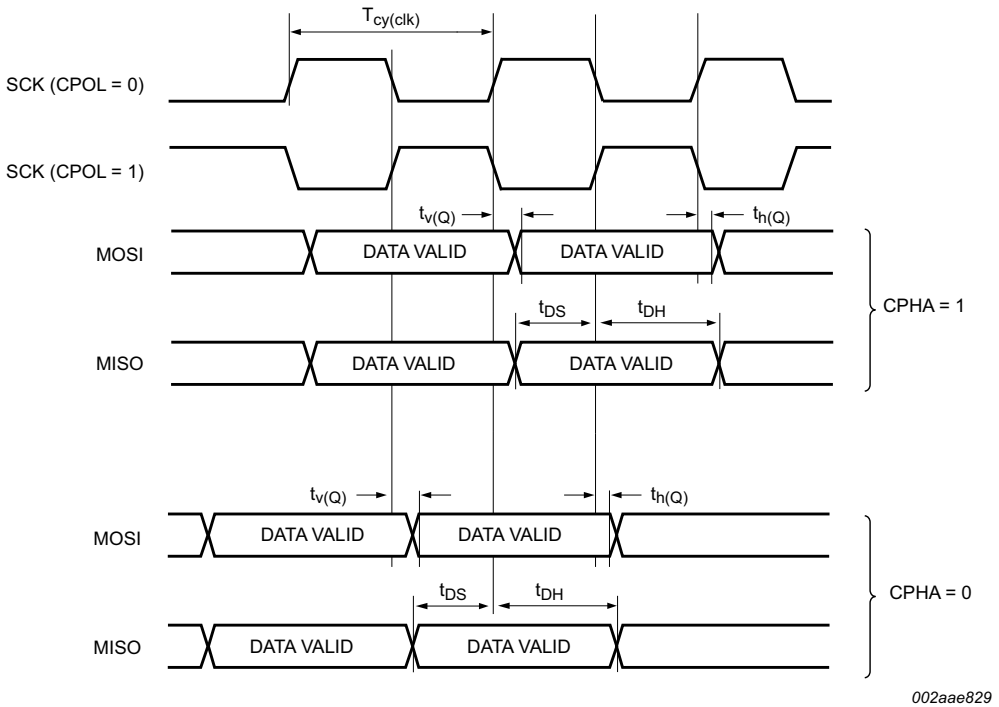


Fig 37. SPI master timing

Table 63. Dynamic characteristics and Timing specification for SPI master interface

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SCK frequency	controlled by the host	0	6.78	MHz
t_{DS}	data set-up time		25	-	ns
t_{DH}	data hold time		25	-	ns
$t_{v(Q)}$	data output valid time		-	25	ns
$t_{h(Q)}$	data output hold time		-	25	ns
Dynamic characteristics for SPI_SCLK, SPIM_NSS, SPIM_MOSI					
t_f	fall time	C_L = 12 pF; high speed; V_{PVDD_IN} = 3.3 V	1	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 3.3 V	3	10	ns
t_r	rise time	C_L = 12 pF; high speed; V_{PVDD_IN} = 3.3 V	1	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 3.3 V	3	10	ns
t_f	fall time	C_L = 12 pF; high speed; V_{PVDD_IN} = 1.8 V	1	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 1.8 V	2	10	ns
t_r	rise time	C_L = 12 pF; high speed; V_{PVDD_IN} = 1.8 V	1	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 1.8 V	2	10	ns

13.2.6 Dynamic characteristics of host interface

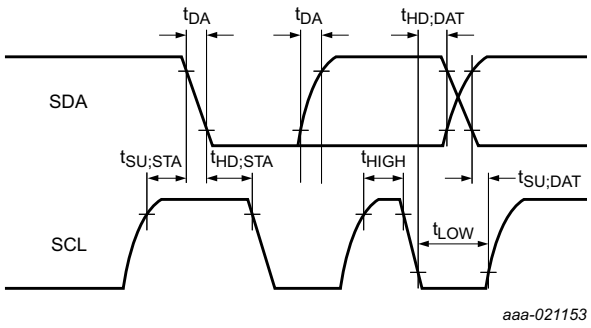


Fig 38. I^2C-bus pins clock timing

Table 64. Timing specification for I2C high speed

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Max	Unit
f_{scl}	clock frequency	high speed; C_b < 100 pF	0	3.4	MHz
$t_{SU;STA}$	set-up time for a (repeated) START condition	high speed; C_b < 100 pF	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	high speed; C_b < 100 pF	160	-	ns
t_{LOW}	low period of the SCL clock	high speed; C_b < 100 pF	160	-	ns
t_{HIGH}	high period of the SCL clock	high speed; C_b < 100 pF	60	-	ns
$t_{SU;DAT}$	data set-up time	high speed; C_b < 100 pF	10	-	ns
$t_{HD;DAT}$	data hold time	high speed; C_b < 100 pF	0	-	µs

Table 64. Timing specification for I2C high speed

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(SDA)}$	SDA rise time	high speed; C_b < 100 pF	10	80	ns
$t_{f(SDA)}$	SDA fall time	high speed; C_b < 100 pF	10	80	ns
V_{hys}	hysteresis of schmitt trigger inputs	high speed; C_b < 100 pF	0.1 × V_{PVDD_IN}	-	V

Table 65. Dynamic characteristics for the I²C slave interface : ATX_B used as I²C_SDA, ATX_A used as I²C_SCL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	C_L = 100 pF, $R_{pull-up}$ = 2 K, standard and fast mode	30	-	250	ns
		C_L = 100 pF, $R_{pull-up}$ = 1 K, high speed	10	-	80	ns
t_r	rise time	C_L = 100 pF, $R_{pull-up}$ = 2 K, standard and fast mode	30	-	250	ns
		C_L = 100 pF, $R_{pull-up}$ = 1 K, high speed	10	-	100	ns

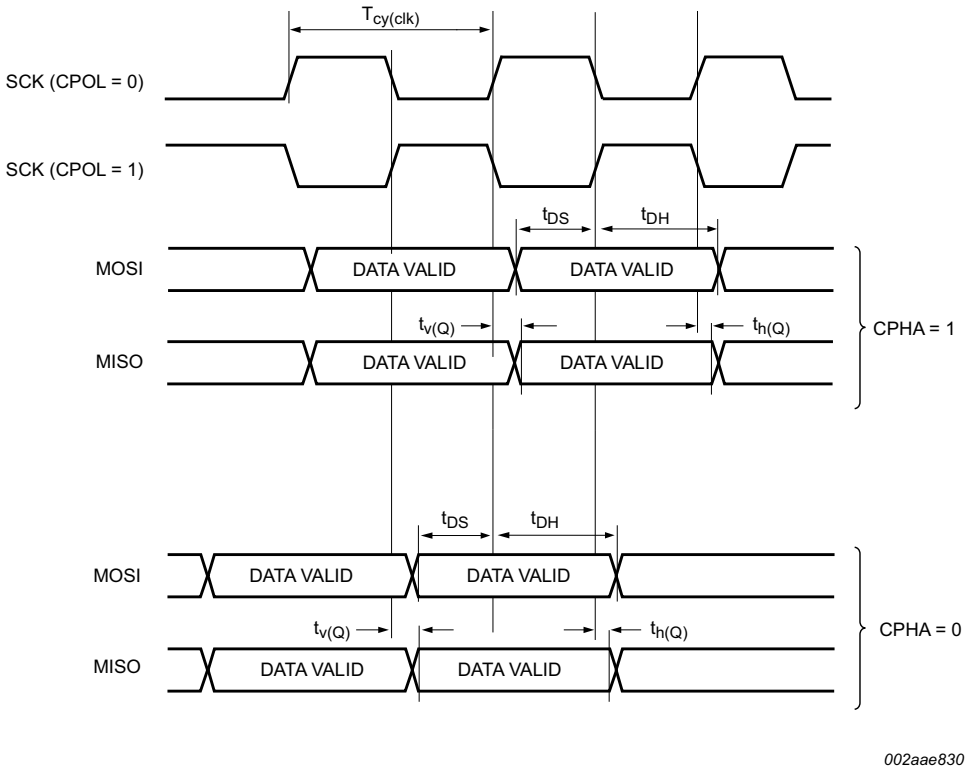


Fig 39. SPI slave timings

Table 66. Dynamic characteristics for SPI slave interface

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SCK frequency	controlled by the host	0	7	MHz
t_{DS}	data set-up time		25	-	ns
t_{DH}	data hold time		25	-	ns
$t_{v(Q)}$	data output valid time		-	25	ns
$t_{h(Q)}$	data output hold time		-	25	ns

Table 67. Dynamic characteristics for SPI slave interface: ATX_C as SPI_MISO

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	C_L = 12 pF; high speed; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 3.3 V	3	-	10	ns
t_r	rise time	C_L = 12 pF; high speed; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 3.3 V	3	-	10	ns
t_f	fall time	C_L = 12 pF; high speed; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 1.8 V	2	-	10	ns
t_r	rise time	C_L = 12 pF; high speed; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
		C_L = 12 pF; slow speed; V_{PVDD_IN} = 1.8 V	2	-	10	ns

Table 68. Dynamic characteristics for HSUART ATX_ as HSU_TX, ATX_ as HSU_RTS

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
t_f	fall time	high speed; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		slow speed; V_{PVDD_IN} = 3.3 V	3	-	10	ns
t_r	rise time	high speed; V_{PVDD_IN} = 3.3 V	1	-	3.5	ns
		slow speed; V_{PVDD_IN} = 3.3 V	3	-	10	ns
t_f	fall time	high speed; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
		slow speed; V_{PVDD_IN} = 1.8 V	2	-	10	ns
t_r	rise time	high speed; V_{PVDD_IN} = 1.8 V	1	-	3.5	ns
		slow speed; V_{PVDD_IN} = 1.8 V	2	-	10	ns

[1] C_L=12 pF maximum.

Table 69. Dynamic characteristics for USB interface

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to VBUS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	109	%
V_{CRS}	output signal crossover voltage		1.3	-	2	V
t_{FEOPT}	source SE0 interval of EOP	T = 25 °C; see Figure 40	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	T = 25 °C; see Figure 40	−2	-	+5	ns
t_{JR1}	receiver jitter to next transition	T = 25 °C	−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %; T = 25 °C	−9	-	+9	ns
t_{FEOPR}	receiver SE0 interval of EOP	must accept as EOP; see Figure 40	82	-	-	ns

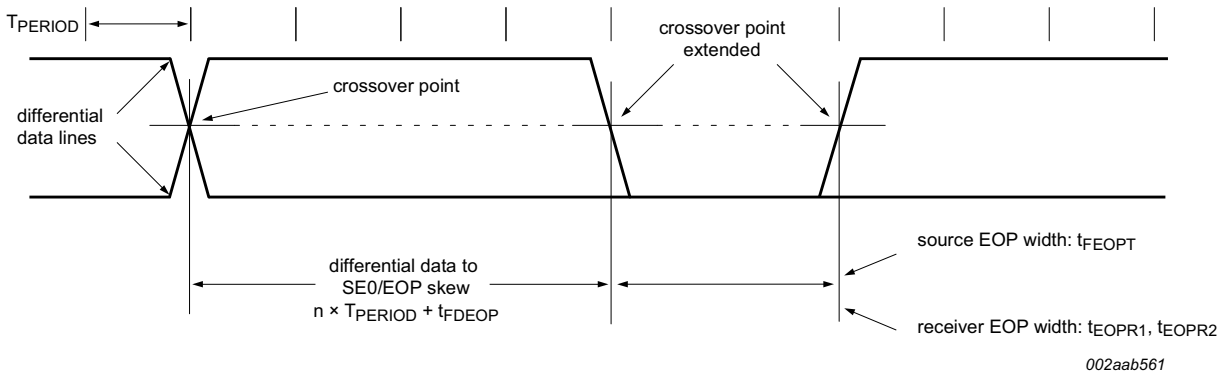


Fig 40. USB interface differential data-to-EOP transition skew and EOP width

13.2.7 Clock dynamic characteristics

Table 70. Dynamic characteristics for internal oscillators

T_{amb} = −40 °C to +80 °C

Symbol	Parameter[1]	Conditions	Min	Typ[2]	Max	Unit
low frequency oscillator						
$f_{osc(int)}$	internal oscillator frequency	$V_{DDP(VBUS)}$ = 3.3 V	300	365	400	kHz
high frequency oscillator						
$f_{osc(int)}$	internal oscillator frequency	$V_{DDP(VBUS)}$ = 3.3 V	18	20	22	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

Table 71. Dynamic characteristics for PLL

T_{amb} = –40 °C to +80 °C

Symbol	Parameter[1]	Conditions	Min	Typ[2]	Max	Unit
Δf	frequency deviation	deviation added to CLK_XTAL1 frequency on RF frequency generated using PLL	–50	-	50	ppm

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

13.2.8 Dynamic characteristics for power supply

Table 72. Dynamic characteristics for power supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC-to-DC internal oscillator						
$f_{osc(int)}$	internal oscillator frequency	DC-to-DC converter	-	3.39	-	MHz

13.2.9 Dynamic characteristics for boot and reset

Table 73. Dynamic characteristics for boot and reset

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wL(RST\_N)}$	RST_N Low pulse width time		10	-	-	µs
t_{boot}	boot time	external PVDD supply; supply is stable at reset	-	-	320	µs
		internal PVDD_LDO supply; supply is stable at reset	-	-	2.2	ms

13.2.10 Dynamics characteristics for power mode

Table 74. Power modes - wake-up timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{wake}	wake-up time	stand-by mode [1]	-	-	500	µs
		suspend mode [1]	-	-	150	µs

[1] Wake-up timings are measured from the wake-up event to the point in which the user application code reads the first instruction.

13.2.11 Dynamic characteristics for contact interface

Table 75. Dynamic characteristics for contact interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Data lines (pins IO, AUX1, AUX2)						
f_{data}	data rate	on data lines	-	-	1.5	Mbps
$t_{r(i)}$	input rise time	from V_{IL} maximum to V_{IH} minimum	-	-	1.2	µs
$t_{f(i)}$	input fall time	from V_{IL} maximum to V_{IH} minimum	-	-	1.2	µs
$t_{r(o)}$	output rise time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	µs
$t_{f(o)}$	output fall time	C_L < = 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	µs

Table 75. Dynamic characteristics for contact interface *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(pu)}$	pull-up pulse width		-	295	-	ns
Reset output to the card						
t_r	rise time	C_L = 100 pF	-	-	0.1	µs
t_f	fall time	C_L = 100 pF	-	-	0.1	µs
Clock output to the card (CLK)						
t_r	rise time	C_L = 30 pF; f_{CLK} = 10 MHz [1]	-	-	8	ns
t_r	rise time	C_L = 30 pF; f_{CLK} = 5 MHz [1]	-	-	16	ns
t_f	fall time	C_L = 30 pF; f_{CLK} = 10 MHz [1]	-	-	8	ns
t_f	fall time	C_L = 30 pF; f_{CLK} = 5 MHz [1]	-	-	16	ns
f_{CLK}	frequency on pin CLK	operational	0	-	13.56	MHz
δ	duty cycle	C_L = 30 pF [1]	45	-	55	%
SR	slew rate	rise and fall; C_L = 30 pF; V_{CC} = +5 V	0.2	-	-	V/ns
		rise and fall; C_L = 30 pF; V_{CC} = +3 V	0.12	-	-	V/ns
		rise and fall; C_L = 30 pF; V_{CC} = +1.8 V	0.072	-	-	V/ns
PRESN						
t_{deb}	debounce time	on pin PRESN	-	6	-	ms
Timings						
t_{act}	activation time	see Figure 9; T = 25 °C	11	-	22	ms
t_{deact}	deactivation time	see Figure 10; T = 25 °C	60	100	250	µs

[1] The transition time and duty factor definitions are shown in Figure 41.

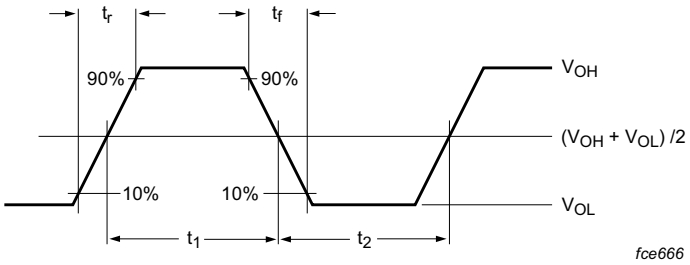


Fig 41. Definition of output and input transition times

14. Marking

Table 76. Marking codes

Type number	Marking code
PN7462	
Line A	PN7462AU-00
Line B	Diffusion Batch ID, Assembly Sequence ID
Line C	Characters: Diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: 1. Diffusion center code: Z 2. Assembly center code: S 3. RHF-2006 indicator: D “Dark Green” 4. Year code (Y) 1 5. Year code (Y) 2 6. Week code (W) 1 7. Week code (W) 2 8. HW version
Line D	Empty
Line E	Empty

14.1 Package marking drawing

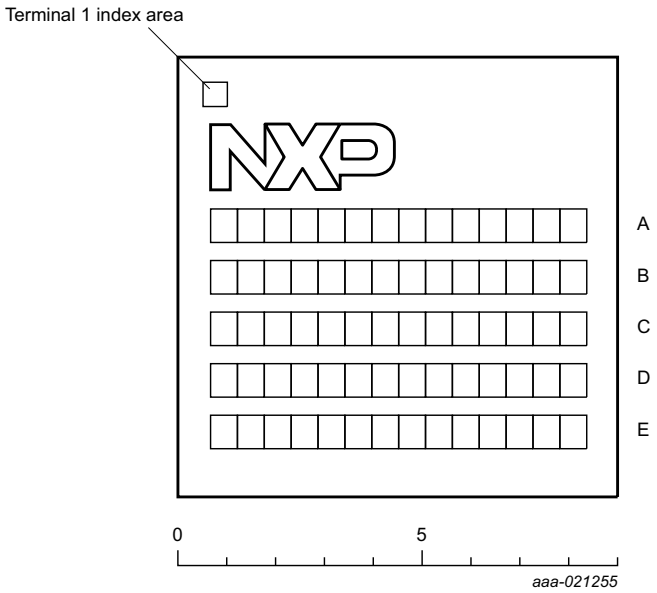
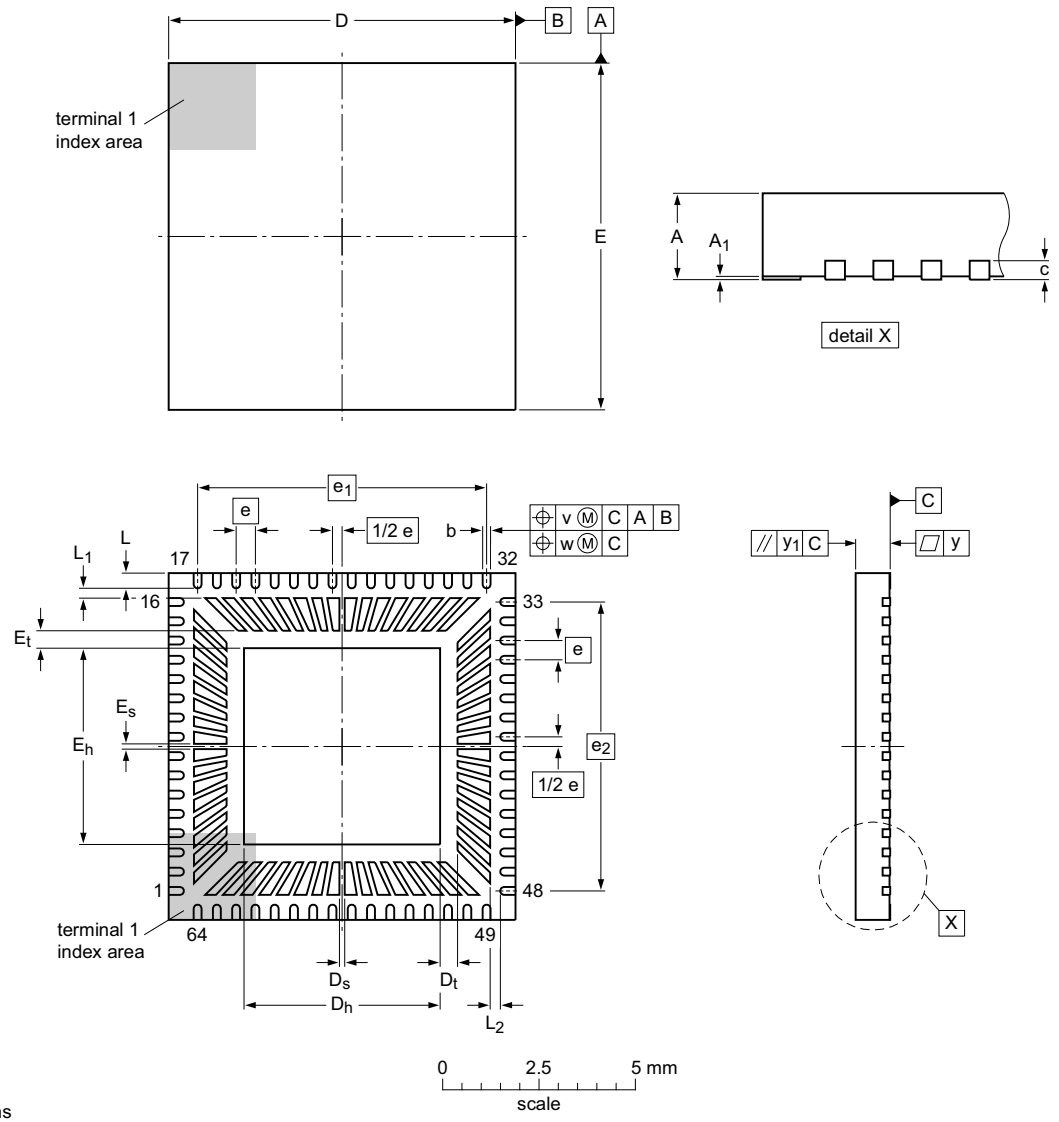


Fig 42. Marking PN7462 in HVQFN64

15. Package outline

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm **SOT804-4**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	D_s	D_t	$E^{(1)}$	E_h	E_s	E_t	e	e_1	e_2	L	L_1	L_2	v	w	y	y_1
mm	max	1.00	0.05	0.30	0.2	9.1	5.25	0.19	0.50	9.1	5.25	0.19	0.50	0.5	7.5	7.5	0.5	0.25	0.25	0.1	0.05	0.05	0.1
	nom	0.85	0.02	0.21		9.0	5.10	0.14	0.45	9.0	5.10	0.14	0.45				0.4						
	min	0.80	0.00	0.18		8.9	4.95	0.09	0.40	8.9	4.95	0.09	0.40				0.3						

Note

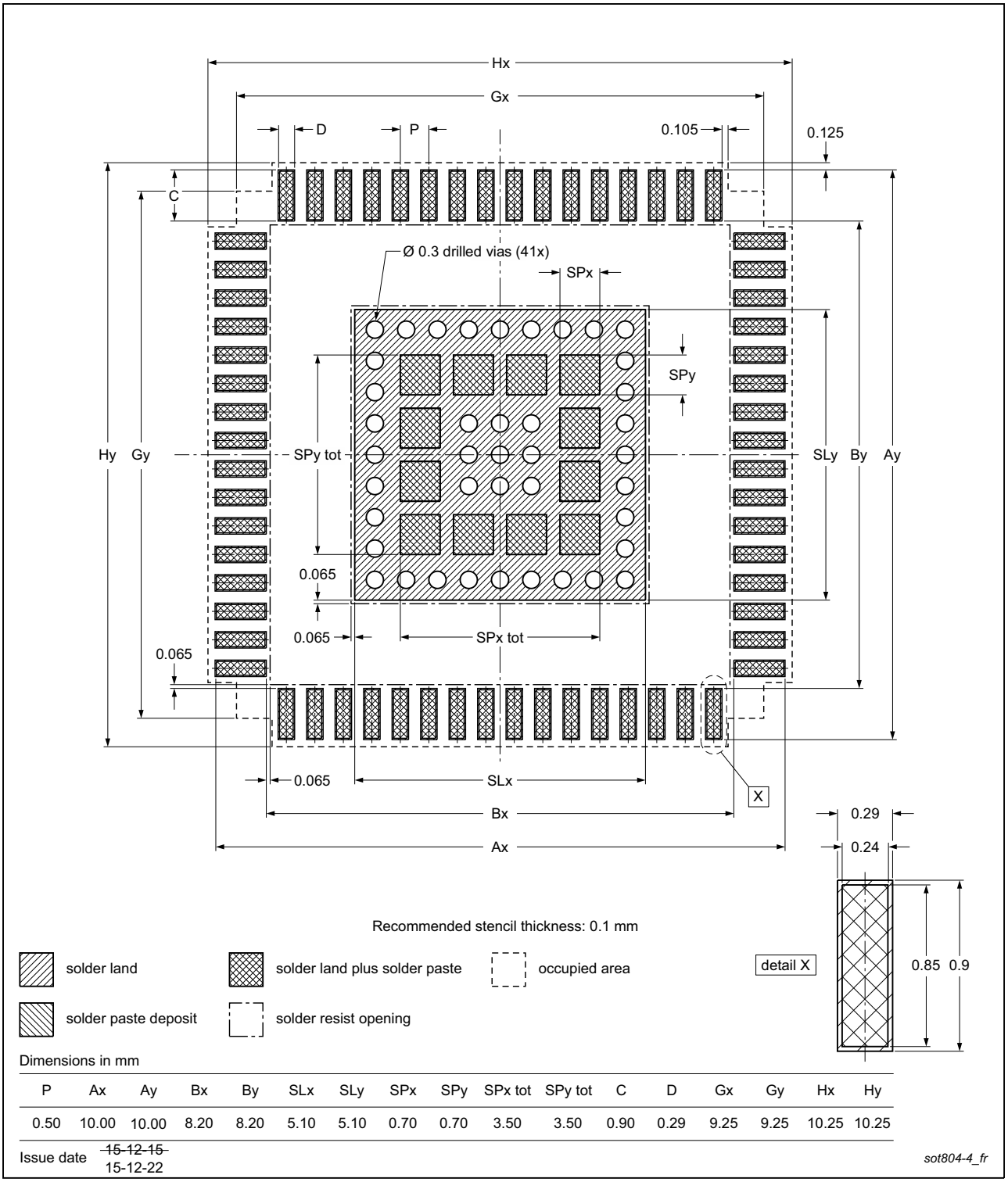
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot804-4_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT804-4	---	---	---		~~10-05-26~~ 10-05-27

Fig 43. Package outline HVQFN64

Footprint information for reflow soldering of HVQFN64 package **SOT804-4**



Dimensions in mm

P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	Gx	Gy	Hx	Hy
0.50	10.00	10.00	8.20	8.20	5.10	5.10	0.70	0.70	3.50	3.50	0.90	0.29	9.25	9.25	10.25	10.25

Issue date ~~15-12-15~~ 15-12-22

sot804-4_fr

Fig 44. Footprint information for reflow soldering of HVQFN64

16. Packing information

Moisture Sensitivity Level (MSL) evaluation has been performed according to JEDEC J-STD-020C. MSL for this package is level 3 which means 260 °C Pb-free convection reflow maximum temperature peak.

Dry packing is required with following floor conditions: 168 hours out of bag floor life at maximum ambient temperature 30 °C/60 % RH.

For information on packing, refer to the PIP relating to this product at http://www.nxp.com.

17. Abbreviations

Table 77. Abbreviations

Acronym	Description
ADC	Analog to Digital Convertor
ALM	Active Load Modulation
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying
CLIF	ContactLess InterFace
CT	Contact InTerface
CRC	Cyclic Redundancy Check
DPC	Dynamic Power Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO	General-Purpose Input Output
I^2C	Inter-Interchanged Circuit
IC	Integrated Circuit
IAP	In-Application Programming
ISP	In-System Programming
LDO	Low DropOut
LPCD	Low-Power Card Detection
NFC	Near Field Communication
NRZ	Non-Return to Zero
NVIC	Nested Vectored Interrupt Controller
P2P	Peer-to-Peer
PLL	Phase Locked Loop
PLM	Passive Load Modulation
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

18. Revision history

Table 78. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN746X_736X v.3.1	20160405	Product data sheet	-	PN746X_736X v.3.0
Modifications:	• Descriptive title updated • Section 1 “General description”: updated			
PN746X_736X v.3.0	20160330	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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