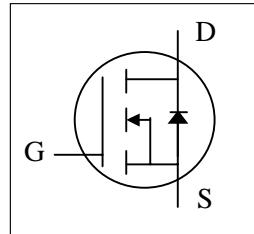
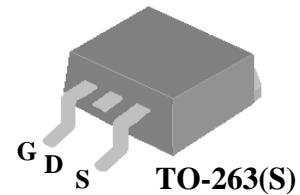




- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	60V
$R_{DS(ON)}$	3.58mΩ
I_D	130A



Description

AP6N3R5 series are from Advanced Power innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-263 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c = 25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	130	A
$I_D @ T_c = 100^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	80	A
I_{DM}	Pulsed Drain Current ¹	300	A
$P_D @ T_c = 25^\circ\text{C}$	Total Power Dissipation	104	W
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation ⁴	3.12	W
E_{AS}	Single Pulse Avalanche Energy ³	183	mJ
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	1.2	°C/W
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁴	40	°C/W



AP6N3R5S

Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=250\mu\text{A}$	60	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_{\text{D}}=40\text{A}$	-	-	3.58	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=250\mu\text{A}$	2	-	5	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_{\text{D}}=40\text{A}$	-	53	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	25	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_{\text{D}}=40\text{A}$	-	80	128	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=30\text{V}$	-	25	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=10\text{V}$	-	25	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=30\text{V}$	-	17	-	ns
t_r	Rise Time	$I_{\text{D}}=40\text{A}$	-	74	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_G=1\Omega$	-	34	-	ns
t_f	Fall Time	$V_{\text{GS}}=10\text{V}$	-	21	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	4500	7200	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=30\text{V}$	-	2800	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	65	-	pF
R_g	Gate Resistance	f=1.0MHz	-	2.3	4.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=40\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_{\text{S}}=40\text{A}$, $V_{\text{GS}}=0\text{V}$	-	55	-	ns
Q_{rr}	Reverse Recovery Charge	dl/dt=100A/ μs	-	56	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting $T_j=25^\circ\text{C}$, $V_{\text{DD}}=30\text{V}$, $L=0.3\text{mH}$, $R_G=25\Omega$
- 4.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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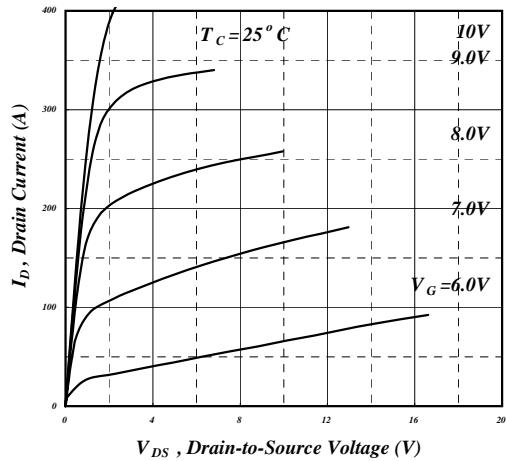


Fig 1. Typical Output Characteristics

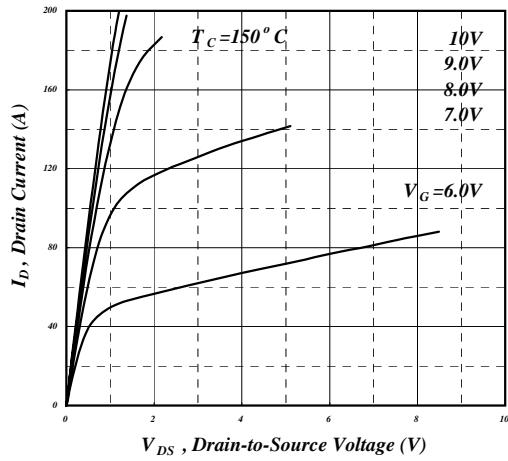


Fig 2. Typical Output Characteristics

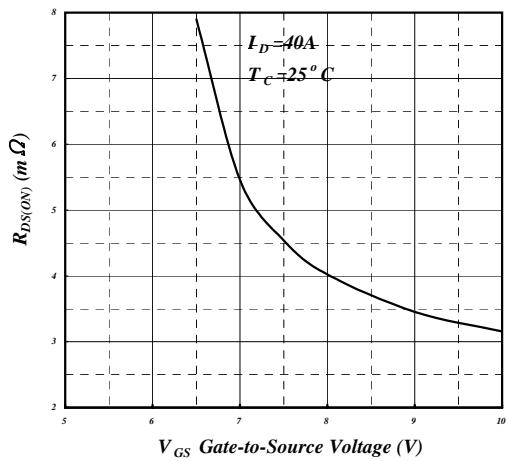


Fig 3. On-Resistance v.s. Gate Voltage

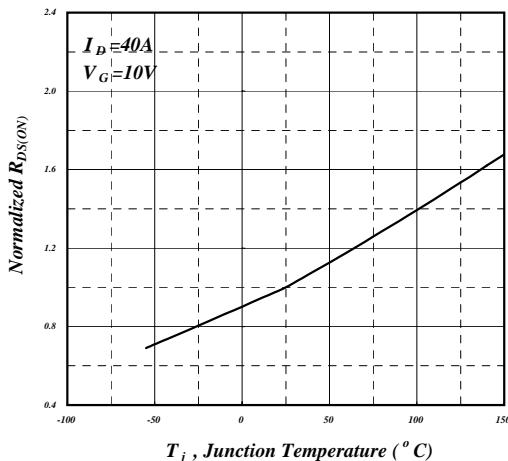


Fig 4. Normalized On-Resistance v.s. Junction Temperature

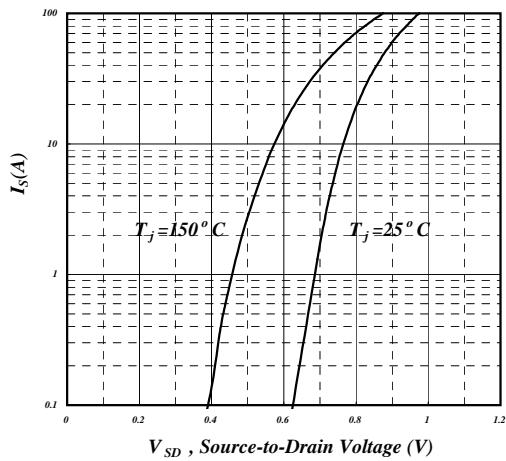


Fig 5. Forward Characteristic of Reverse Diode

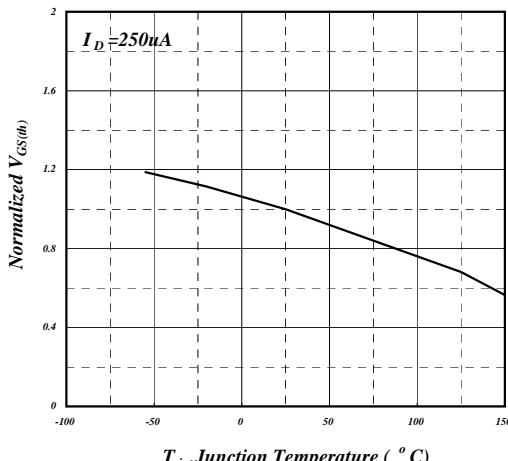


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

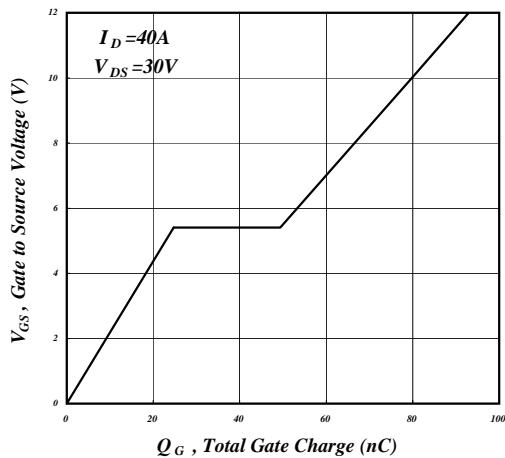


Fig 7. Gate Charge Characteristics

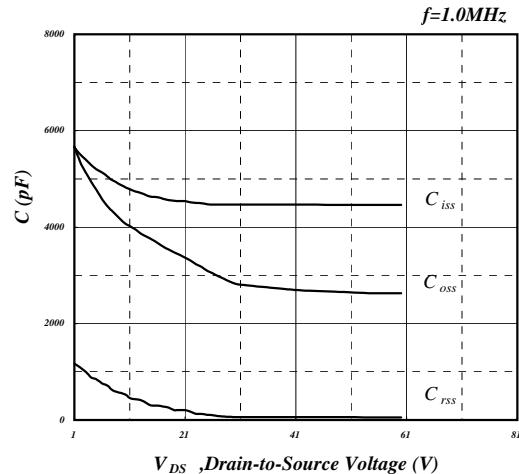


Fig 8. Typical Capacitance Characteristics

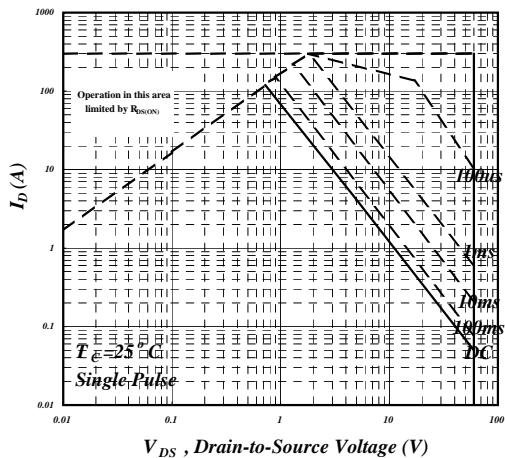


Fig 9. Maximum Safe Operating Area

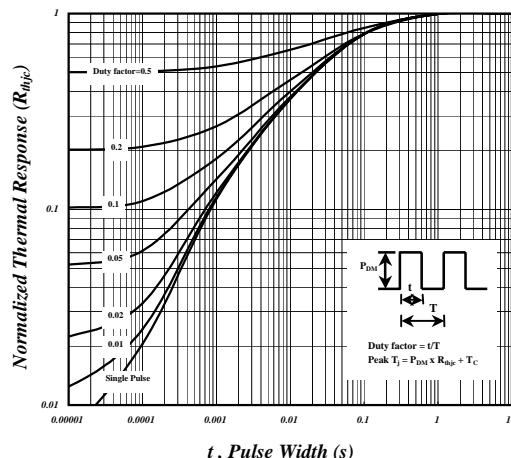


Fig 10. Effective Transient Thermal Impedance

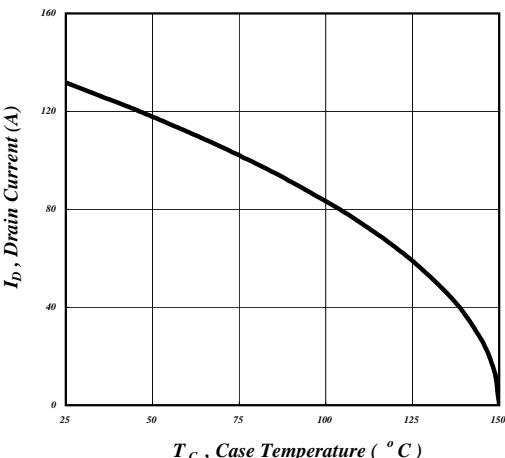


Fig 11. Drain Current v.s. Case Temperature

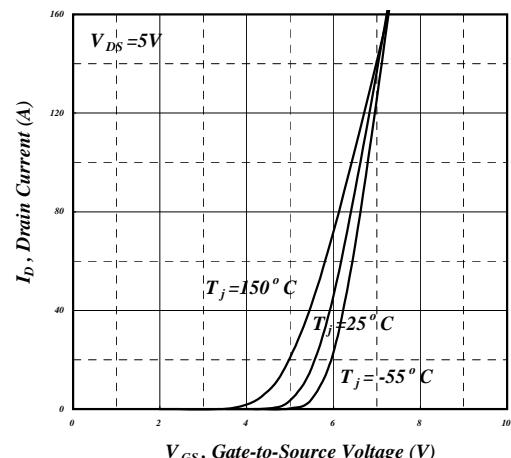


Fig 12. Transfer Characteristics

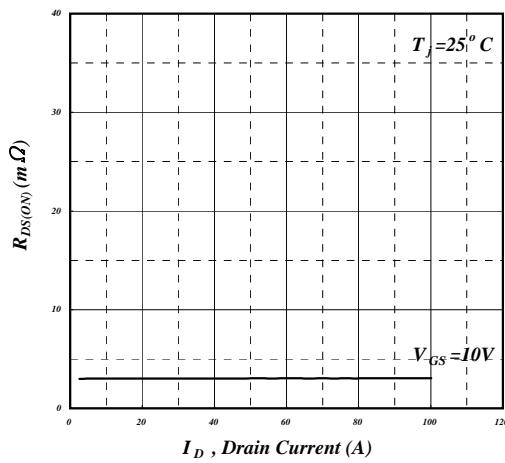


Fig 13. Typ. Drain-Source on State Resistance

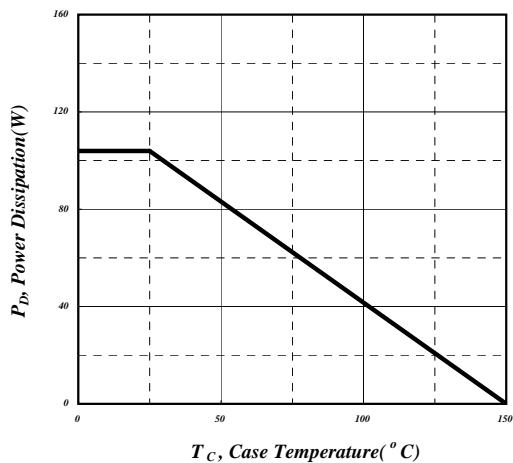


Fig 14. Total Power Dissipation

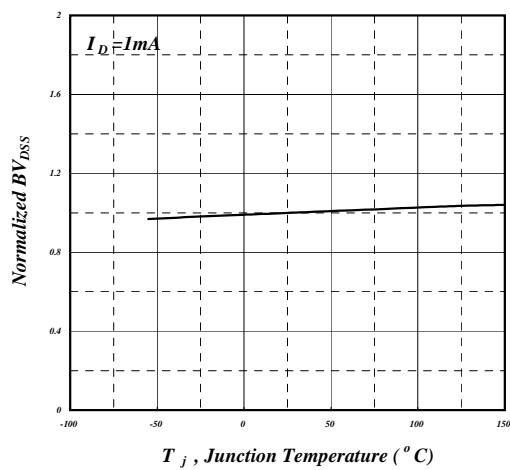


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature



AP6N3R5S

MARKING INFORMATION

