

**14N65K-MT**

Preliminary

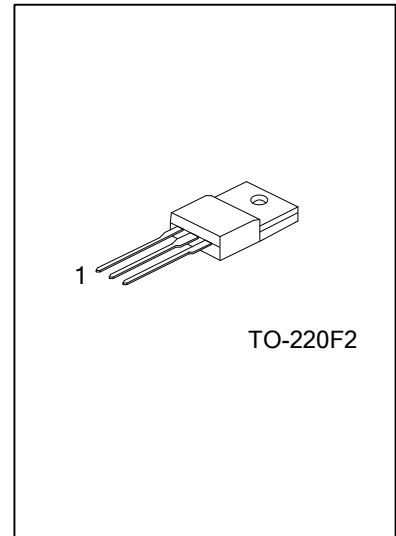
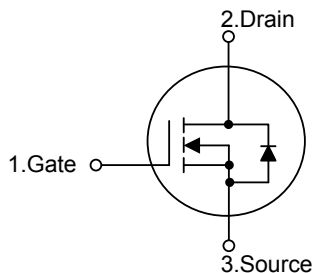
Power MOSFET**14A, 650V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **14N65K-MT** is an N-Channel enhancement mode power MOSFET. The device adopts planar stripe and uses DMOS technology to minimize and provide lower on-state resistance and faster switching speed. It can also withstand high energy pulse under the avalanche and commutation mode conditions.

The UTC **14N65K-MT** is ideally suitable for high efficiency switch mode power supply, power factor correction and electronic lamp ballast based on half bridge topology.

FEATURES

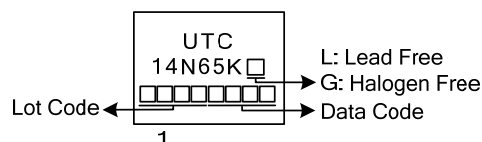
- * $R_{DS(ON)} < 0.63\Omega$ @ $V_{GS} = 10V$, $I_D = 7A$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
14N65KL-TF2-T	14N65KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

14N65KL-TF2-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube (2) TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free
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MARKING

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	14	A
Pulsed Drain Current (Note 2)	I_{DM}	48	A
Avalanche Current (Note 2)	I_{AR}	14	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	325	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	150	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature

3. $L = 3.31\text{mH}$, $I_{AS} = 14\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 14\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.83	$^\circ\text{C}/\text{W}$

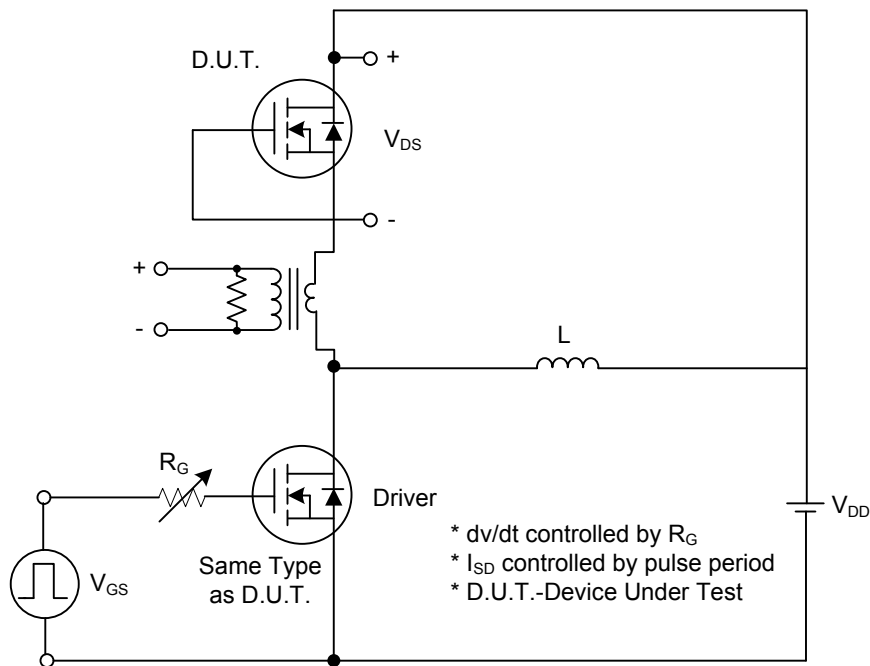
■ **ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250 μA	650			V	
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = 30V, V _{DS} = 0V			100	nA	
		V _{GS} = -30V, V _{DS} = 0V			-100	nA	
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250mA,Referenced to 25°C		0.5		V/°C	
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V	
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 7A			0.63	Ω	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		980		pF	
Output Capacitance	C _{OSS}				185		pF
Reverse Transfer Capacitance	C _{RSS}				10		pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time	t _{D(ON)}	V _{DS} =30V, I _D =0.5A, R _G =25Ω (Note 1, 2)		89		nS	
Turn-On Rise Time	t _R				116		nS
Turn-Off Delay Time	t _{D(OFF)}				388		nS
Turn-Off Fall Time	t _F				145		nS
Total Gate Charge	Q _G	V _{GS} =10V, V _{DS} =50V, I _D =1.3A (Note 1, 2)		47		nC	
Gate-Source Charge	Q _{GS}				12.2		nC
Gate-Drain Charge	Q _{GD}				11.6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 14A			1.4	V	
Maximum Continuous Drain-Source Diode Forward Current	I _S				14	A	
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				56	A	

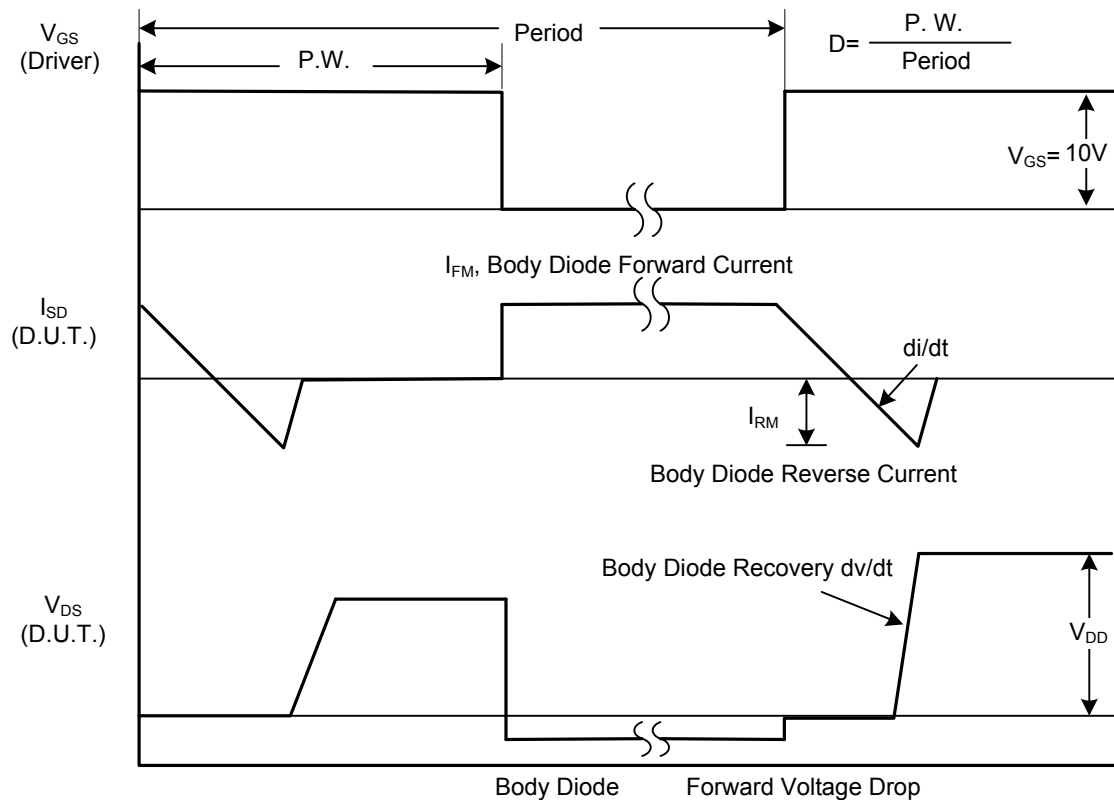
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating ambient temperature

■ TEST CIRCUITS AND WAVEFORMS

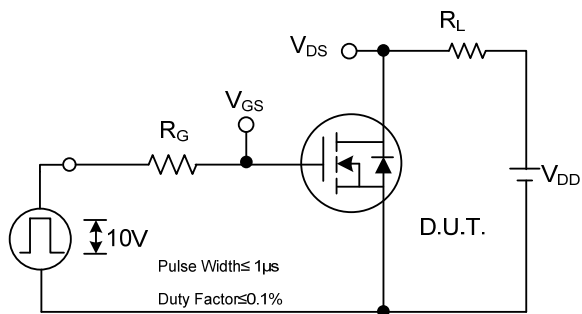


Peak Diode Recovery dv/dt Test Circuit

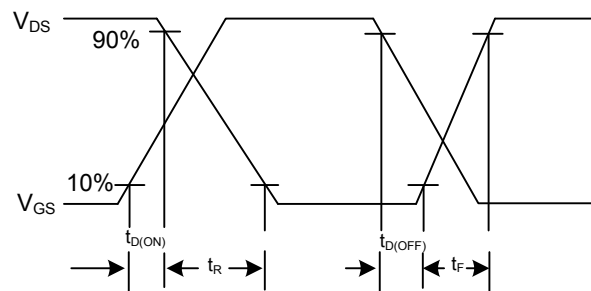


Peak Diode Recovery dv/dt Waveforms

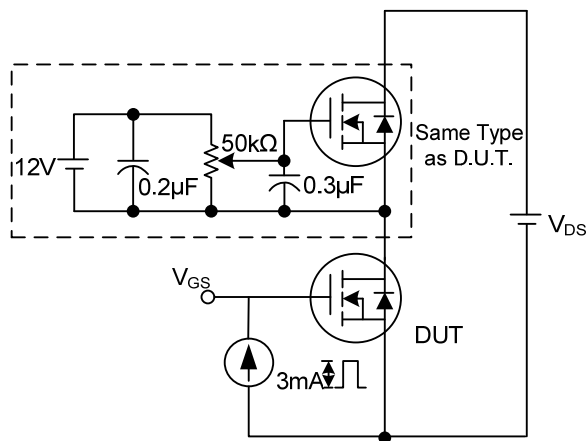
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



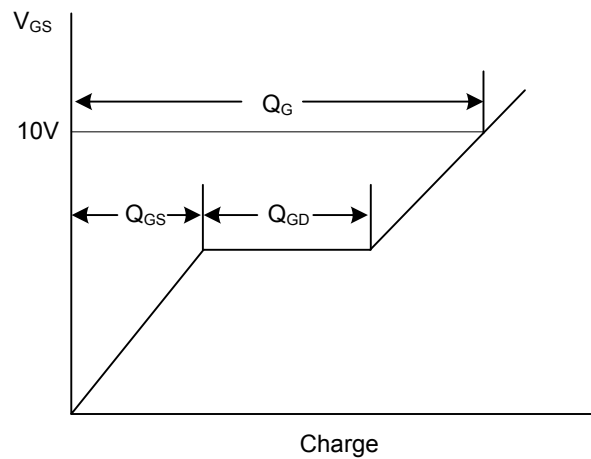
Switching Test Circuit



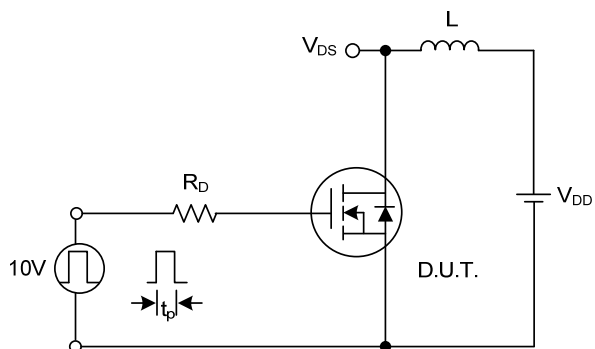
Switching Waveforms



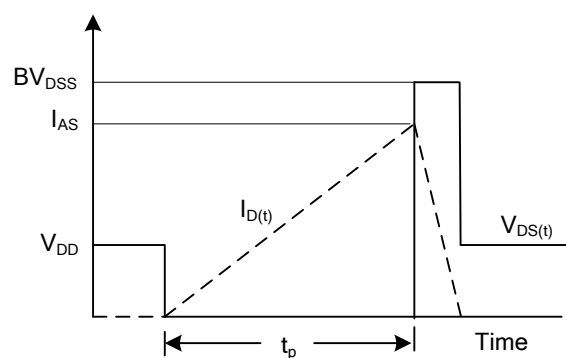
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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