ACE24AC02A3
Two-wire Serial EEPROM

Description

The ACE24AC02A3 is 2048 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 256 words of 8 bits (1 byte) each. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, 8-lead SOP, 8-lead MSOP, 8-lead TSSOP, 8-lead DFN and SOT-23-5 packages. A standard 2-wire serial interface is used to address all read and write functions. Our extended VCC range (1.8V to 5.5V) devices enables wide spectrum of applications.

Features

- Low voltage and low power operations:
  ACE24AC02A3: VCC = 1.8V to 5.5V, Industrial temperature range (-40℃ to 85℃).
  ACE24AC02A3: With 3 bits device address, the devices are suitable for all application. (For use of 5 pins package, the device address A2, A1, and A0 bits must be set to zero)
- Maximum Standby current < 1μA
- 16 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 256 × 8 (2K).
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5ms maximum).
- 1 MHz (5V), 400 kHz (1.8V, 2.5V, 2.7V) Compatibility.
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 1,000,000 cycle's endurance.
- 100 years data retention.
- Standard 8-pin DIP/SOP/MSOP/TSSOP/TDFN and SOT-23-5 Pb-free packages.

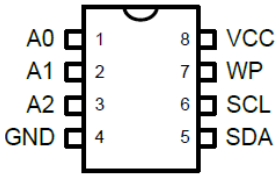
Absolute Maximum Ratings

Industrial operating temperature	-40℃ to 85℃
Storage temperature	-50℃ to 125℃
Input voltage on any pin relative to ground	-0.3V to V_{CC} + 0.3V
Maximum voltage	8V
ESD protection on all pins	>2000V

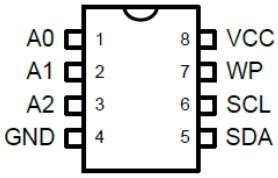
*Notice: Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.

Packaging Type

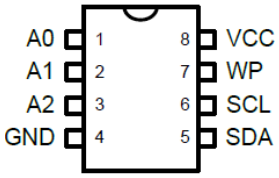
SOP-8



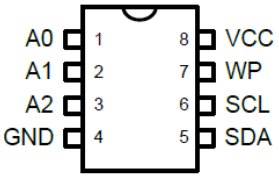
TSSOP-8



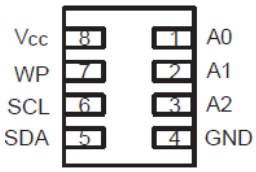
MSOP-8



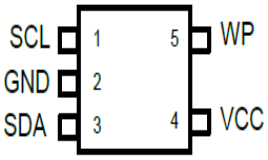
DIP-8



TDFN-8



SOT-23-5



Pin Configurations

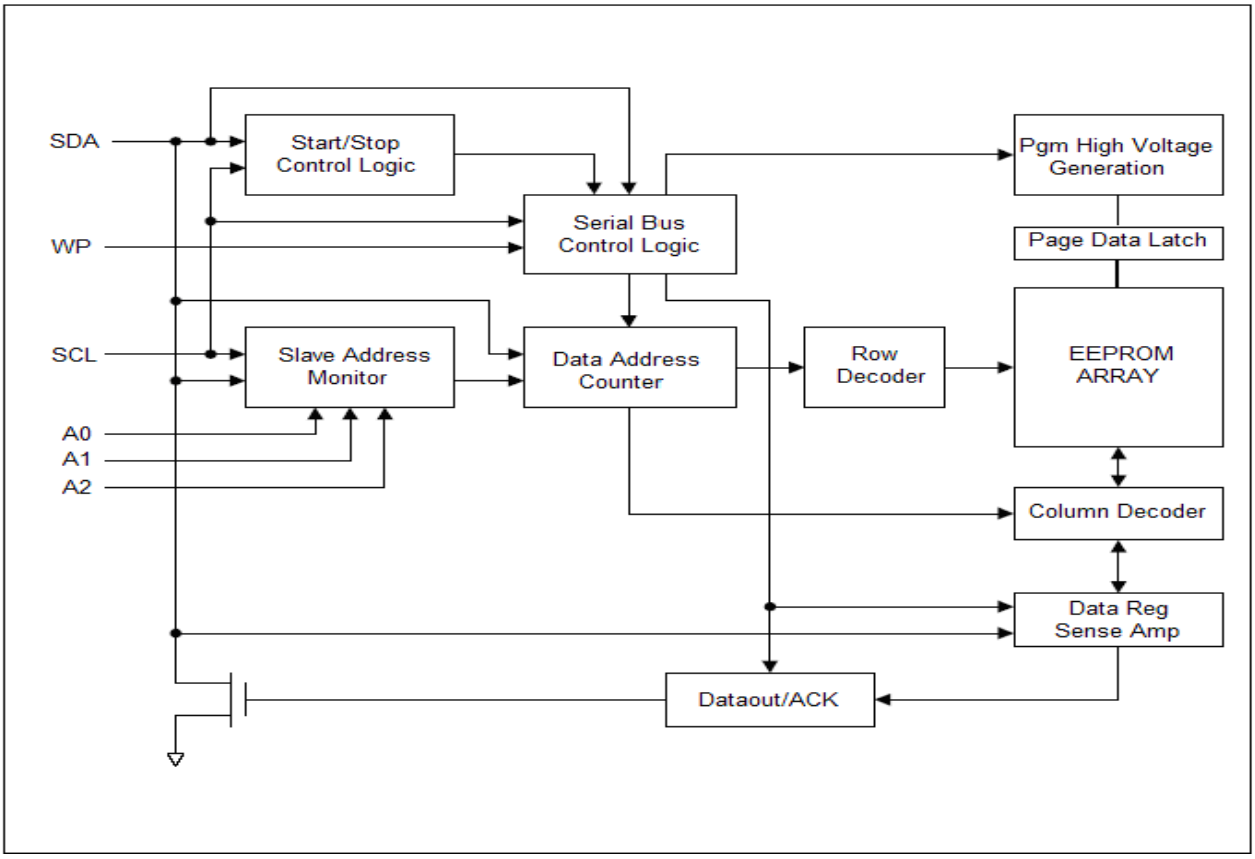
Pin Name	Function
A2,A1,A0	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
VCC	Power Supply
GND	Ground
NC	No-Connect

Ordering Information

ACE24AC02A3 XX + X H

- Halogen - free
- U：Tube
  T：Tape and Reel
- Pb - free
- FM：SOP-8
  TM：TSSOP-8
  OM：MSOP-8
  DP：DIP-8
  DM：TDFN-8
  BN：SOT-23-5

Block Diagram



Pin Description

A. Serial Clock (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

B. Serial Data Line (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

C. Write Protect(WP)

The ACE24AC02A3 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}. Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}. Read operations is not affected by the WP pin's input level.

Memory Organization

The ACE24AC02A3 devices have 16 pages. Since each page has 16 bytes, random word addressing to ACE24AC02A3 will require 8 bits data word addresses.

Device Operation

A. Serial Clock And Data Transitions

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at VIL. Any SDA signal transition may interpret as either a start or stop condition as described below.

B. Start Conditions

With SCL ≥ V_{IH}, a SDA transition from high to low is interpreted as a start condition. All valid commands must begin with a start condition.

C. Stop Condition

With SCL ≥ V_{IH}, a SDA transition from low to high is interpreted as a stop condition. All valid read or write commands end with a stop condition. The device goes into the standby mode if it is after a read command. A stop condition after page or byte write command will trigger the chip into the standby mode after the self-timed internal programming finish.

D. Acknowledge

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledge the data or address by outputting a "0" after receiving each word. The acknowledge signal occurs on the 9th serial clock after each word.

E. Standby Mode

The EEPROM goes into low power standby mode after a fresh power up, after receiving a stop bit in read mode, or after completing a self-time internal programming operation.

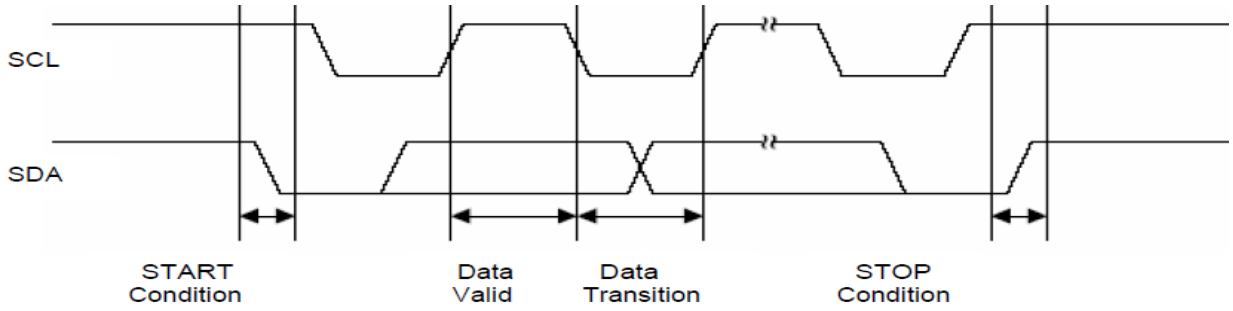


Figure 3: Timing diagram for start and stop conditions

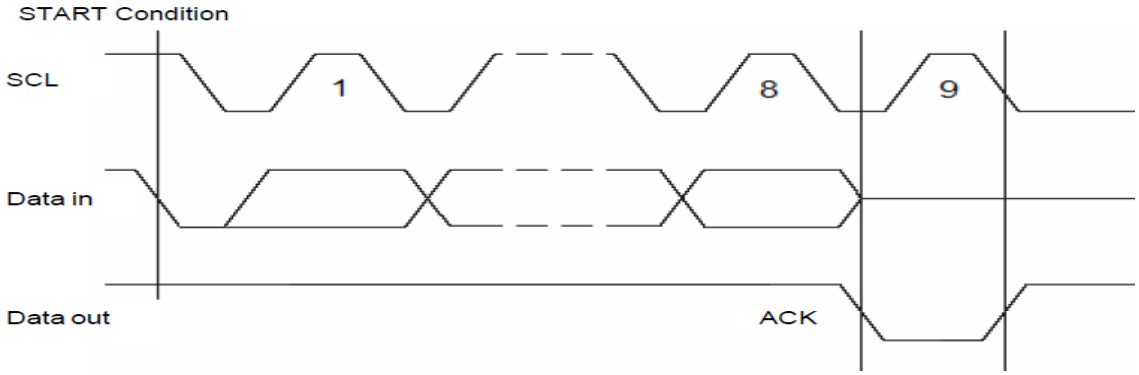


Figure 4: Timing diagram for output acknowledge

Device Addressing

The 2-wire serial bus protocol mandates an 8 bits device address word after a start bit condition to invoke valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next three bits are device address bits. These three device address bits (5^{th}, 6^{th} and 7^{th}) are not cared and could be coded from 000 (b) to 111 (b). Only one ACE24AC02A3 device can be used on the on 2-wire bus. If a match is made, the EEPROM device outputs an acknowledge signal after the 8^{th} read/write bit, otherwise the chip will go into standby mode.

The last or 8th bit is a read/write command bit. If the 8th bit is at VIH then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

Write Operations

A. Byte Write

A byte write operation starts when a micro-controller sends a start bit condition, follows by a proper EEPROM device address and then a write command. If the device address bits match the chip select address, the EEPROM device will acknowledge at the 9^{th} clock cycle. The micro-controller will then send the rest of the lower 8 bits word address. At the 18^{th} cycle, the EEPROM will acknowledge the 8-bit address word. The micro-controller will then transmit the 8 bit data. Following an acknowledge signal from the EEPROM at the 27^{th} clock cycle, the micro-controller will issue a stop bit. After receiving the stop bit, the EEPROM will go into a self-timed programming mode during which all external inputs will be disabled. After a programming time of T_{WC}, the byte programming will finish and the EEPROM device will return to the standby mode.

B. Page Write

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All ACE24AC02A3 are organized to have 16 bytes per memory row or page.

With the same write command as the byte write, the micro-controller does not issue a stop bit after sending the 1^{st} byte data and receiving the acknowledge signal from the EEPROM on the 27^{th} clock cycle. Instead it sends out a second 8-bit data word, with the EEPROM acknowledging at the 36^{th} cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a stop bit after the $n \times 9^{th}$ clock cycle. After which the EEPROM device will go into a self- timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the standby mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data

words are loaded, the 17th data word will be loaded to the 1st data word column address. The 18th data word will be loaded to the 2nd data word column address and so on. In other word, data word address (column address) will "roll" over the previously loaded data.

C. Acknowledge Polling

Acknowledge polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the standby mode, the device will return a valid acknowledge signal at the 9th clock cycle.

Read Operations

The read command is similar to the write command except the 8th read/write bit in address word is set to "1". The three read operation modes are described as follows:

(A) Current Address Read

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a start bit and a valid device address word with the read/write bit (8th) set to"1". The EEPROM will response with an acknowledge signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an acknowledge signal on the 18th clock cycle. The micro-controller issues a valid stop bit after the 18th clock cycle to terminate the read operation. The device then returns to standby mode.

(B) Sequential Read

The sequential read is very similar to current address read. The micro-controller issues a start bit and a valid device address word with read/write bit (8th) set to "1". The EEPROM will response with an acknowledge signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an acknowledge signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the acknowledge signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an acknowledge signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an acknowledge signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a stop bit afterwards instead.

(C) Random Read

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a “dummy write” instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a start bit first, follows by a valid device address with the read/write bit (8^{th}) set to “0”. The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a start bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction which is to read the current address.

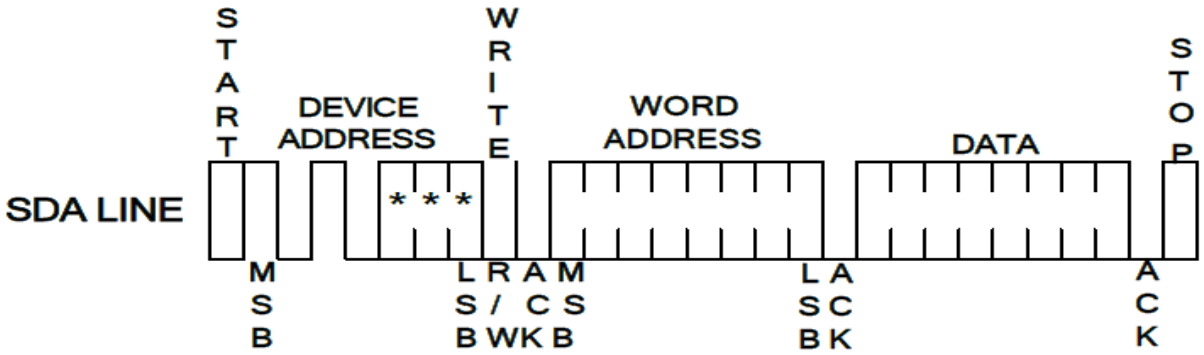


Figure 5: Byte Write

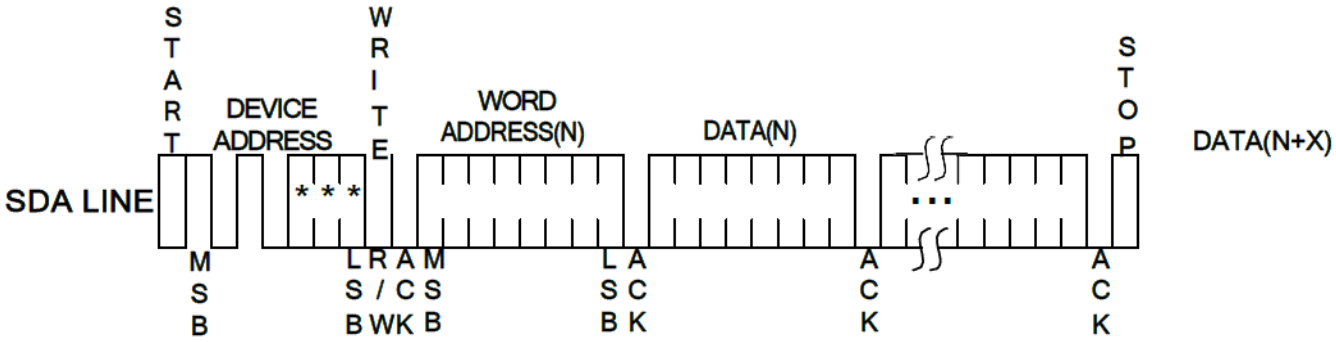


Figure 6: Page Write

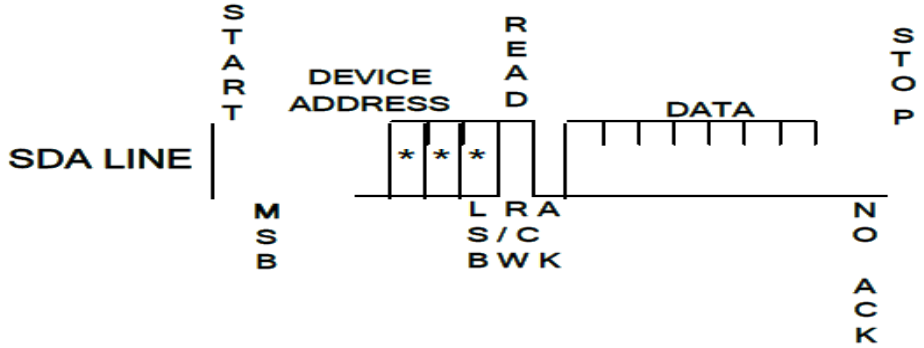


Figure 7: Current Address Read

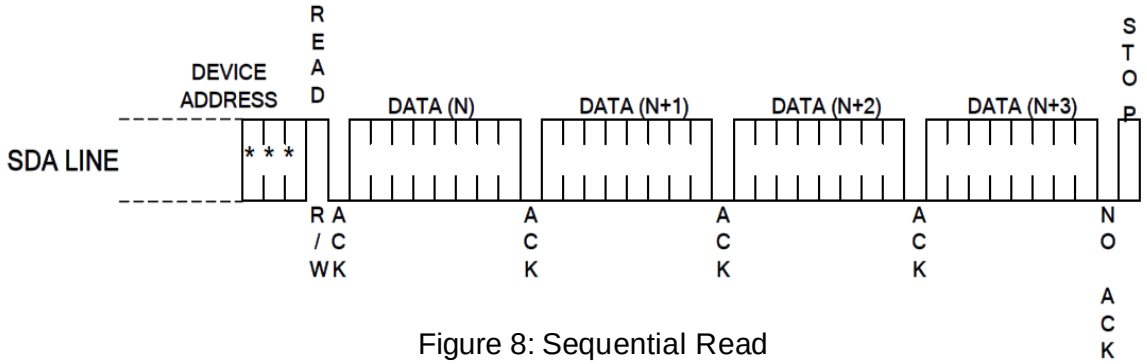


Figure 8: Sequential Read

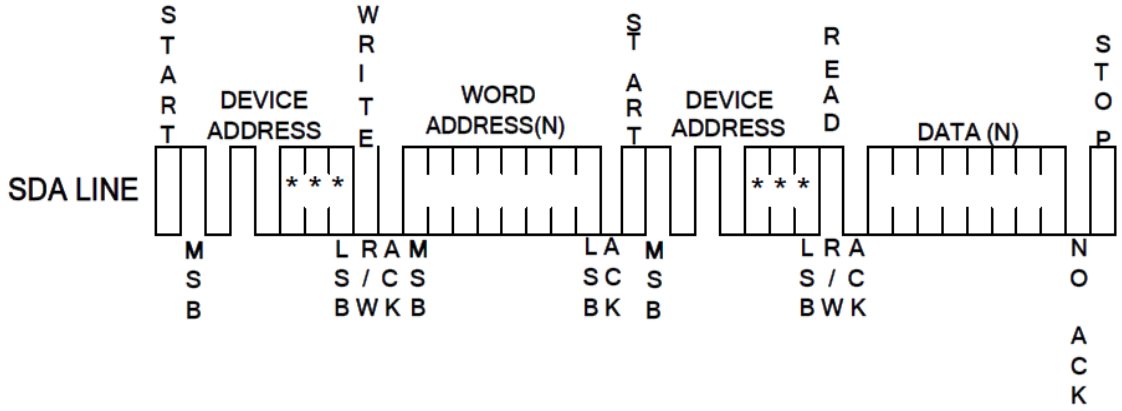


Figure 9: Random Read

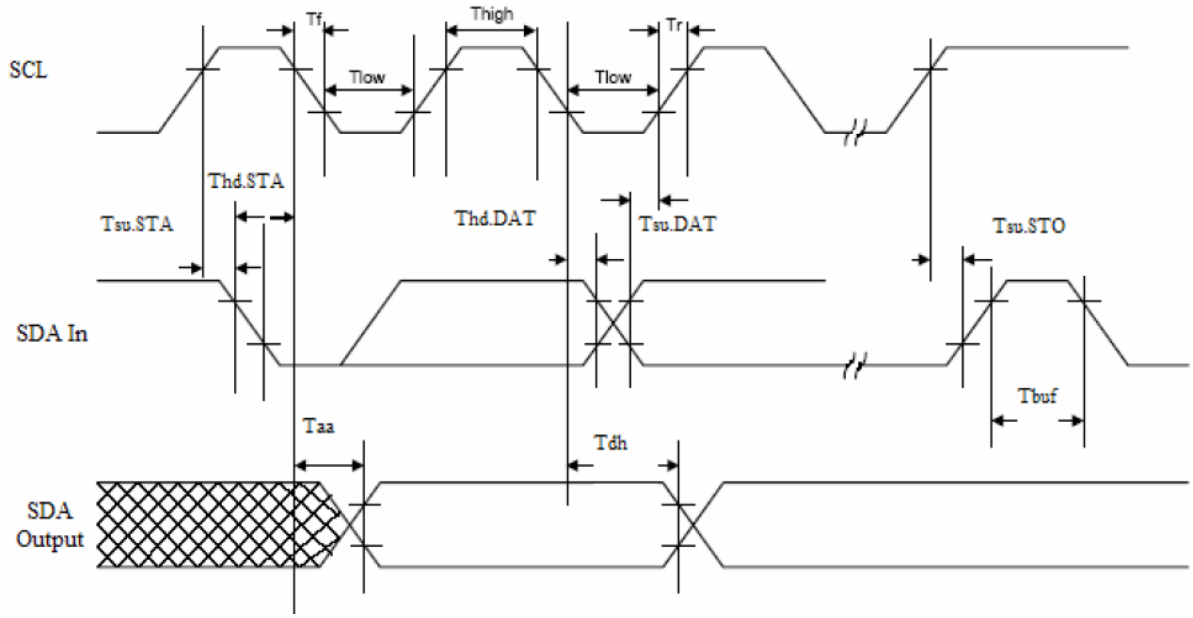


Figure 10: SCL and SDA Bus Timing

AC Characteristics

Symbol	Parameter	1.8V-2.7V		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
T_{LOW}	Clock Pulse Width Low	1.3		0.4		μs
T_{HIGH}	Clock Pulse Width High	0.6		0.4		μs
T_I	Noise suppression time(1)		180		120	ns
T_{AA}	Clock Low to Data Out Valid	0.3	0.9	0.2	0.55	μs
T_{BUF}	Time the bus must be free before a new transmission can Start	1.3		0.5		μs
$T_{HD.STA}$	Start Hold Time	0.6		0.25		μs
$T_{SU.STA}$	Start Set-up Time	0.6		0.25		μs
$T_{HD.DAT}$	Data In Hold Time	0		0		μs
$T_{SU.DAT}$	Data In Set-up Time	100		100		ns
T_R	Inputs Rise Time		0.3		0.3	μs
T_F	Inputs Fall Time		300		100	ns
$T_{SU.STO}$	Stop Setup Time	0.6		0.25		μs
T_{DH}	Data Out Hold Time	50		50		ns
T_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25℃, Page Mode,3.3V	1,000,000				Write Cycles

Notes*： 1.This Parameter is expected by characterization but is not fully screened bytest.

2.AC Measurement conditions:

R_L (Connects to Vcc): 1.3KΩ

Input Pulse Voltages: 0.3Vcc to 0.7Vcc

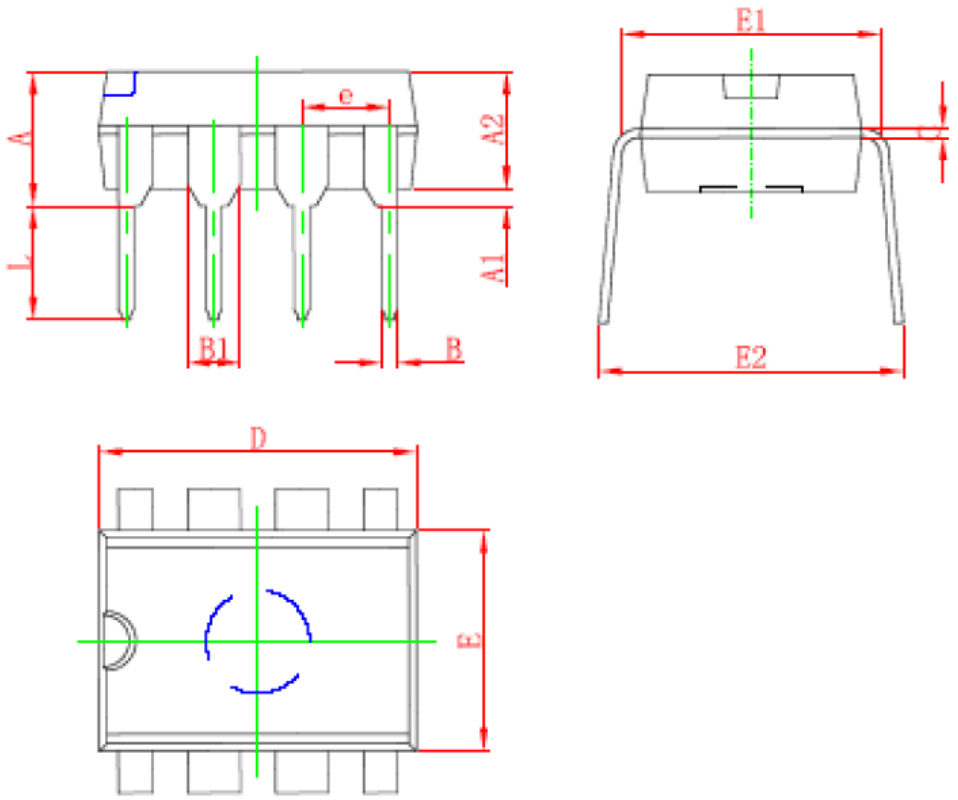
Input and output timing reference Voltages: 0.5Vcc

DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Power supply VCC		1.8		5.5	V
I_{CC}	Supply Current	V_{CC} @5.0V, Read = 400kHZ		0.5	1.0	mA
I_{CC}	Supply Current	V_{CC}@ 5.0V, Write = 400kHZ		2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} @1.8V, V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current	V_{CC} @2.5V, V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB3}	Standby Current	V_{CC} @5.0V, V_{IN} = V_{CC} or V_{SS}		0.07	1.0	
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			3.0	µA
I_{LO}	Output Leakage Current	V_{IN} = V_{CC} or V_{SS}			3.0	µA
V_{IL}	Input Low Level		-0.6		V_{CC}*0.3	V
V_{IH}	Input High Level		V_{CC}*0.7		V_{CC}+0.5	V
V_{OL1}	Output Low Level	V_{CC} @1.8V, I_{OL} =0.15 mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} @3.0V, I_{OL} = 2.1 mA			0.4	V

Packaging information

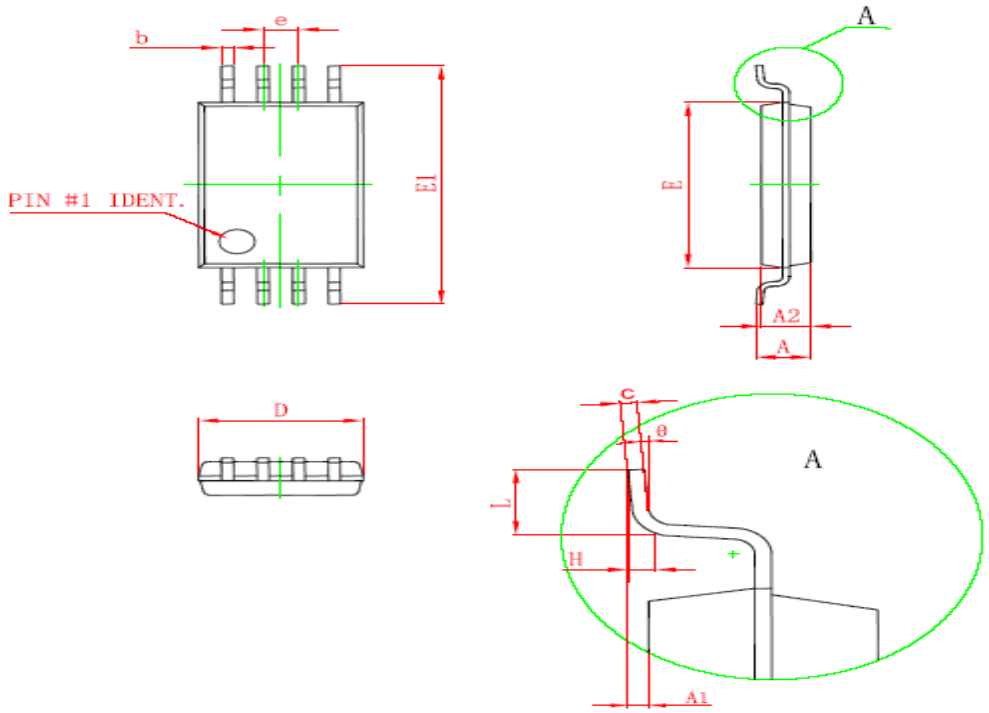
DIP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Packaging information

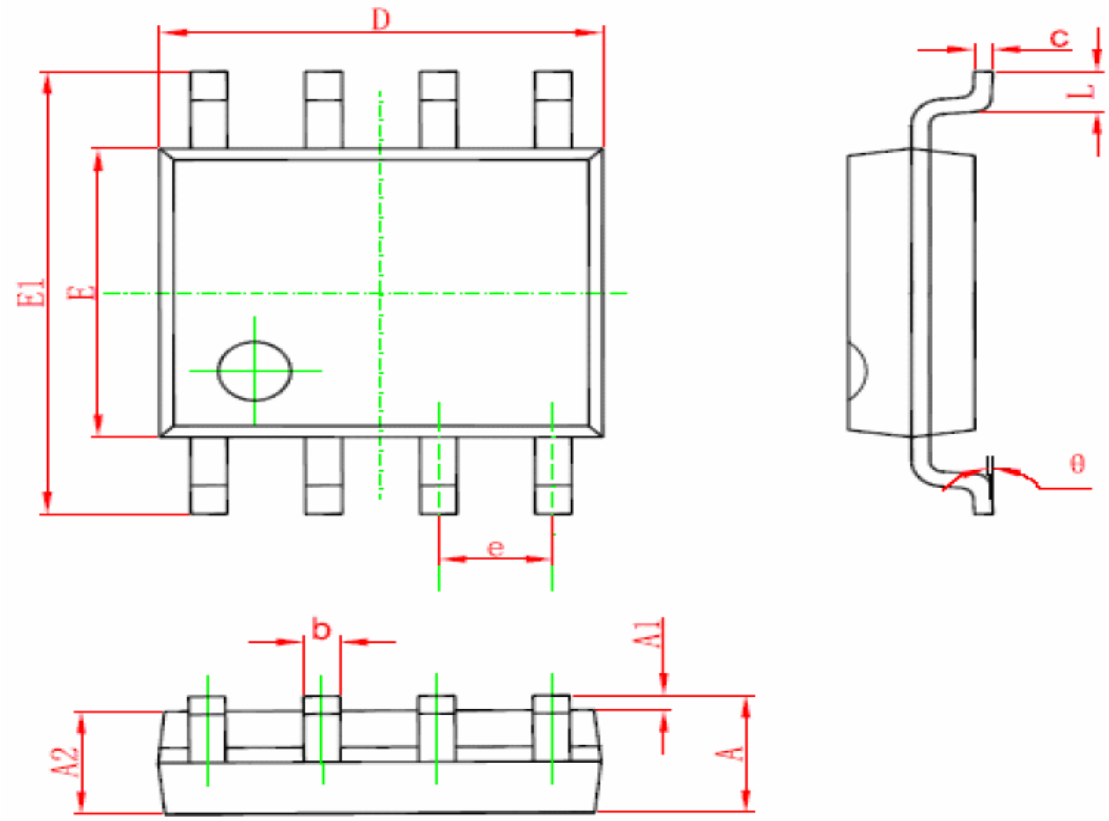
TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Packaging information

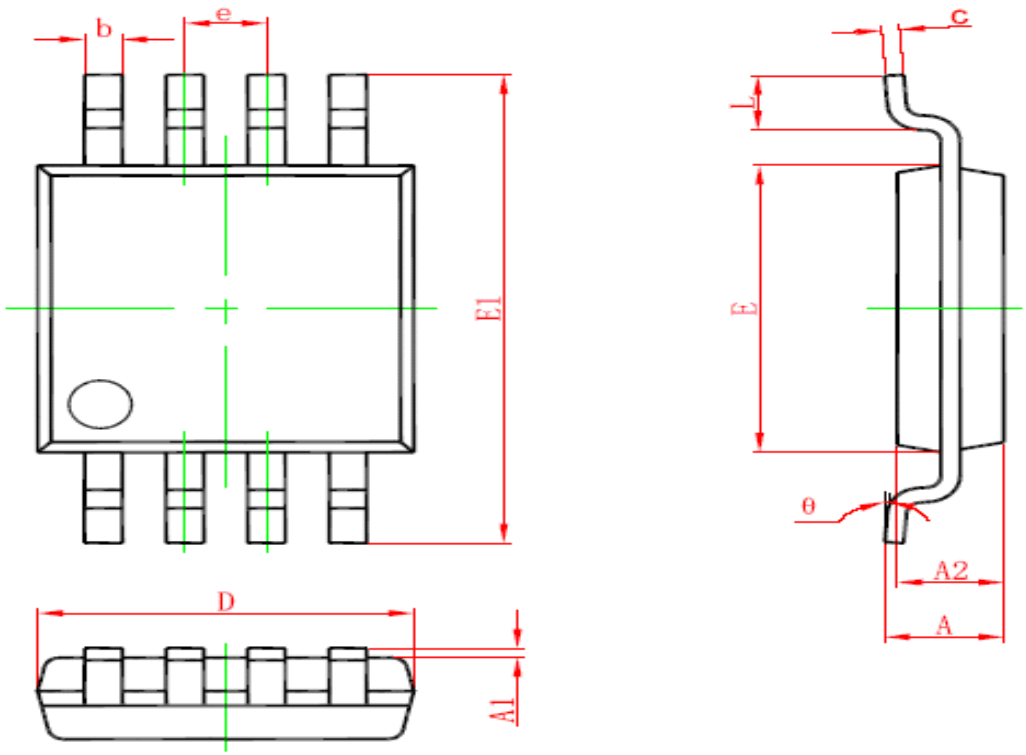
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Packaging information

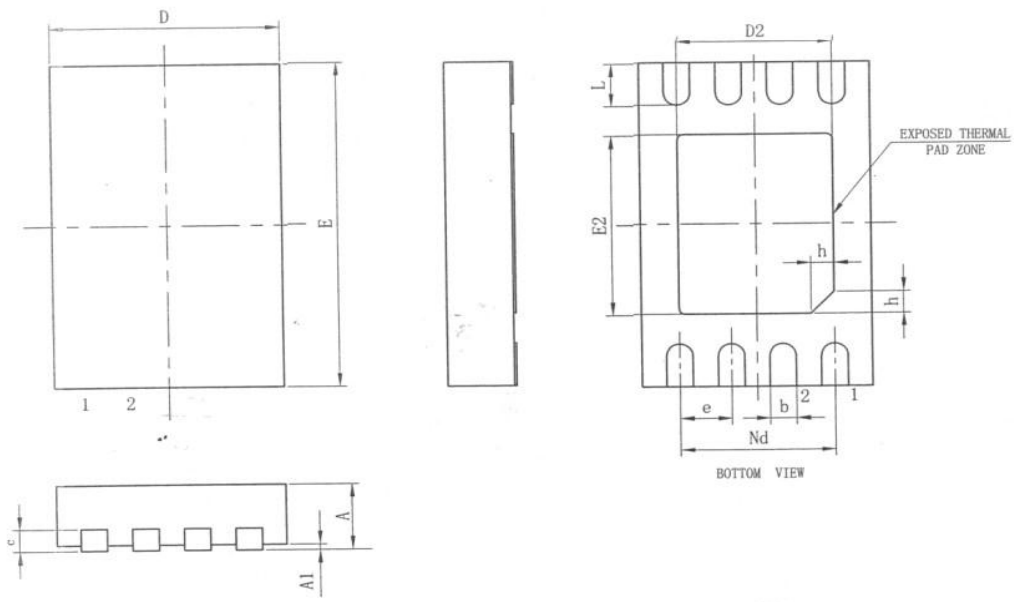
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.320	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.65 (BSC)		0.026 (BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Packaging information

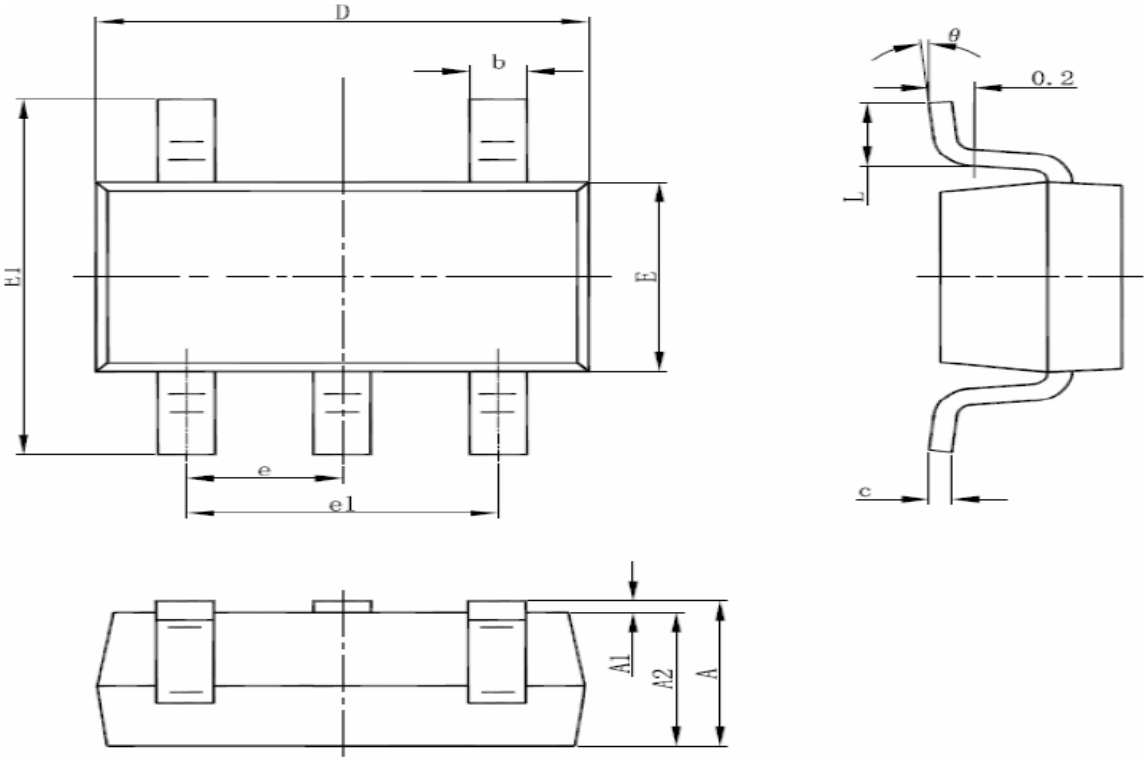
TDFN-8



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.50REF		
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.60REF		
L	0.30	0.40	0.50
h	0.20	0.25	0.30
L/F Surface Electroplate	NIPdAu (Nickel, Pd, Metal)		
Dimension（mil）	67*75		

Packaging information

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
	0°	8°	0°	6°

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.