50 GHz to 95 GHz, GaAs, pHEMT, MMIC, Wideband Low Noise Amplifier

Data Sheet **ADL7003**

FEATURES

- Gain: 14 dB typical
- Noise figure: 5 dB typical
- Input return loss (S11): 15 dB typical
- Output return loss (S22): 20 dB typical
- Output power for 1 dB compression (P1dB): 14 dBm typical
- Saturated output power (P_{SAT}): 18 dBm typical
- Output third-order intercept (IP3): 21 dBm typical
- Supply voltage: 3 V at 120 mA
- 50 Ω matched input/output
- Die size: 1.9 mm × 1.9 mm × 0.05 mm

APPLICATIONS

- Test instrumentation
- Military and space
- Telecommunications infrastructure

FUNCTIONAL BLOCK DIAGRAM

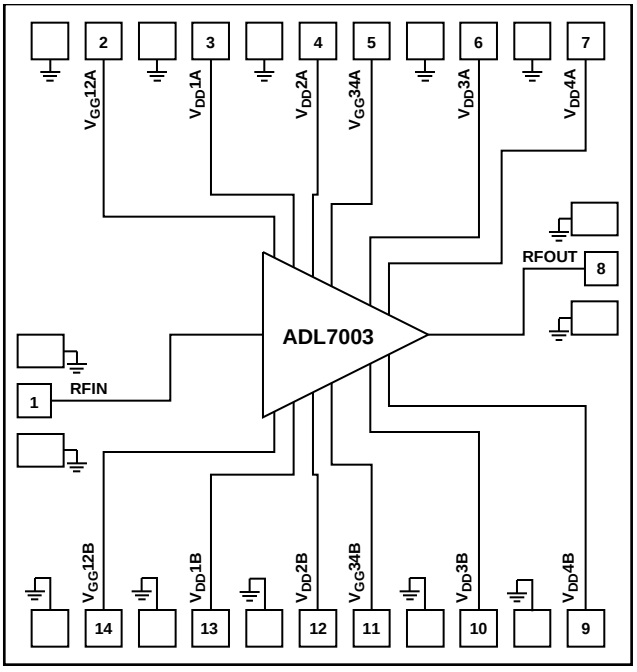

Figure 1.

GENERAL DESCRIPTION

The ADL7003 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), balanced low noise amplifier that operates from 50 GHz to 95 GHz. In the lower band of 50 GHz to 70 GHz, the ADL7003 provides 14 dB (typical) of gain, 21 dBm output IP3, and 12 dBm of output power for 1 dB gain compression. In the upper band of 70 GHz to 90 GHz, the ADL7003 provides 15 dB (typical) of gain, 21 dBm output IP3, and 14 dBm of output power for 1 dB gain compression. The ADL7003 requires 120 mA from a 3 V supply. The ADL7003 amplifier inputs/outputs are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via one 0.076 mm (3 mil) ribbon bond of 0.076 mm (3 mil) minimal length.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

4/2017—Revision 0: Initial Version

SPECIFICATIONS

50 GHz TO 70 GHz FREQUENCY RANGE

$T_{DIE\ BOTTOM}$ = 25°C; V_{DD} = $V_{DD}1A$ = $V_{DD}2A$ = $V_{DD}3A$ = $V_{DD}4A$ = 3 V; I_{DQ} = I_{DQ1A} + I_{DQ2A} + I_{DQ3A} + I_{DQ4A} = 120 mA, unless otherwise noted. Adjust V_{GG} = $V_{GG}12A$ = $V_{GG}34A$ from −1.5 V to 0 V to achieve the desired I_{DQ}. Typical V_{GG} = −0.5 V for I_{DQ} = 120 mA.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		50		70	GHz	
GAIN			14		dB	
Gain Variation over Temperature			0.02		dB/°C	
NOISE FIGURE			5		dB	
RETURN LOSS						
Input	S11		15		dB	
Output	S22		20		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		12		dBm	
Saturated Output Power	P_{SAT}		16		dBm	
Output Third-Order Intercept	OIP3		21		dBm	Output power (P_{OUT})/tone = 0 dBm with 1 MHz tone spacing
INPUT						
Input Third-Order Intercept	IIP3		7		dBm	P_{OUT}/tone = 0 dBm with 1 MHz tone spacing
SUPPLY						
Current	I_{DQ}		120	180	mA	Adjust V_{GG} to achieve I_{DQ} = 120 mA typical
Voltage	V_{DD}	2	3	4	V	

70 GHz TO 90 GHz FREQUENCY RANGE

$T_{DIE\ BOTTOM}$ = 25°C; V_{DD} = $V_{DD}1A$ = $V_{DD}2A$ = $V_{DD}3A$ = $V_{DD}4A$ = 3 V; I_{DQ} = I_{DQ1A} + I_{DQ2A} + I_{DQ3A} + I_{DQ4A} = 120 mA, unless otherwise noted. Adjust V_{GG} = $V_{GG}12A$ = $V_{GG}34A$ from −1.5 V to 0 V to achieve the desired I_{DQ}. Typical V_{GG} = −0.5 V for I_{DQ} = 120 mA.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		70		90	GHz	
GAIN		13	15		dB	
Gain Variation over Temperature			0.02		dB/°C	
NOISE FIGURE			5.5	6.5	dB	
RETURN LOSS						
Input	S11		15		dB	
Output	S22		15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		14		dBm	
Saturated Output Power	P_{SAT}		18		dBm	
Output Third-Order Intercept	OIP3		21		dBm	P_{OUT}/tone = 0 dBm with 1 MHz tone spacing
INPUT						
Input Third-Order Intercept	IIP3		6		dBm	P_{OUT}/tone = 0 dBm with 1 MHz tone spacing
SUPPLY						
Current	I_{DQ}		120	180	mA	Adjust V_{GG} to achieve I_{DQ} = 120 mA typical
Voltage	V_{DD}	2	3	4	V	

90 GHz TO 95 GHz FREQUENCY RANGE

$T_{DIE\ BOTTOM}$ = 25°C; V_{DD} = V_{DD}1A = V_{DD}2A = V_{DD}3A = V_{DD}4A = 3 V; I_{DQ} = I_{DQ1A} + I_{DQ2A} + I_{DQ3A} + I_{DQ4A} = 120 mA, unless otherwise noted. Adjust V_{GG} = V_{GG}12A = V_{GG}34A from −1.5 V to 0 V to achieve the desired I_{DQ}. Typical V_{GG} = −0.5 V for I_{DQ} = 120 mA.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		90		95	GHz	
GAIN			11		dB	
Gain Variation over Temperature			0.02		dB/°C	
RETURN LOSS						
Input	S11		15		dB	
Output	S22		15		dB	
SUPPLY						
Current	I_{DQ}		120	180	mA	Adjust V_{GG} to achieve I_{DQ} = 120 mA typical
Voltage	V_{DD}	2	3	4	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD})	4.5 V
Gate Bias Voltage (V_{GG})	−2 V to 0 V dc
Radio Frequency (RF) Input Power (RFIN)	15 dBm
Continuous Power Dissipation (P_{DISS}), at $T_{DIE\ BOTTOM}$ = 85°C (Derate 15.00 mW/°C Above 85°C)	1.350 W
Storage Temperature Range (Ambient)	−65°C to +150°C
Operating Temperature Range (Die Bottom)	−55°C to +85°C
ESD Sensitivity Human Body Model (HBM)	Class 1A 250 V
Channel Temperature to Maintain 1 Million Hour MTTF	175°C
Nominal Channel Temperature at $T_{DIE\ BOTTOM}$ = 85°C, V_{DD} = 3 V	110°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-14-5	66.70	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

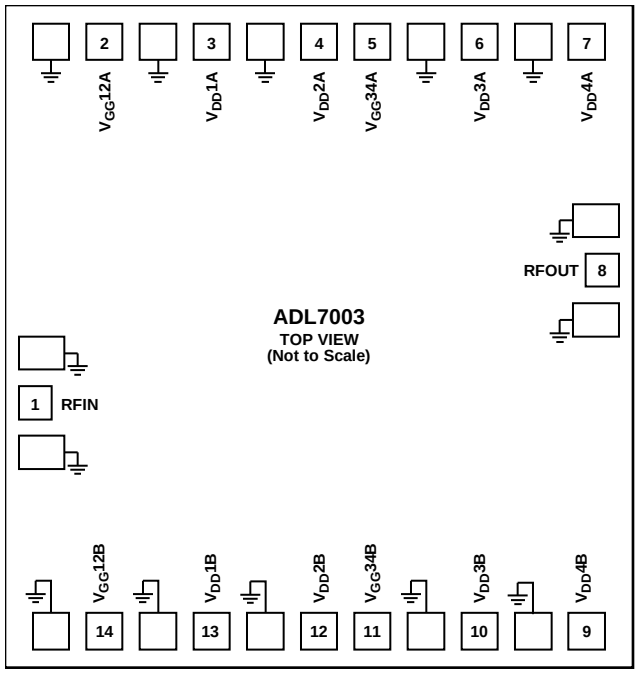

Figure 2. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input. This pad is ac-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2	V_{GG}12A	Gate Control Pad for the First and Second Stage Amplifiers. See Figure 4 for the interface schematic.
3, 4	V_{DD}1A, V_{DD}2A	Drain Bias Voltage Pads for the First and Second Stage Amplifiers. External bypass capacitors of 120 pF, 0.1 µF, and 4.7 µF are required. Connect these pads to a 3 V supply. See Figure 5 for the interface schematic.
5	V_{GG}34A	Gate Control Pad for the Third and Fourth Stage Amplifiers. See Figure 4 for the interface schematic.
6, 7	V_{DD}3A, V_{DD}4A	Drain Bias Voltage Pads for the Third and Fourth Stage Amplifiers. External bypass capacitors of 120 pF, 0.1 µF, and 4.7 µF are required. Connect these pads to a 3 V supply. See Figure 5 for the interface schematic.
8	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω. See Figure 9 for the interface schematic.
9, 10	V_{DD}4B, V_{DD}3B	Drain Bias Voltage Pads for the Fourth and Third Stage Alternative Bias Configuration. External bypass capacitors of 120 pF, 0.1 µF, and 4.7 µF are required. See Figure 7 for the interface schematic.
11	V_{GG}34B	Gate Control Pad for the Third and Fourth Stage Alternative Bias Configuration. Coupling capacitors are required. See Figure 8 for the interface schematic.
12, 13	V_{DD}2B, V_{DD}1B	Drain Bias Voltage Pads for the Second and First Stage Alternative Bias Configuration. External bypass capacitors of 120 pF, 0.1 µF, and 4.7 µF are required. See Figure 7 for the interface schematic.
14	V_{GG}12B	Gate Control Pad for the First and Second Stage Alternative Bias Configuration. Coupling capacitors are required. See Figure 8 for the interface schematic.
Die Bottom	GND	Ground. Die bottom must be connected to RF/dc ground. See Figure 6 for the interface schematic.

INTERFACE SCHEMATIC

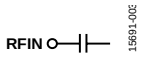

Figure 3. RFIN Interface Schematic

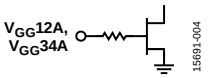

Figure 4. V_{GG}12A, V_{GG}34A Interface Schematic

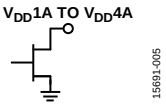

Figure 5. V_{DD}1A to V_{DD}4A Interface Schematic

Figure 6. GND Interface Schematic

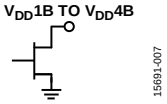

Figure 7. V_{DD}1B to V_{DD}4B Interface Schematic

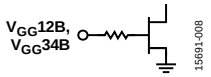

Figure 8. V_{GG}12B, V_{GG}34B Interface Schematic

Figure 9. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

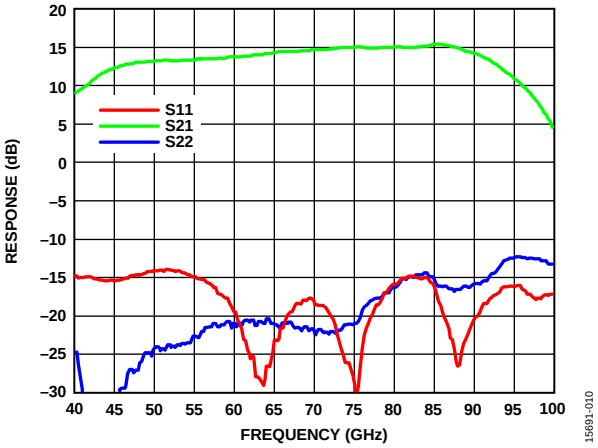

Figure 10. Broadband Gain and Return Loss vs. Frequency

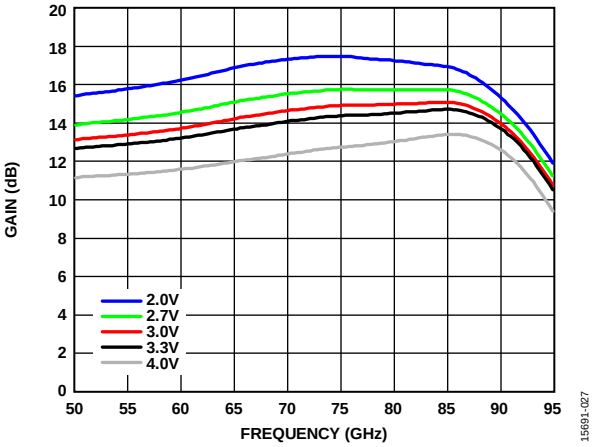

Figure 13. Gain vs. Frequency for Various V_{DD} Values

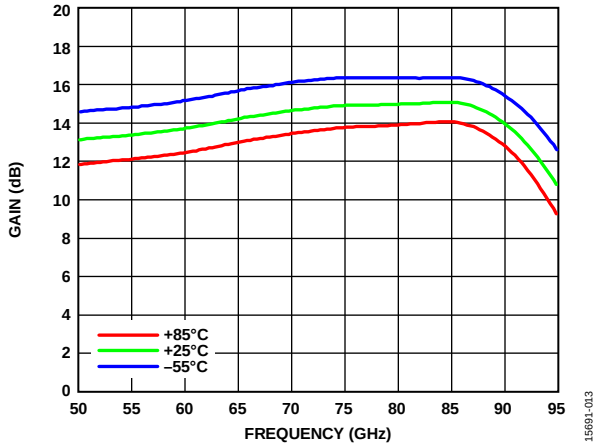

Figure 11. Gain vs. Frequency for Various Temperatures

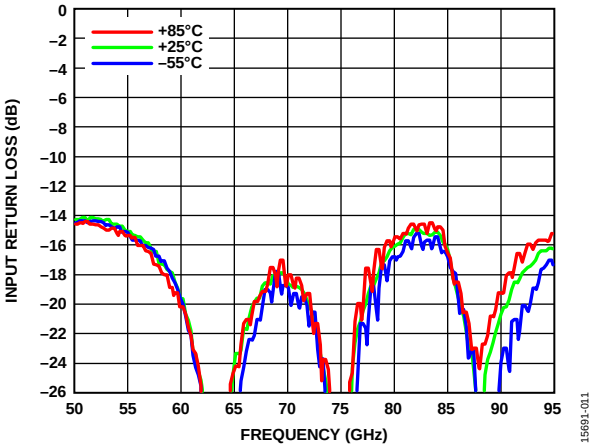

Figure 14. Input Return Loss vs. Frequency at Various Temperatures

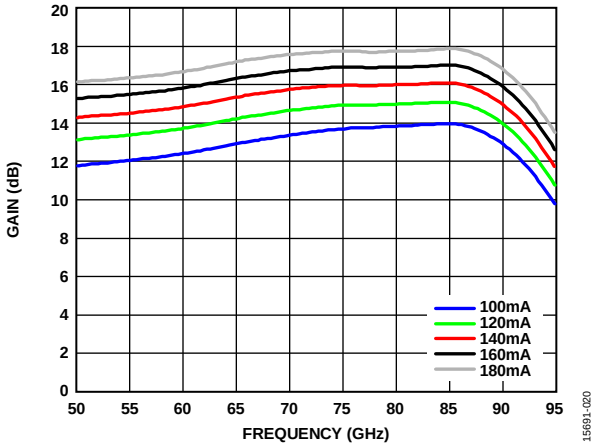

Figure 12. Gain vs. Frequency for Various I_{DQ} Values

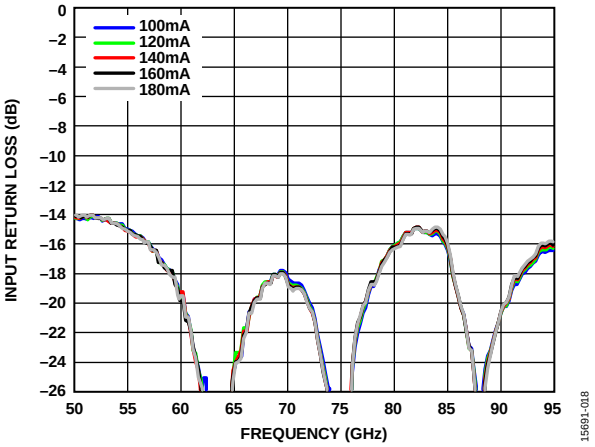

Figure 15. Input Return Loss vs. Frequency for Various I_{DQ} Values

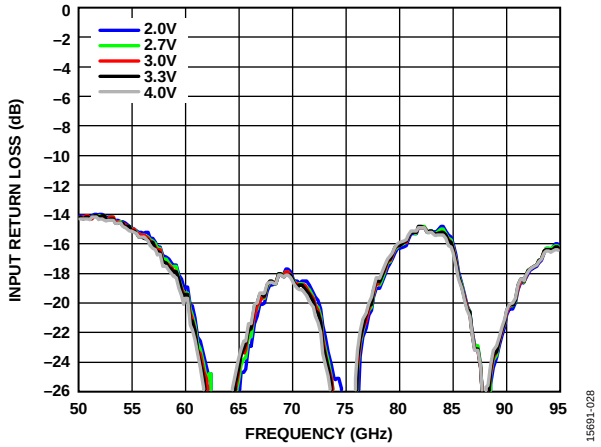

Figure 16. Input Return Loss vs. Frequency for Various V_{DD} Values

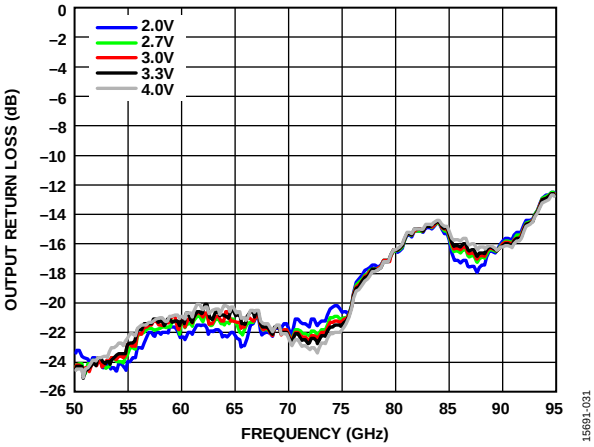

Figure 19. Output Return Loss vs. Frequency for Various V_{DD} Values

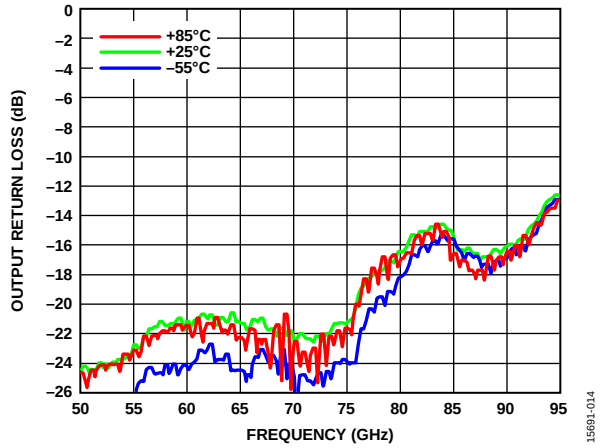

Figure 17. Output Return Loss vs. Frequency for Various Temperatures

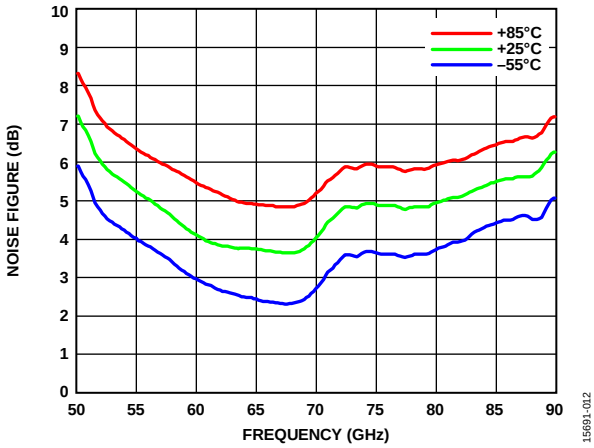

Figure 20. Noise Figure vs. Frequency at Various Temperatures

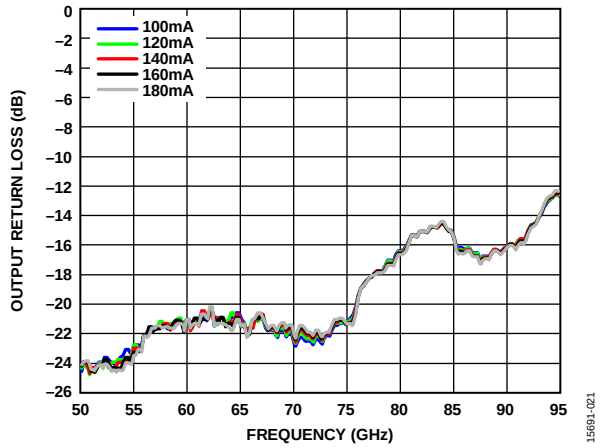

Figure 18. Output Return Loss vs. Frequency for Various I_{DQ} Values

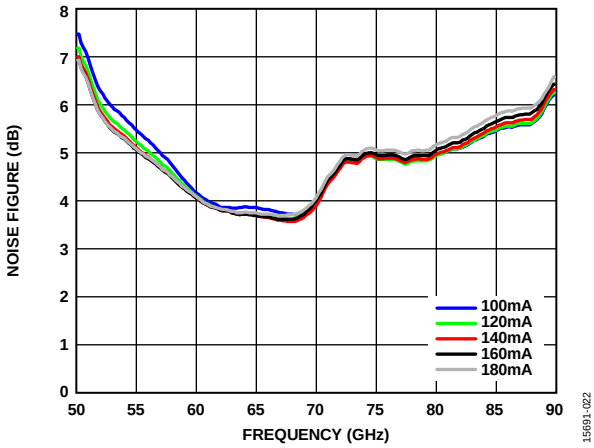

Figure 21. Noise Figure vs. Frequency for Various I_{DQ} Values

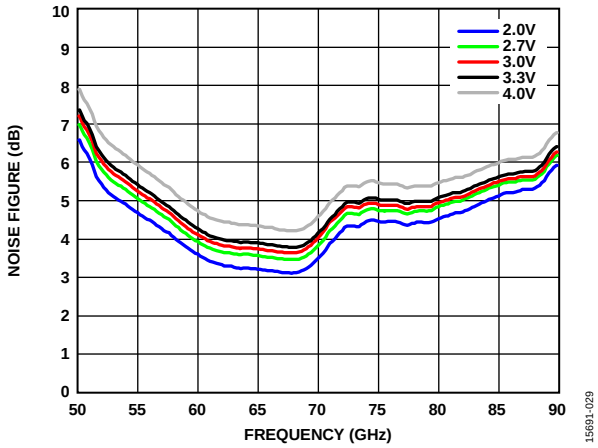

Figure 22. Noise Figure vs. Frequency for Various V_{DD} Values

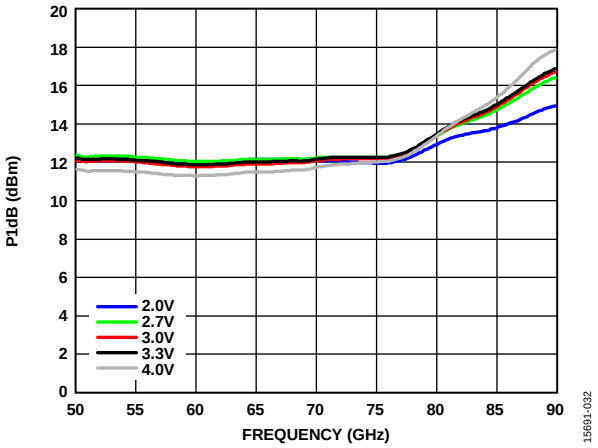

Figure 25. P1dB vs. Frequency for Various V_{DD} Values

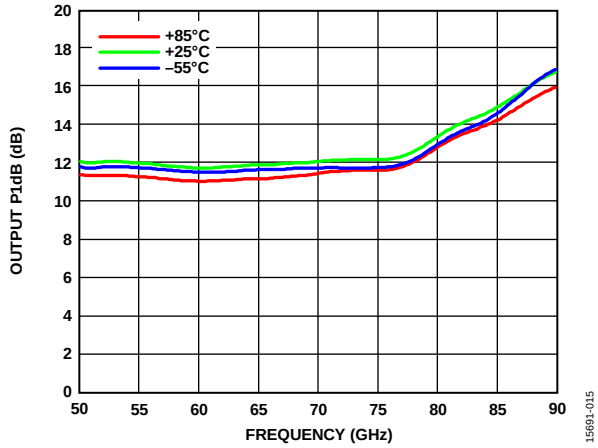

Figure 23. Output P1dB vs. Frequency at Various Temperatures

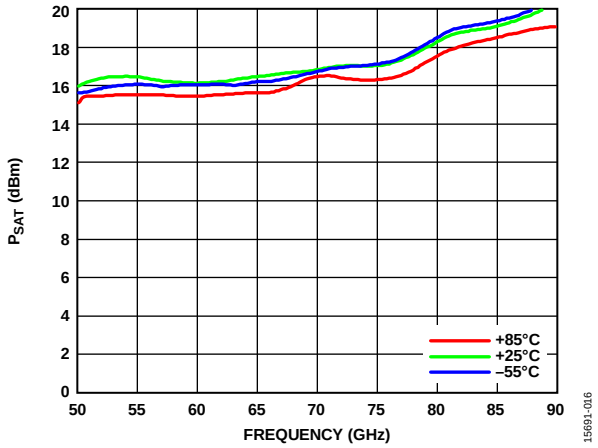

Figure 26. P_{SAT} vs. Frequency at Various Temperatures

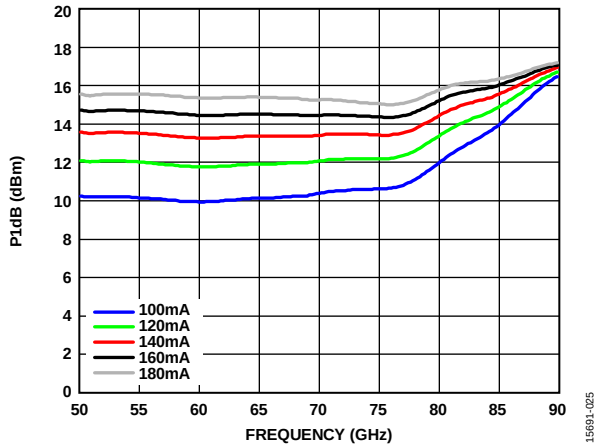

Figure 24. P1dB vs. Frequency for Various I_{DQ} Values

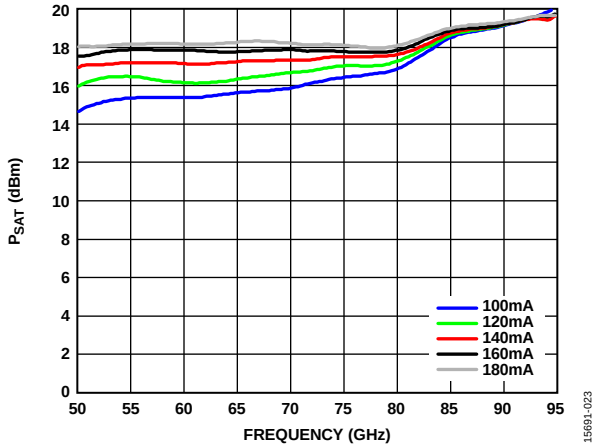

Figure 27. P_{SAT} vs. Frequency at Various I_{DQ} Values

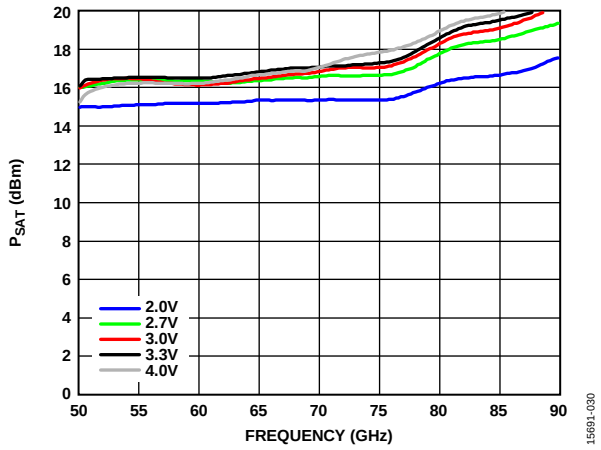

Figure 28. P_{SAT} vs. Frequency for Various V_{DD} Values

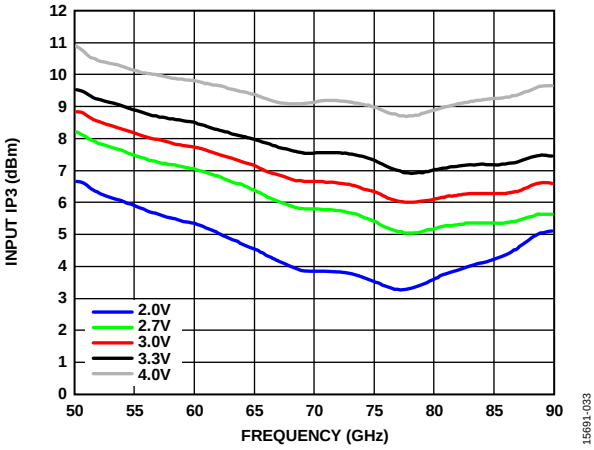

Figure 31. IIP3 vs. Frequency for Various V_{DD} Values

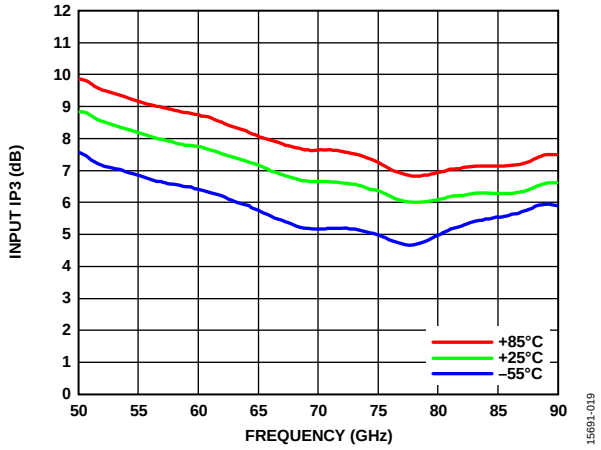

Figure 29. IIP3 vs. Frequency at Various Temperatures

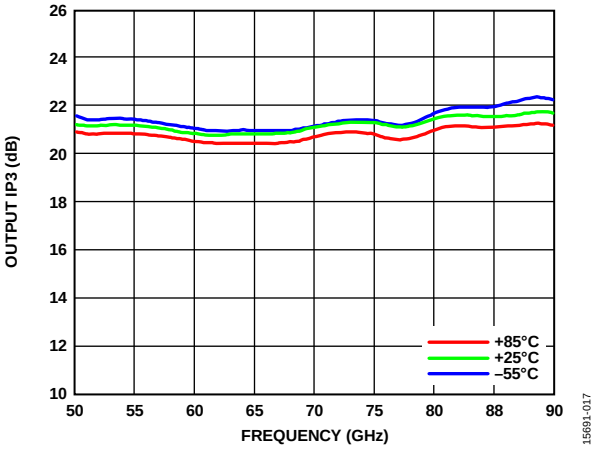

Figure 32. OIP3 vs. Frequency at Various Temperatures

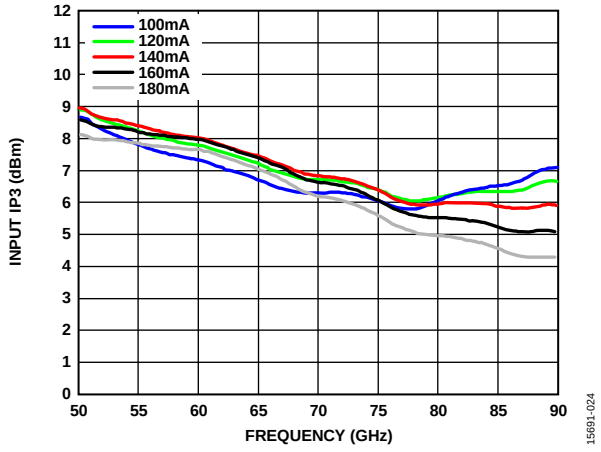

Figure 30. IIP3 vs. Frequency for Various I_{DQ} Values

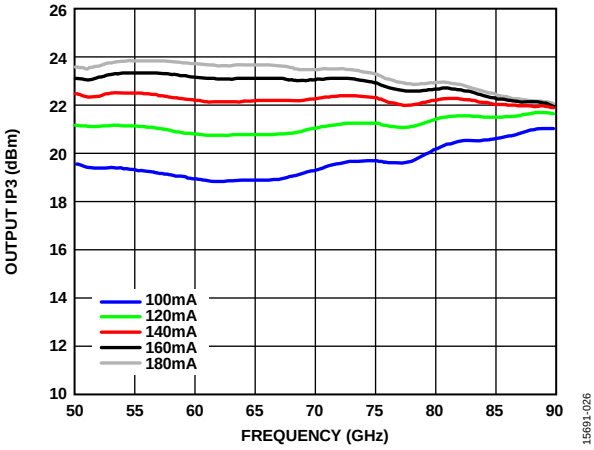

Figure 33. OIP3 vs. Frequency for Various I_{DQ} Values

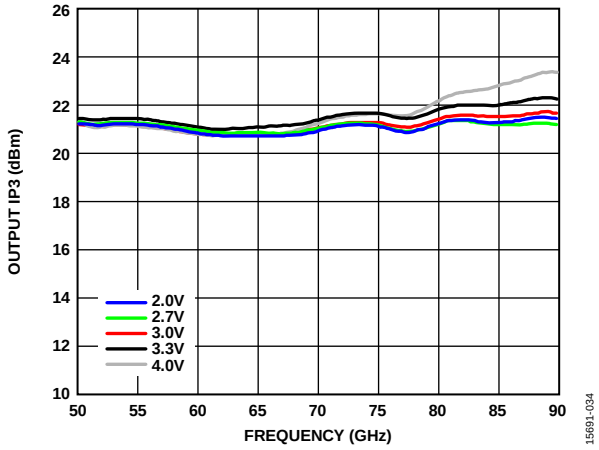

Figure 34. OIP3 vs. Frequency for Various V_{DD} Values

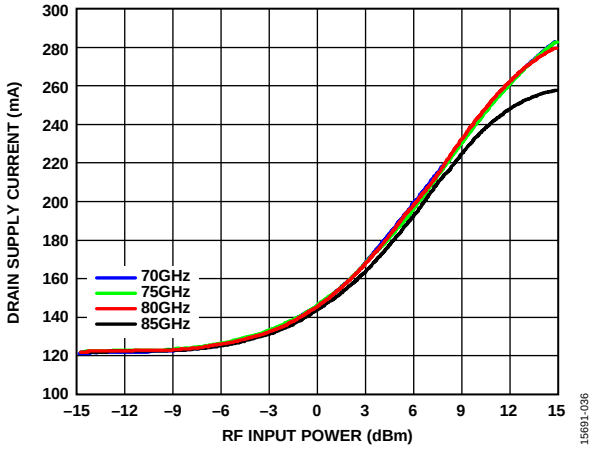

Figure 36. Drain Supply Current (I_{DD}) vs. RF Input Power

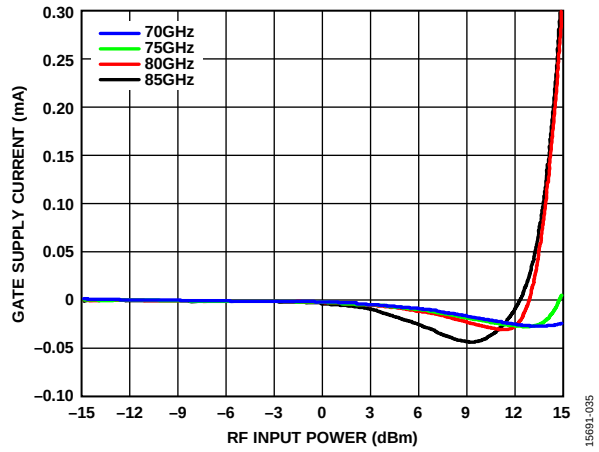

Figure 35. Gate Supply Current (I_{DD}) vs. RF Input Power

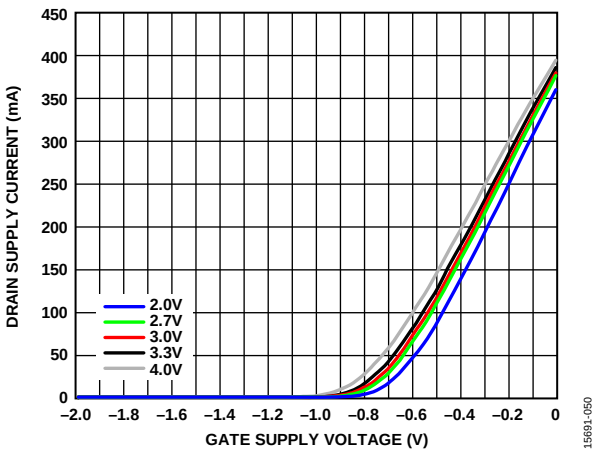

Figure 37. Drain Supply Current (I_{DQ}) vs. Gate Supply Voltage (V_{GG})

THEORY OF OPERATION

The architecture of the ADL7003 low noise amplifier is shown in Figure 38. The ADL7003 uses two cascaded four-stage amplifiers operating in quadrature between two 90° hybrids. This balanced amplifier approach forms an amplifier with a combined gain of 14 dB and a saturated output power (P_{SAT}) of 18 dBm. The 90° hybrids ensure that the input and output return losses are greater than or equal to 15 dB. See the application circuit shown in Figure 41 for further details on biasing the various blocks.

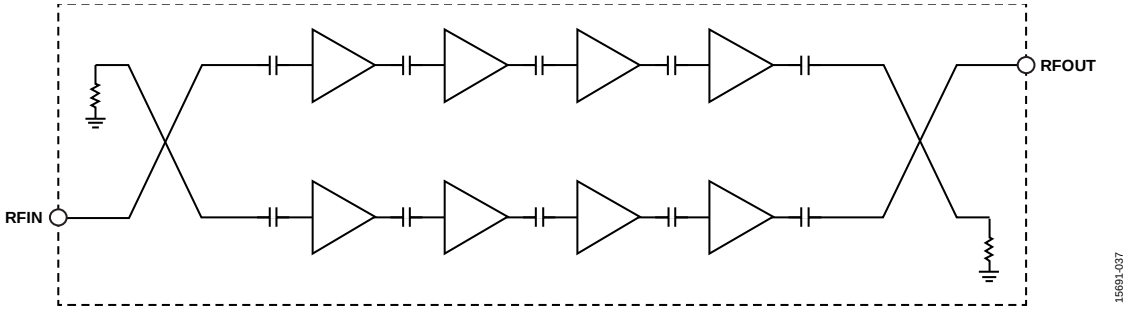

Figure 38. ADL7003 Architecture

APPLICATIONS INFORMATION

The ADL7003 is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for V_{DD}1A through V_{DD}4A and V_{DD}1B through V_{DD}4B (see Figure 41). V_{GG}12A is the gate bias pad for the first two gain stages. V_{GG}34A is the gate bias pad for the second two gain stages. Apply a gate bias voltage to V_{GG}12A and V_{GG}34A, and use capacitive bypassing as shown in Figure 41.

All measurements for this device were taken using the typical application circuit (see Figure 41) and configured as shown in the assembly diagram (Figure 42).

The following is the recommended bias sequence during power-up:

1. Connect to ground.
2. Set the gate bias voltage to −1.5 V.
3. Set all the drain bias voltages, V_{DD} = 3 V.
4. Increase the gate bias voltage to achieve a quiescent current, I_{DD} = 120 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltage to −1.5 V to achieve I_{DD} = 0 mA (approximately).
3. Decrease all of the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

Table 7. Power Selection Table[1]

I_{DQ} (mA)[2]	Gain (dB)	P1dB (dBm)	OIP3 (dBm)	P_{DISS} (mW)	V_{GG} (V)
100	12	10	20	300	−0.52
120	13	12	21	360	−0.49
140	14	13	22	420	−0.44
160	15	14	22.5	480	−0.40
180	16	15	23	540	−0.36

[1] Data taken at nominal bias conditions; V_{DD} = 3 V, T_A = 25°C.
[2] Adjust V_{GG}12A and V_{GG}24A from −1.5 V to 0 V to achieve the desired drain current.

The VDD = 3 V and IDD = 120 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias condition. Operation of the ADL7003 at different bias conditions may provide performance that differs from what is shown in Figure 41. Biasing the ADL7003 for higher drain current typically results in higher P1dB, output IP3, and gain but at the expense of increased power consumption (see Table 7).

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended for bringing the radio frequency to and from the chip. Raise the die 0.075 mm (3 mil) to ensure that the surface of the die is coplanar with the surface of the substrate.

Place microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil). To ensure wideband matching, a 15fF capacitive stub is recommended on the PCB board before the ribbon bond.

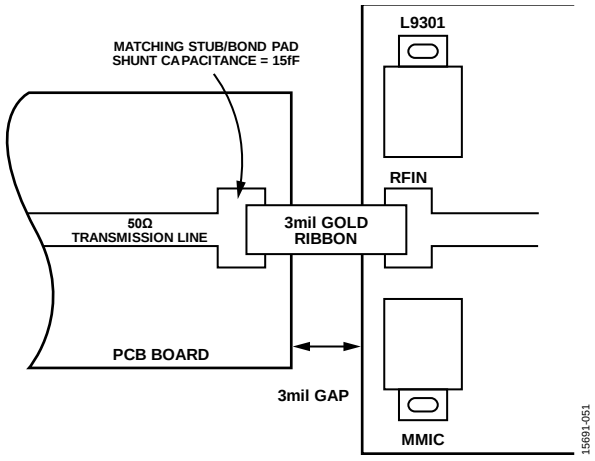

Figure 39. High Frequency Input Wideband Matching

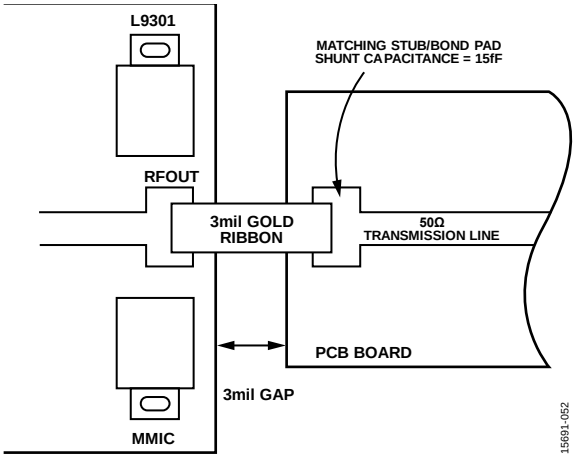

Figure 40. High Frequency Output Wideband Matching

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

Before epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 0.001 in. (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

Alternatively, short (≤3 mil) RF bonds made with two 1-mil wires can be used.

TYPICAL APPLICATION CIRCUIT

The drain and gate voltages can be applied to either the north or the south side of the circuit.

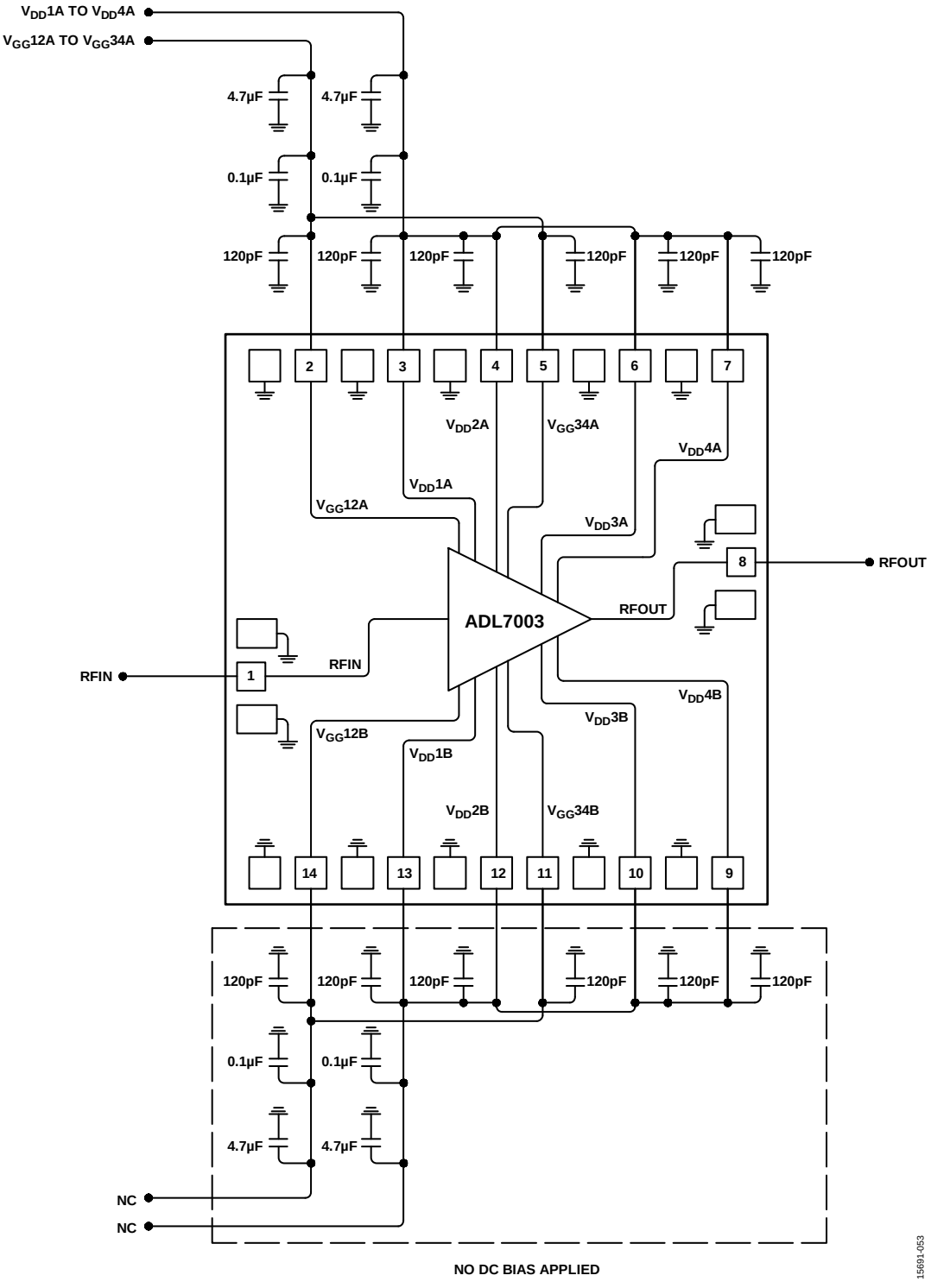

Figure 41. Typical Application Circuit

ASSEMBLY DIAGRAM

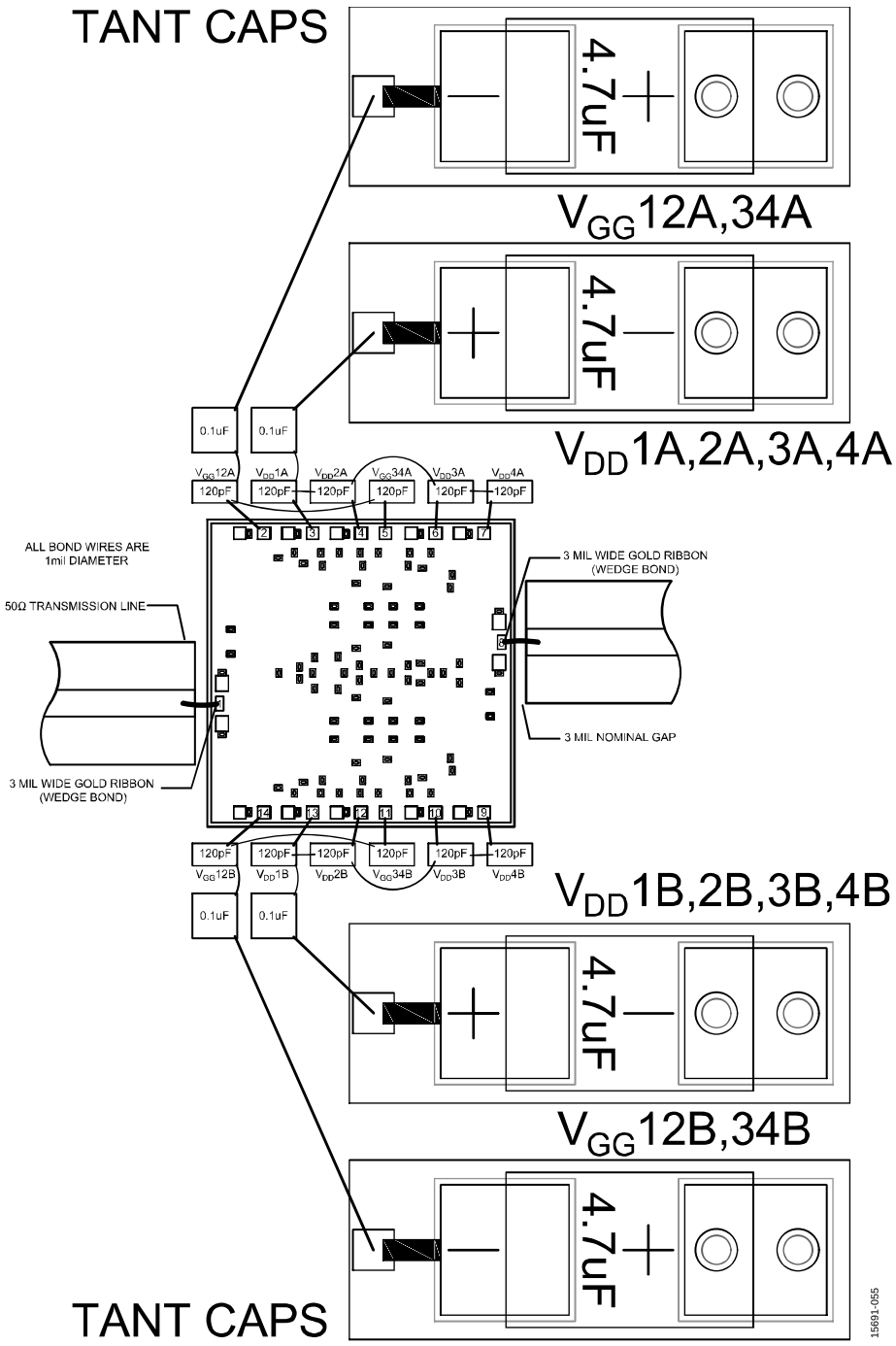

Figure 42. Assembly Diagram

OUTLINE DIMENSIONS

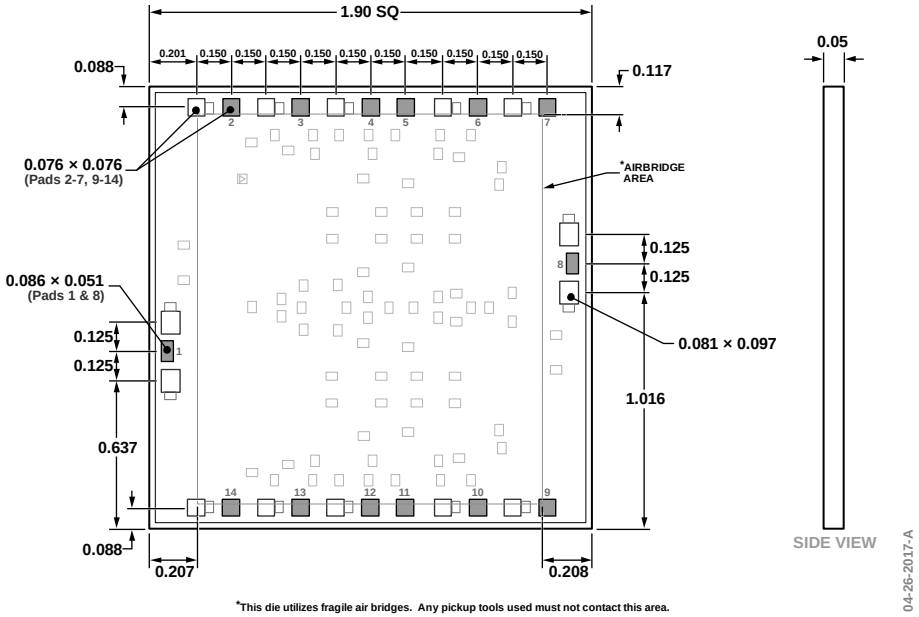

Figure 43. 14-Pad Bare Die [CHIP]
(C-14-5)
Dimensions shown in millimeter

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADL7003CHIPS	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-5
ADL7003CHIPS-SX	−55°C to +85°C	14-Pad Bare Die [CHIP]	C-14-5