BC2102
Sub-1GHz OOK/FSK Transmitter

Features

- Operating voltage:
  - V_{DD}=2.2V~3.6V@Ta= -40°C~+85°C
- Complete Sub-1GHz OOK/FSK transmitter
- Frequency bands: 315MHz, 433MHz, 868MHz, 915MHz
- Supports OOK/FSK modulation
- Supports 2-wire I^2C interface
- Low sleep current
- TX current consumption@433MHz:
  - 17mA (FSK, 10dBm)/11mA (OOK, 10dBm, 50% duty cycle)
- Programmable symbol rate
- On-chip full range VCO and Fractional-N PLL synthesizer
- Supports 16/24 MHz low cost crystal
- 4-steps programmable TX Power: 0/5/10/13 dBm
- Fully integrated VCO, on chip loop filter and PLL synthesizer
- Hardware control mode – MCU not required for radio control
- Integrated 64×1-bit FUSE Data Memory
- Auto calibration function
- Package type: 8-pin SOP-EP

Abbreviation Notes

TX: RF Transmitter

SX: Synthesizer

XO: External Crystal

PA: Power Amplifier

OOK: On-Off Keying

FSK: Frequency Shift Keying

VCO: Voltage Control Oscillator

PLL: Phase Lock Loop

MMD: Multi-Mode Divider

XTAL: External Crystal

General Description

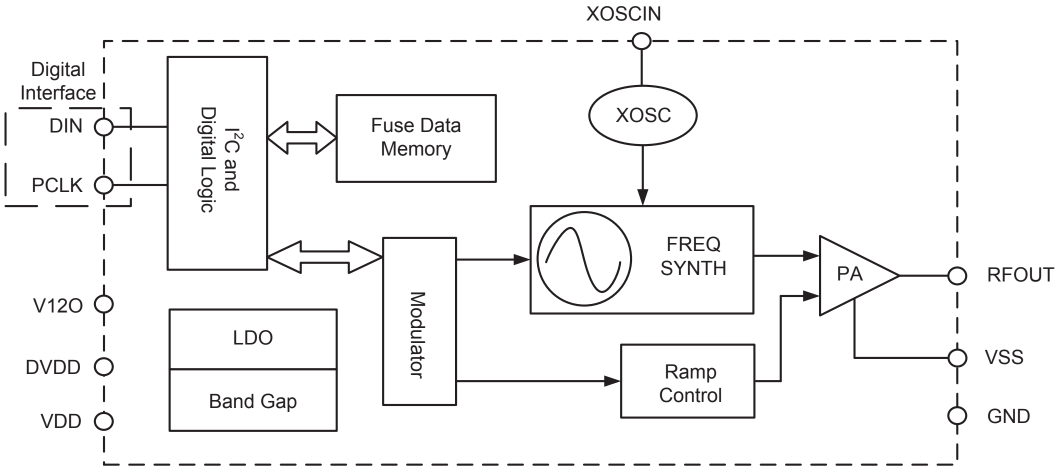
The BC2102 is a highly integrated OOK/FSK transmitter for remote wireless applications. The transmitter is a true "data-in, antenna-out" monolithic device making it very easy for users to implement wireless systems.

The BC2102 can operate at the 315MHz, 433MHz, 868MHz and 915MHz frequency bands. It supports both OOK and FSK modulation schemes and can operate with symbol rate up to 25Kbps and 50Kbps respectively.

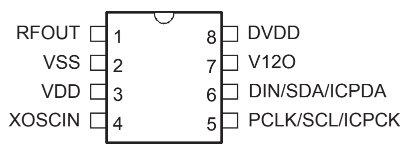
BC2102 offers a programmable output power level. It is capable of delivering +13dBm maximum power into a 50Ω load. The BC2102 adopts an agile state machine to ease the control and minimize the power consumption. With an external crystal and a few external components, BC2102 can implement a complete solution for an effective RF transmitter.

These features can be easily programmed through I^2C interface or internal Fuse. With these combined features the BC2102 can provide a power-saving and cost effective solution for a huge range of remote wireless applications.

Block Diagram



Pin Assignment



BC2102
8 SOP-EP-A

Pin Description

Pin No.	Pin Name	Function	Type	Description
1	RFOUT	PA_OUT	AO	RF output signal from Power Amplifier Connect to matching circuit
2	VSS	PA_GND	PWR	Analog negative power supply, ground
3	VDD	VDD	PWR	Analog positive power supply
4	XOSCIN	Crystal	AI	External crystal input
5	PCLK/SCL/ICPCK	PCLK	I	Clock input
		SCL	I	I^2C clock input
		ICPCK	I	ICP clock input pin
6	DIN/SDA/ICPDA	DIN	I	RF transmitter data input
		SDA	I	I^2C data input
		ICPDA	I	ICP data input pin
7	V12O	LDO_OUT	PWR	1.2V LDO output
8	DVDD	VDD	PWR	Digital positive power supply
9	GND	Ground	PWR	Expose Pad

Note: I: Digital Input   O: Digital Output
AI: Analog Input   AO: Analog Output
PWR: Power

Absolute Maximum Ratings

Supply Voltage .... V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O pins .... V_{SS}-0.3V to V_{DD}+0.3V

ESD HBM .... ±2kV

Storage Temperature .... -55°C to 150°C

Operating Temperature .... -40°C to 85°C

*This device is ESD sensitive. HBM (Human Body Mode) is based on the MIL-STD-883H Method 3015.8.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those has listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16 MHz, OOK/FSK modulation with Matching circuit, PAOUT is powered by V_{DD}=3.3V, unless otherwise noted.

Ta=25°C

Symbol	Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.2	3.3	3.6	V
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{IH}	High Level Input Voltage	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	$0.3V_{DD}$	V
V_{OH}	High Level Output Voltage	@I_{OH} = -5mA	$0.8V_{DD}$	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	@I_{OL} = 5mA	0	—	$0.2V_{DD}$	V
I_{Sleep}	Current Consumptions	—	—	0.1	—	μA
$I_{Standby}$		XTAL On, PA off, Synthesizer On	—	6.5	—	mA
I_H	High Data Current Consumption @315MHz Band (Data=1)	P_{RF} = 0dBm	—	11	—	mA
		P_{RF} = 10dBm	—	20	—	
		P_{RF} = 13dBm	—	26	—	
	High Data Current Consumption @433MHz Band (Data=1)	P_{RF} = 0dBm	—	11	—	mA
		P_{RF} = 10dBm	—	17	—	
		P_{RF} = 13dBm	—	22	—	
	High Data Current Consumption @868MHz Band (Data=1)	P_{RF} = 0dBm	—	12	—	mA
		P_{RF} = 10dBm	—	19	—	
		P_{RF} = 13dBm	—	25	—	
	High Data Current Consumption @ 915MHz Band (Data=1)	P_{RF} = 0dBm	—	12	—	mA
		P_{RF} = 10dBm	—	19	—	
		P_{RF} = 13dBm	—	25	—	

A.C. Characteristics

RF Characteristics

Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RF						
f_{RF}	RF Operating Frequency Range	—	—	315	—	MHz
				433		
				868		
				915		
XTAL						
f_{XTAL}	RF Operating XTAL Frequency	—	16	—	24	MHz
ESR	XTAL Equivalent Series Resistance	—	—	—	100	Ω
C_L	XTAL Capacitor Load	—	—	16	—	pF
	XTAL Tolerance (1)	—	—	±20	—	ppm
$t_{Startup}$	XTAL Startup Time (2)	—	—	1	—	ms
PLL						
f_{STEP}	RF Frequency Synthesizer Step	—	—	0.5	—	kHz
PN_{PLL}	433MHz PLL Phase Noise	Phase Noise @ 100k offset	—	-80	—	dBc/Hz
		Phase Noise @ 1M offset		-104		
	868MHz PLL Phase noise	Phase Noise @ 100k offset	—	-70	—	
		Phase Noise @ 1M offset		-100		
f_{dev}	Frequency Deviation	f_{XTAL} = 16MHz	2	—	100	kHz
TX						
SR	Symbol Rate	OOK modulation	0.5	25	—	kbps
		FSK modulation (@f_{dev}=12.5kHz)	0.5	50	—	
P_{RF}	RF Transmitter Output Power	433MHz	0	—	13	dBm
		868MHz	0	—	13	
t_{ST}	RF Transmitter Settling Time	PLL to transmit	—	370	—	μs
ER_{OOK}	OOK Extinction Ratio	OOK Modulation depth	—	70	—	dB
	Occupied Bandwidth (OOK, -20dBc)	@315MHz	—	400	—	kHz
		@433MHz				
		@868MHz				
		@915MHz				
	Output Blanking	Time from Sleep to RF out	—	—	1	ms
	One Shot Delay Time	OOK/FSK	4	—	32	ms
SE_{TX}	Transmitter Spurious Emission (Pout =10dBm)	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz 87.5 MHz < f < 118MHz 174MHz < f < 230MHz 470MHz < f < 790MHz	—	—	-54	
		2^{nd}, 3^{rd} Harmonic	—	—	-30	

Note: 1. This is the total tolerance including (1) Initial tolerance (2) Crystal loading (3) Aging and (4) Temperature dependence.

The acceptable crystal tolerance depends on RF frequenc and channel spacing/band width.

2. Depend on crystal property.

Functional Description

The fully integrated RF transmitter can operate in the 315MHz, 433MHz, 868MHz and 915MHz frequency bands. The additional of a crystal and a limited number of external components are all that is required to create a complete and versatile RF transmitter system. The device includes an internal power amplifier and is capable of delivering up to +13dBm into a 50Ω load. Such a power level enables a small form factor transmitter to operate near the maximum transmission regulation limits. The device can operate with OOK and FSK receiver types. The FSK data rate is up to 50kbps, allowing the device to support more complicated control protocols.

Solution Overview

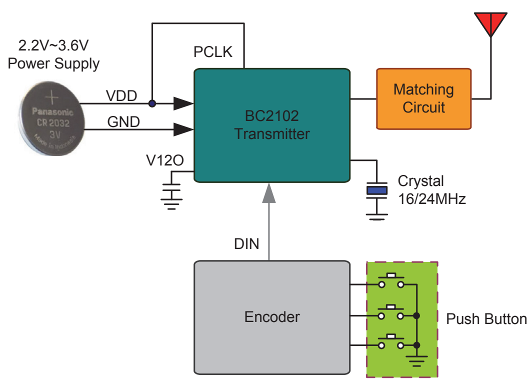
To provide extra user conveniences, the BC2102 contains an area of FUSE memory, which is a kind of popular One-time Programming Non-volatile Memory.

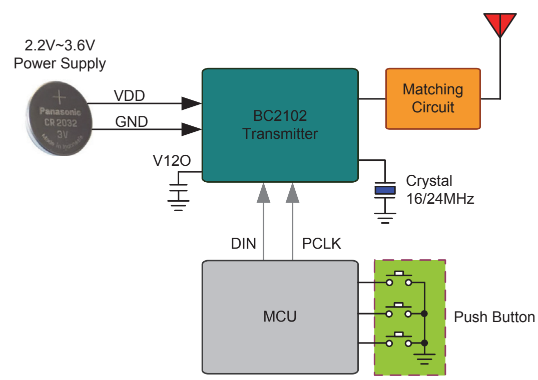
If the FUSE is un-programmed, which can be detected by checking the EFPGM bit in the CFG7 register, the user should connect the device to an MCU and setup the relevant RF registers configuration in the I^2C Mode using an I^2C interface. The device can operate properly after returning to the Normal Mode. However, the registers will be reset to their initial state when the device is powered off.

For devices whose FUSE is programmed, users can implement a complete and versatile RF transmitter system to work together with an external MCU or Encoder. The corresponding application solutions are shown as below. Note that when EFPGM bit is low the device can only be connected to an external MCU.

If the device is connected with an Encoder, the FUSE data will be automatically copied to the corresponding registers. After a delay time, the encoder can send data to the device through the DIN pin and thus start a transmission sequence.

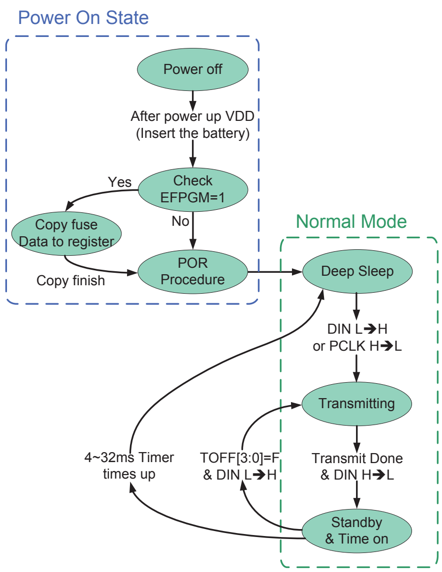
If the device is connected to an MCU, the same function aforementioned can also be implemented. The difference is that the MCU can configure the frequency, power and other parameters by setting the relevant registers using an I^2C interface when operating in the I^2C Mode.



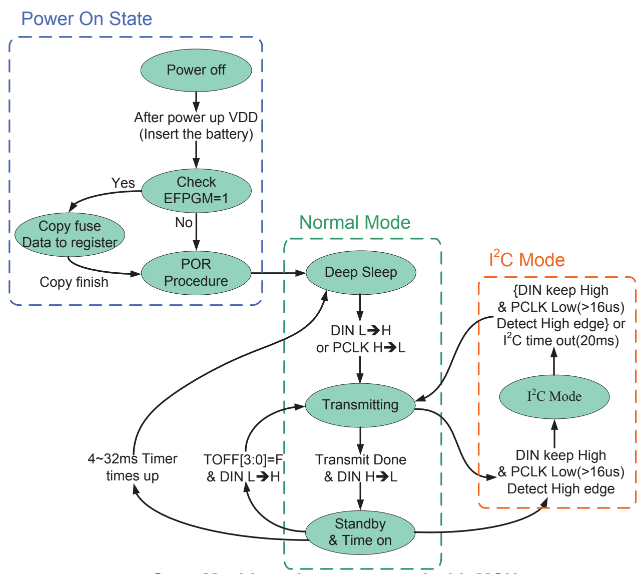


State Control

The BC2102 has integrated state machines that control the state transition between modes.



State Machine when connected with Encoder



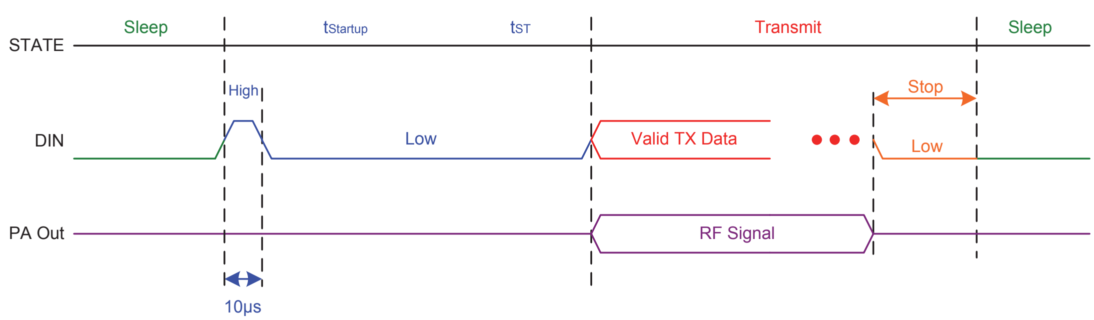
State Machine when connected with MCU

Power On State

After power-on, perhaps by the insertion of a battery, if the EFPGM bit state is high, the FUSE data will be automatically copied to the corresponding registers. When completed the device will enter the Deep Sleep Mode after a POR delay time. Note that the device will directly enter the Deep Sleep Mode after a delay time if the EFPGM bit is low.

Normal Mode

After a power-on reset operation, the device enters the Deep Sleep Mode. Data will be transmitted if the DIN pin is pulled high or the pulse on the PCLK pin changes from high to low. When data transmission is finished and the DIN pin state changes from high to low, the device will enter the Standby state and the Timer, whose timeout period is determined by DLY_TOFF bits in the CFG1 register, will turn on and start to count. The device will return to the Deep Sleep Mode when the Timer overflows. However, it should be noted that when the DLY_TOFF[3:0] bit value is "1111", the device will start to transmit again without entering the Deep Sleep Mode once the DIN pin state changes from low to high.



TX Enabled by DIN Pin

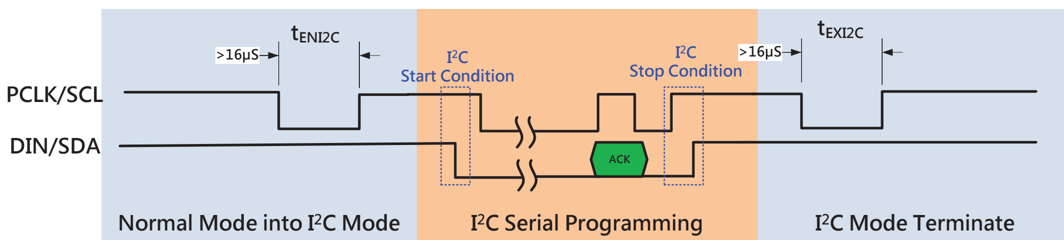
I^2C Mode

If the device is connected to an external MCU, then the I^2C mode can be used. When the SCL line (Pin 5) is pulled low for more than 16μs (t_{ENI2C}), the device will enter the I^2C Mode from the Normal Mode, during which the external control register can configure the special function registers in the device using I^2C commands. When the device receives a correct I^2C STOP signal followed by the SCL line being pulled low for more than 16μs, the device will return to the Normal Mode.

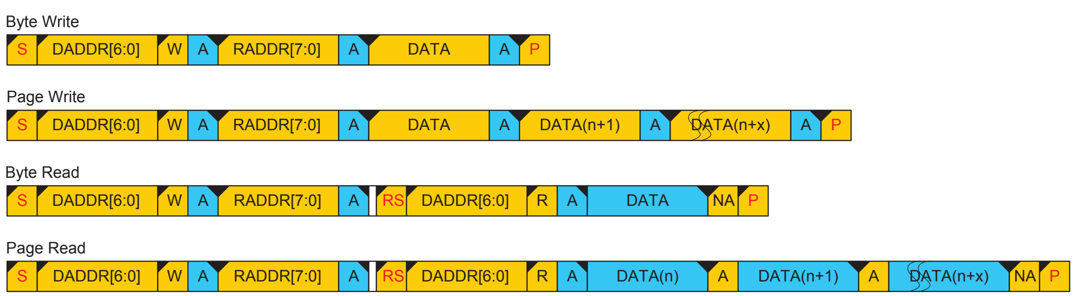
In the I^2C Mode, the MCU can configure the internal relevant registers using I^2C serial programming. The transmitter only supports the I^2C format for byte write, page write, byte read and page read format. The transmission procedure is shown as below.

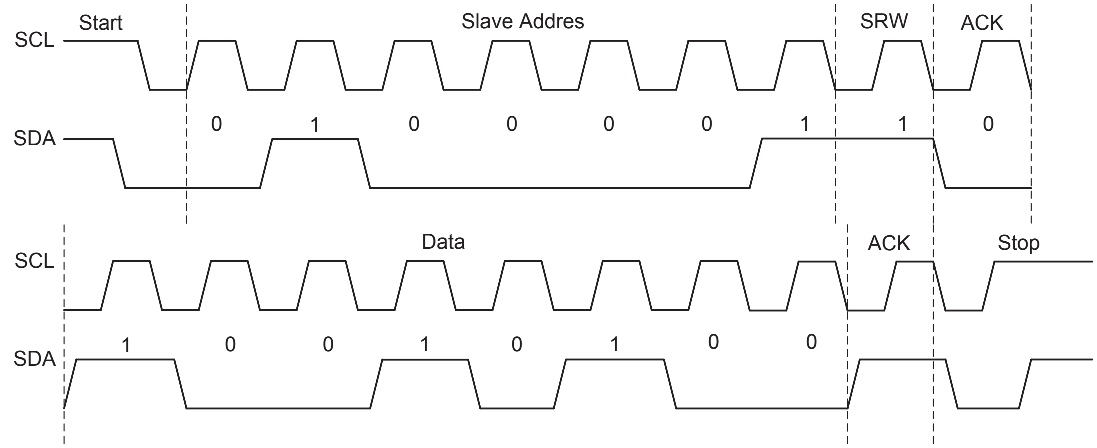
Symbol definition:

- S: Start symbol
- RS: Repeat Start
- P: Stop symbol
- DADDR[6:0]: device address, 21h
- R/W: read write select, R(0): write, (1): read
- RADDR[7:0]: register address
- ACK: A(0):ACK, NA(1):NAK
- Bus Direction:
  host to device:
  device to host:



I^2C Serial Programming





S = Start (1 bit)
SA = Slave Address (7 bits)
SR = SRW bit (1 bit)
M = Slave device send acknowledge bit (1 bit)
D = Data (8 bits)
A = ACK (RXAK bit for transmitter, TXAK for receiver, 1bit)
P = Stop (1 bit)

S	SA	SR	M	D	A	D	A	···	SR	SA	SR	M	D	A	D	A	···	P

Note: *When a slave address is matched, the device must be placed in either the transmit mode and then Write data to the SIMD register, or the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.

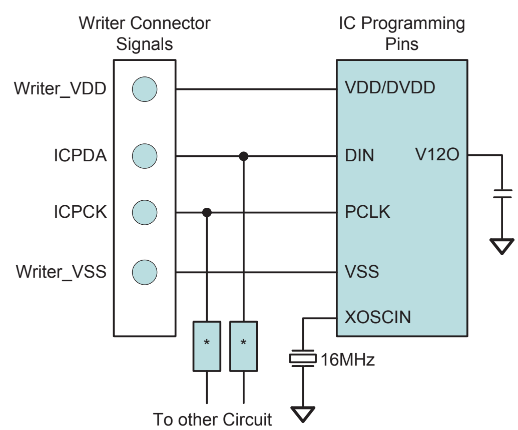
I^2C Communication Timing Diagram

Programming Methodology

The device programming interface should utilise an adaptor with an integrated 16MHz crystal.

Program Function	Pin Name	Pin Description
ICPCK	PCLK (Pin5)	ICP clock
ICPDA	DIN (Pin)	ICP Data/Address
VDD	VDD (Pin3) DVDD (Pin8)	Power supply
VSS, EP	VSS (Pin2), Exposed-Pad	Ground
XTAL IN (Adaptor)	XOSCIN (Pin4)	IC system clock

When programming, the device needs to be located on a Socket with a 16MHz crystal connected between Pin XOSCIN and ground. Holtek provides an e-link or e-WriterPro tool for communication with the PC. Between the e-link and the device there are four interconnecting lines, namely VDD, VSS, PCLK and DIN pins.



Note: * may be resistor or capacitor – the resistance of * must be greater than 1kΩ and the capacitance of * must be less than 1nF.

Register Map

When connected to an external MCU, the device can be setup and operated using a series of internal registers. Device commands and data are written to and read from the device using its internal I^2C bus. This list provides a summary of all internal registers. Their detailed operation is described under their relevant section in the functional description.

<table>
<tr><th rowspan="2">Address</th><th rowspan="2">Register Name</th><th colspan="8">Bit</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00h</td><td>CFG0</td><td colspan="2">XO_SEL</td><td colspan="6">XO_TRIM[5:0]</td></tr>
<tr><td>01h</td><td>CFG1</td><td colspan="4">DLY_TOFF[3:0]</td><td colspan="4">Setting1</td></tr>
<tr><td>02h</td><td>CFG2</td><td colspan="8">FDEV[7:0]</td></tr>
<tr><td>03h</td><td>CFG3</td><td>FSK_SEL</td><td colspan="3">Setting2</td><td colspan="4">TXPWR[3:0]</td></tr>
<tr><td>04h</td><td>CFG4</td><td colspan="6">D_N[5:0]</td><td colspan="2">BAND_SEL[1:0]</td></tr>
<tr><td>05h</td><td>CFG5</td><td colspan="8">D_K[11:4]</td></tr>
<tr><td>06h</td><td>CFG6</td><td colspan="8">D_K[19:12]</td></tr>
<tr><td>07h</td><td>CFG7</td><td>EFPGM</td><td colspan="7">Setting3</td></tr>
</table>

CFG0: Configuration Control Register 0

<table>
<tr><th>Address</th><th>Bit</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="3">00h</td><td>Name</td><td colspan="2">XO_SEL</td><td colspan="6">XO_TRIM[5:0]</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>Initial Value</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

Bit 7~6 **XO_SEL**: External Crystal Selection
- 00: Reserved
- 01: 24MHz X'tal
- 10: 16MHz X'tal
- 11: Reserved

Bit 5~0 **XO_TRIM[5:0]**: Trim value for the internal capacitor load for the crystal

XO_TRIM[5:0]	Equiv. C_L (pF)
0	11.676
4	11.822
8	11.927
12	13.247
16	13.962
17	14.137
18	14.295
20	14.639
24	15.301
28	15.955
32	16.651
36	17.288
40	17.962
44	18.610
48	19.294
52	19.870
56	20.472
60	21.003
63	21.411

CFG1: Configuration Control Register 1

Address	Bit	7	6	5	4	3	2	1	0
01h	Name	DLY_TOFF[3:0]				Setting1			
	R/W	R/W				R/W			R/W
	Initial Value	1	1	1	0	0	0	0	1

Bit 7~4 **DLY_TOFF[3:0]**: Transmitter Auto Power Off Delay Time
t = 2ms×(DLY_TOFF[3:0]+2)
0000: 4ms
0001: 6ms
0010: 8ms
:
1110: 32ms
1111: Infinite – Never enter the Deep Sleep Mode

Bit 3~0 **Setting1**: Must be [0b0001]

CFG2: Configuration Control Register 2

Address	Bit	7	6	5	4	3	2	1	0
02h	Name	FDEV[7:0]							
	R/W	R/W							
	Initial Value	0	1	1	0	0	1	1	0

Bit 7~0 **FDEV[7:0]**: Frequency deviation for FSK
When External Crystal = 24MHz, FDEV = ($f_{dev} \times 2^{14}$ / Fxtal); Fxtal=12MHz
When External Crystal = 16MHz, FDEV = ($f_{dev} \times 2^{15}$ / Fxtal); Fxtal=16MHz
Examples are as follows:
Default FDEV[7:0]=01100110 → Decimal 102
External Crystal = 16MHz
f_{dev} (Frequency deviation) = FDEV × (16M / 2^{15})
f_{dev} (Frequency deviation) = 102 × (16M / 32768) = 49.8kHz

CFG3: Configuration Control Register 3

Address	Bit	7	6	5	4	3	2	1	0
03h	Name	FSK_SEL	Setting2			TXPWR[3:0]			
	R/W	R/W	R/W			R/W			
	Initial Value	0	1	0	0	1	0	0	0

Bit 7 **FSK_SEL**: FSK Mode Enable
0: OOK
1: FSK

Bit 6~4 **Setting 2**: Must be [0b100]

Bit 3~0 **TXPWR[3:0]**: RF Output Power
The device has several output power values which are 0, 5, 10, and 13 dBm for all temperatures.

TXPWR[3:0]	RF Output Power	TXPWR[3:0]	RF Output Power
0000	0dBm	1000	10dBm
0100	5dBm	1100	13dBm

CFG4: Configuration Control Register 4

Address	Bit	7	6	5	4	3	2	1	0
04h	Name	D_N[5:0]						BAND_SEL[1:0]	
	R/W	R/W						R/W	
	Initial Value	0	1	0	1	1	0	0	1

Bit 7~2 **D_N[5:0]**: Integer of dividend for MMD

Bit 1~0 **BAND_SEL[1:0]**: Band Frequency Coarse Control

BAND_SEL	Frequency
00	315MHz
01	433MHz
10	868MHz
11	915MHz

Note that the BAND_SEL only select an approximate frequency range while the exact frequency value is determined by the D_N and D_K bit fields.

CFG5: Configuration Control Register 5

Address	Bit	7	6	5	4	3	2	1	0
05h	Name	D_K[11:4]							
	R/W	R/W							
	Initial Value	0	1	1	1	0	0	0	0

CFG6: Configuration Control Register 6

Address	Bit	7	6	5	4	3	2	1	0
06h	Name	D_K[19:12]							
	R/W	R/W							
	Initial Value	0	0	1	1	1	1	0	1

D_K[19:4]: 16-bit Fractional of dividend for MMD

D_N&D_K example.

X'TAL=16MHz and TX band =433MHz

1. D_N → (433M×Divider)/16M=54.125
   Take the integer part → D_N=54-32=22 → 010110
2. D_K → (433M×Divider)/16M=54.125
   Take the fractional part → D_K=0.125×2^{20}=131072 → 0010-0000-0000-0000
3. 24MHz X'TAL calculation:
   (433M×Divider)/(24M/2)=72.16666667
   Take the integer part → D_N=72-32=40 → 101000
   Take the fractional part → D_K=0.16666667×2^{20}=174762 → 0010-1010-1010-1010
4. The example frequency can be refered in the following table.

Band_SEL	Frequency	Divider	X'TAL	D_N[5:0]	D_K[19:4]
315MHz	315MHz	2	24MHz	010100	1000-0000-0000-0000
			16MHz	000111	0110-0000-0000-0000
433MHz	433MHz	2	24MHz	101000	0010-1010-1010-1010
			16MHz	010110	0010-0000-0000-0000
433MHz	433.92MHz	2	24MHz	101000	0101-0001-1110-1011
			16MHz	010110	0011-1101-0111-0000
868MHz	868MHz	1	24MHz	101000	0101-0101-0101-0101
			16MHz	010110	0100-0000-0000-0000
915MHz	915MHz	1	24MHz	101100	0100-0000-0000-0000
			16MHz	011001	0011-0000-0000-0000

CFG7: Configuration Control Register 7

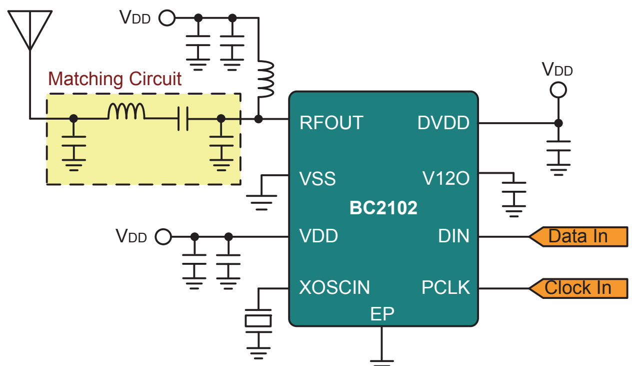
Address	Bit	7	6	5	4	3	2	1	0
07h	Name	EFPGM	Setting3						
	R/W	R	R/W				R/W		R/W
	Initial Value	0	1	0	0	1	0	1	1

Bit 7 **EFPGM**: Fuse programmed, read only for I^2C
0: FUSE is not programmed – FUSE data is not mapped to the configuration register
1: FUSE is programmed – FUSE data is mapped to the configuration register

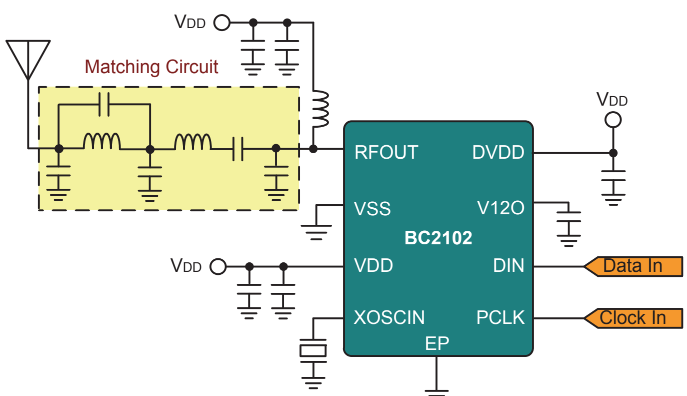
Bit 6~0 **Setting3**: Must be [0b1001011]

Application Circuits

433MHz Application Example



Evaluation Board Circuit



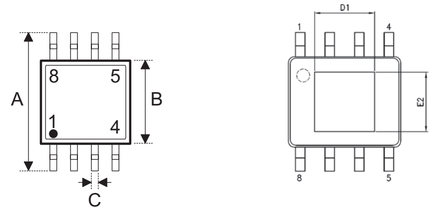
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

8-pin SOP (150mil) Outline Dimensions (Exposed Pad)



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.059	—	—
E	—	0.050 BSC	—
E2	0.039	—	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.50	—	—
E	—	1.27 BSC	—
E2	1.00	—	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

Copyright© 2016 by HOLTEK SEMICONDUCTOR INC.

The information appearing in this Data Sheet is believed to be accurate at the time of publication. However, Holtek assumes no responsibility arising from the use of the specifications described. The applications mentioned herein are used solely for the purpose of illustration and Holtek makes no warranty or representation that such applications will be suitable without further modification, nor recommends the use of its products for application that may present a risk to human life due to malfunction or otherwise. Holtek's products are not authorized for use as critical components in life support devices or systems. Holtek reserves the right to alter its products without prior notification. For the most up-to-date information, please visit our web site at http://www.holtek.com.tw/en/home.