



PJQ1900

20V N-Channel Enhancement Mode MOSFET

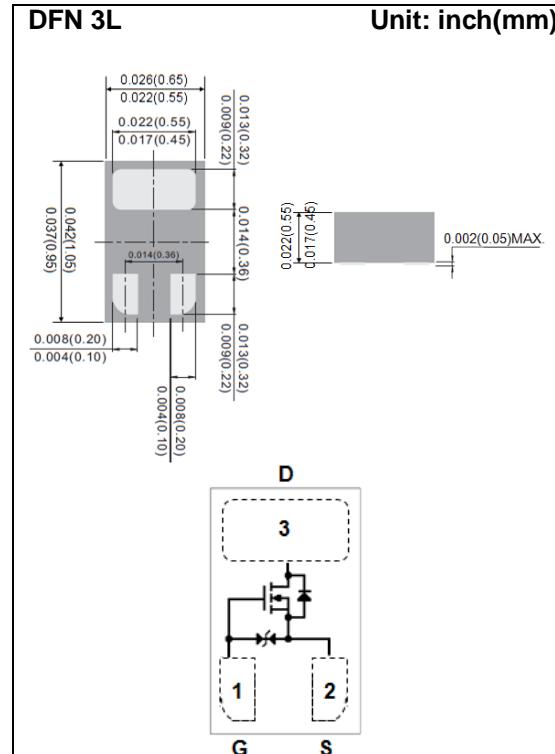
Voltage 20 V Current 1.2 A

Features

- Low Voltage Drive (1.2V).
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: DFN 3L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00004 ounces, 0.0011 grams
- Marking: 0



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current <small>$T_A=25^\circ\text{C}$</small>	I_D	1.2	A
		2.0	
Pulsed Drain Current, $t_p \leq 10\mu\text{s}$	I_{DM}	4.0	A
Power Dissipation <small>$T_A=25^\circ\text{C}$</small>	P_D	900	mW
		7.2	$\text{mW}/^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Typical Thermal resistance - Junction to Ambient, $t < 10\text{s}$ <small>(Note 4)</small>	$R_{\theta JA}$	139	$^\circ\text{C}/\text{W}$



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	-	-	V
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.3	0.65	0.9	V
Drain-Source On-State Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=600\text{mA}$	-	300	400	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=200\text{mA}$	-	350	650	
		$V_{\text{GS}}=1.8\text{V}, I_{\text{D}}=100\text{mA}$	-	400	800	
		$V_{\text{GS}}=1.5\text{V}, I_{\text{D}}=50\text{mA}$	-	500	1200	
		$V_{\text{GS}}=1.2\text{V}, I_{\text{D}}=20\text{mA}$	-	1000	3000	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=16\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 8\text{V}, V_{\text{DS}}=0\text{V}$	-	± 0.5	± 10	μA
Dynamic <small>(Note 6)</small>						
Total Gate Charge	Q_g	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=300\text{mA}, V_{\text{GS}}=4.5\text{V}$ <small>(Note 2)</small>	-	1.4	-	nC
Gate-Source Charge	Q_{gs}		-	0.22	-	
Gate-Drain Charge	Q_{gd}		-	0.21	-	
Input Capacitance	C_{iss}	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, f=1.0\text{MHz}$	-	67	-	pF
Output Capacitance	C_{oss}		-	19	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=10\text{V}, I_{\text{D}}=150\text{mA}, V_{\text{GS}}=4.0\text{V}, R_{\text{G}}=10\Omega$ <small>(Note 1,2)</small>	-	2.8	-	ns
Turn-On Rise Time	t_{r}		-	20	-	
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	23	-	
Turn-Off Fall Time	t_{f}		-	23	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	300	mA
Diode Forward Voltage	V_{SD}	$I_s=300\text{mA}, V_{\text{GS}}=0\text{V}$	-	0.87	1.3	V

NOTES :

1. Pulse width $\leq 300\text{us}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. Tsp is the temperature at the soldering point of the source lead.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1inch FR-4 with 2oz. square pad of copper.
5. The maximum current rating is package limited
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

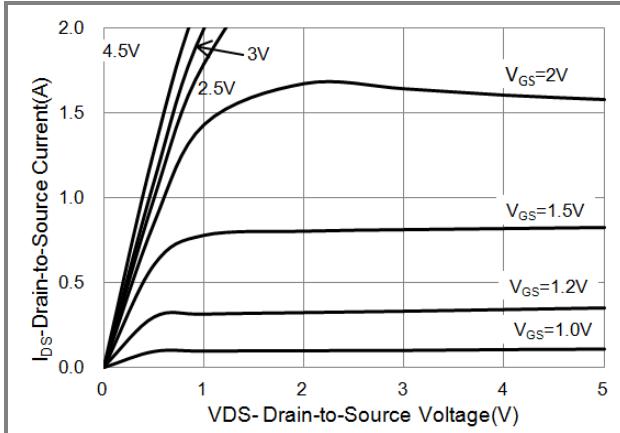


Fig.1 On-Region Characteristics

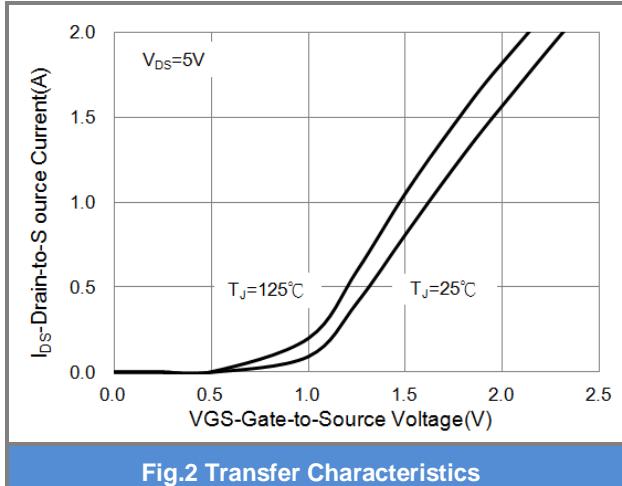


Fig.2 Transfer Characteristics

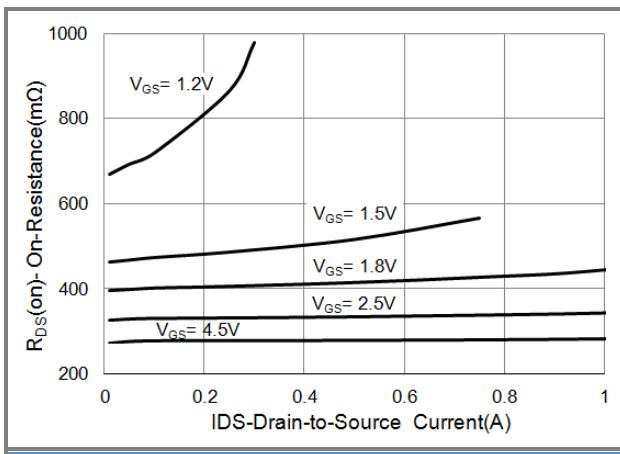


Fig.3 On-Resistance vs. Drain Current

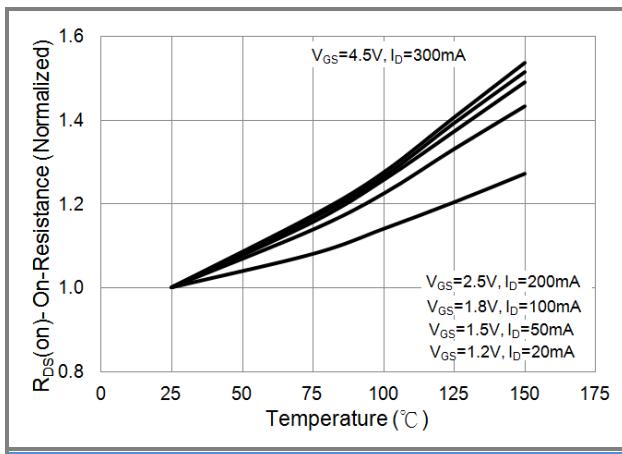


Fig.4 On-Resistance vs. Junction temperature

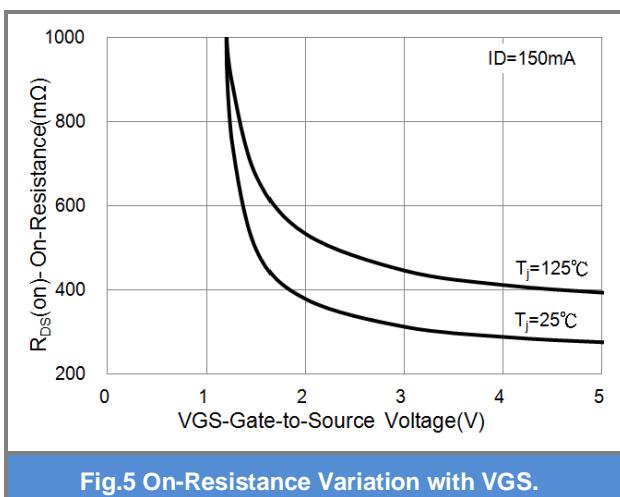


Fig.5 On-Resistance Variation with VGS.

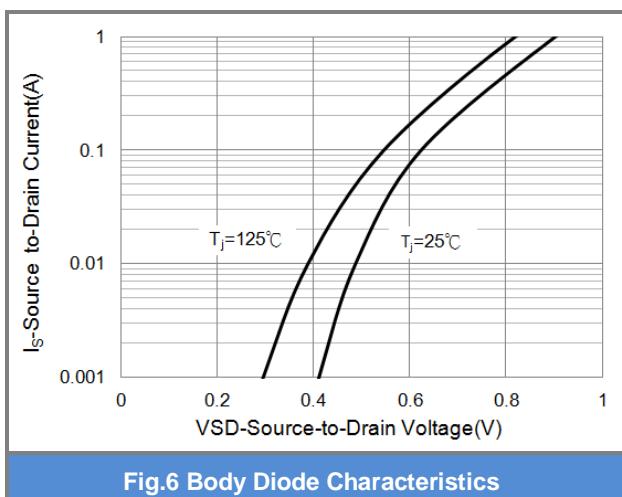


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

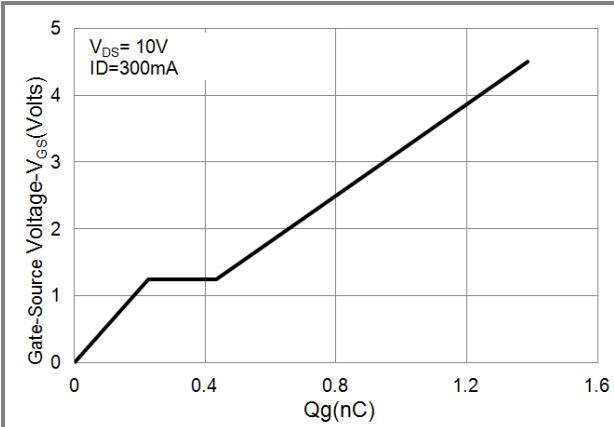


Fig.7 Gate-Charge Characteristics

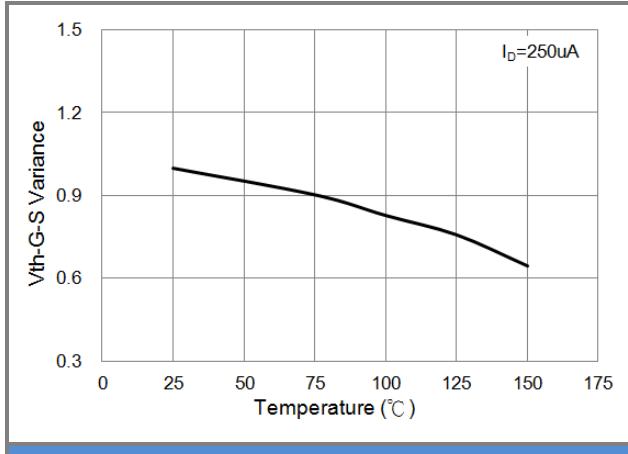


Fig.8 Threshold Voltage Variation with Temperature.

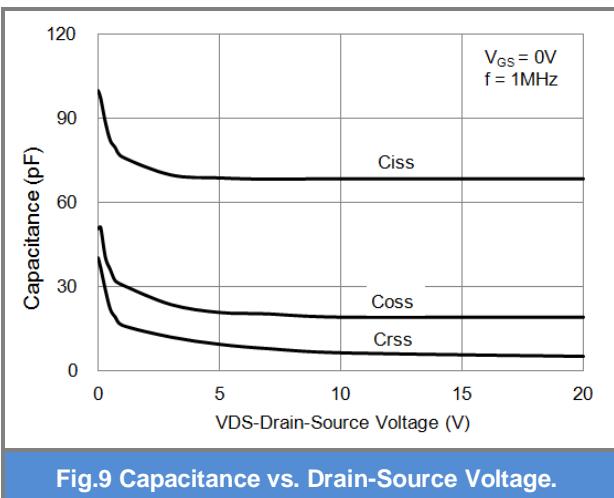


Fig.9 Capacitance vs. Drain-Source Voltage.

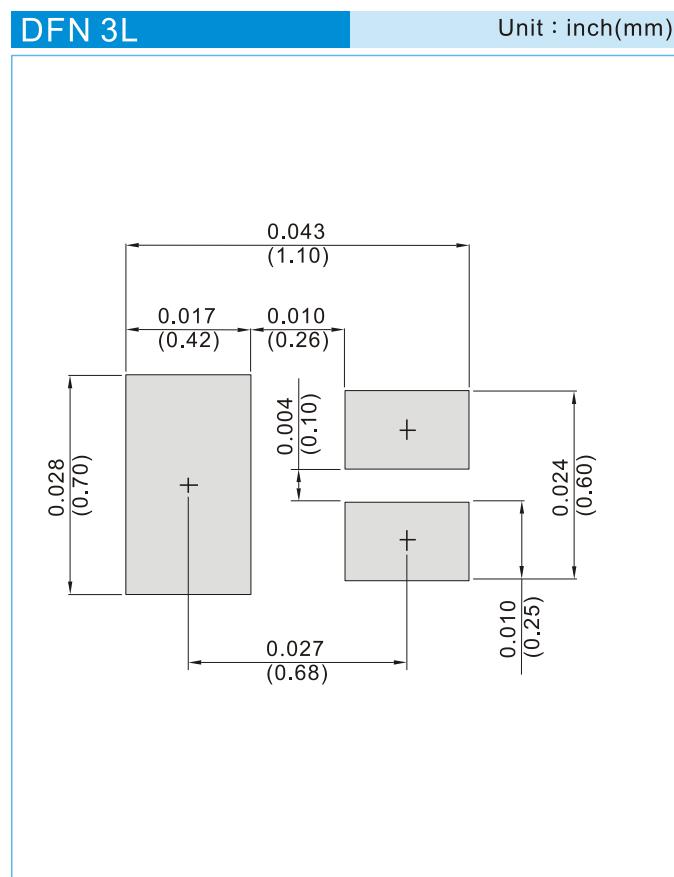


PJQ1900

PART NO PACKING CODE VERSION

PART NO PACKING CODE	Package Type	Packing type	Marking	Version
PJQ1900_R1_00001	DFN 3L	8K pcs / 7" reel	0	Halogen free

MOUNTING PAD LAYOUT





PJQ1900

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