



## PJQ1902

### 30V N-Channel Enhancement Mode MOSFET – ESD Protected

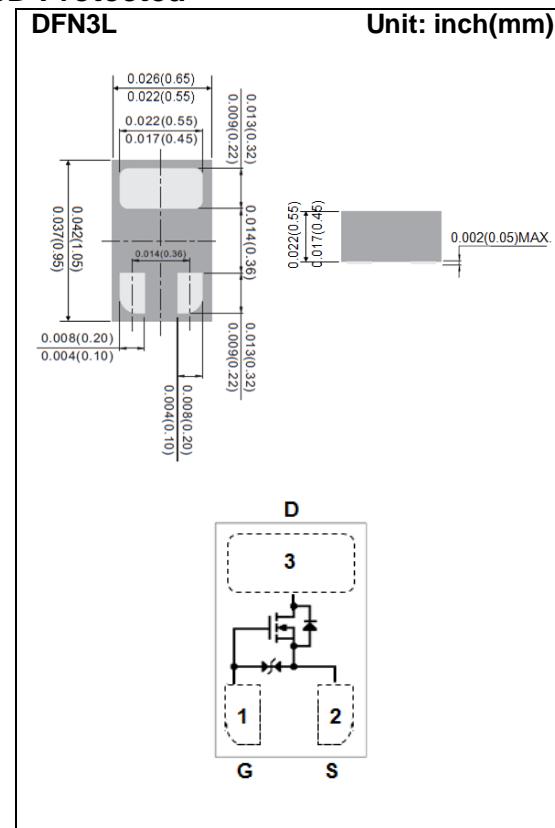
**Voltage**    **30 V**    **Current**    **500mA**

#### Features

- R<sub>DS(ON)</sub> , V<sub>GS</sub>@4.5V, I<sub>D</sub>@350mA<1.2Ω
- R<sub>DS(ON)</sub> , V<sub>GS</sub>@2.5V, I<sub>D</sub>@200mA<1.6Ω
- R<sub>DS(ON)</sub> , V<sub>GS</sub>@1.8V, I<sub>D</sub>@80mA<2.3Ω
- R<sub>DS(ON)</sub> , V<sub>GS</sub>@1.5V, I<sub>D</sub>@10mA<2.5Ω(typ.)
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.  
(Halogen Free)

#### Mechanical Data

- Case: DFN3L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00004 ounces, 0.0011 grams
- Marking: 2



#### Maximum Ratings and Thermal Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±10	V
Continuous Drain Current	I <sub>D</sub>	500	mA
Pulsed Drain Current	I <sub>DM</sub>	1500	mA
Power Dissipation	T <sub>a</sub> =25°C	700	mW
	Derate above 25°C	5.6	mW/°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55~150	°C
Typical Thermal resistance - Junction to Ambient <sup>(Note 3)</sup>	R <sub>θJA</sub>	175	°C/W



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### Electrical Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6	0.85	1.1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=350mA$	-	0.94	1.2	$\Omega$
		$V_{GS}=2.5V, I_D=200mA$	-	1.32	1.6	
		$V_{GS}=1.8V, I_D=80mA$	-	1.82	2.3	
		$V_{GS}=1.5V, I_D=10mA$	-	2.5	-	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	0.01	1	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 8V, V_{DS}=0V$	-	-	$\pm 10$	
		$V_{GS}=\pm 5V, V_{DS}=0V$	-	-	$\pm 1$	
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=350mA,$ $V_{GS}=4.5V$ (Note 1,2)	-	0.87	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.26	-	
Gate-Drain Charge	$Q_{gd}$		-	0.16	-	
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0MHz$	-	34	-	pF
Output Capacitance	$C_{oss}$		-	8.9	-	
Reverse Transfer Capacitance	$C_{rss}$		-	2.5	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=80mA,$ $V_{GS}=4.0V,$ $R_G=6\Omega$ (Note 1,2)	-	7.1	-	ns
Turn-On Rise Time	$t_r$		-	20	-	
Turn-Off Delay Time	$t_{d(off)}$		-	41	-	
Turn-Off Fall Time	$t_f$		-	31	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_s$	---	-	-	350	mA
Diode Forward Voltage	$V_{SD}$	$I_s=350mA, V_{GS}=0V$	-	0.88	1.3	V

#### NOTES :

1. Pulse width $\leq 300\mu s$ , Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
4. The maximum current rating is package limited
5. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

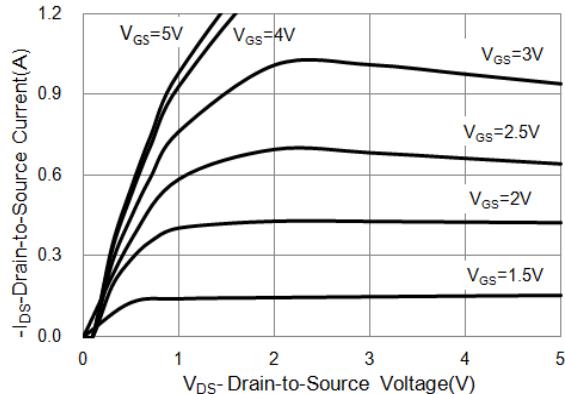


Fig.1 On-Region Characteristics

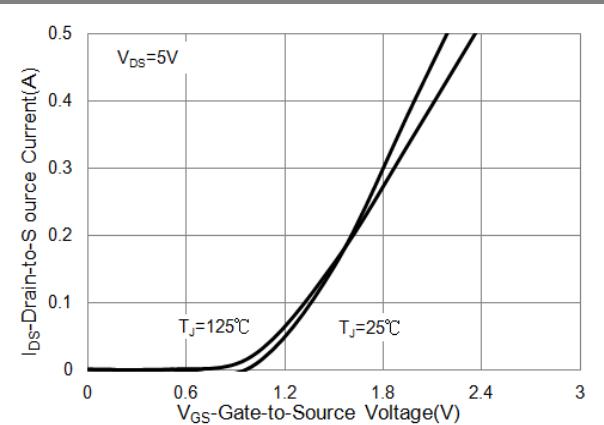


Fig.2 Transfer Characteristics

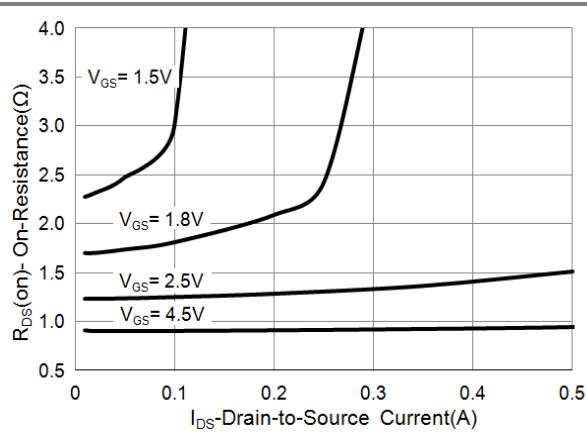


Fig.3 On-Resistance vs. Drain Current

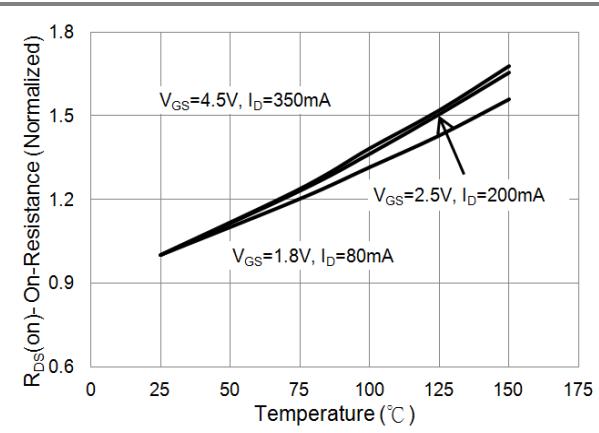


Fig.4 On-Resistance vs. Junction temperature

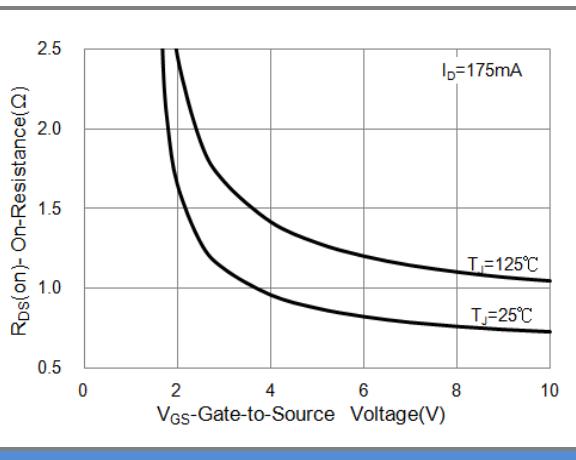


Fig.5 On-Resistance Variation with VGS.

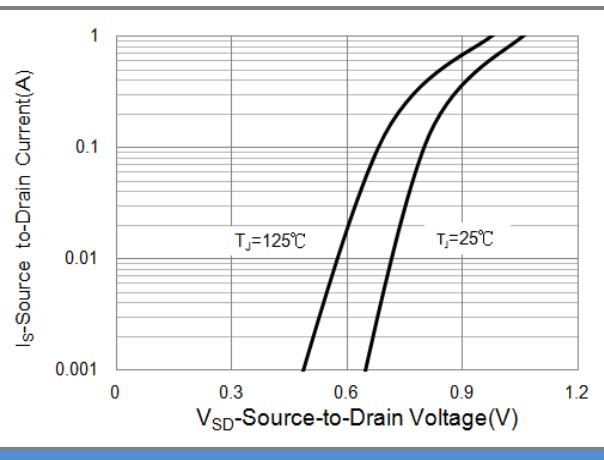


Fig.6 Body Diode Characteristics



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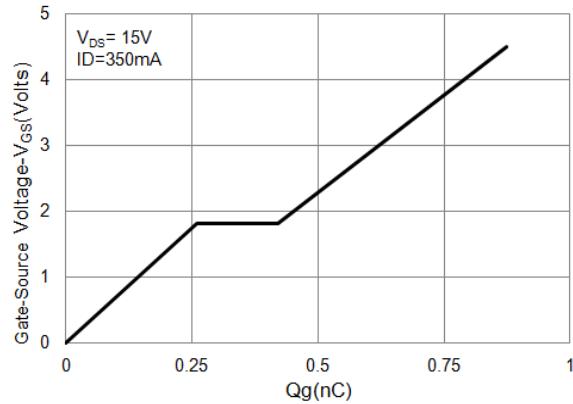


Fig.7 Gate-Charge Characteristics

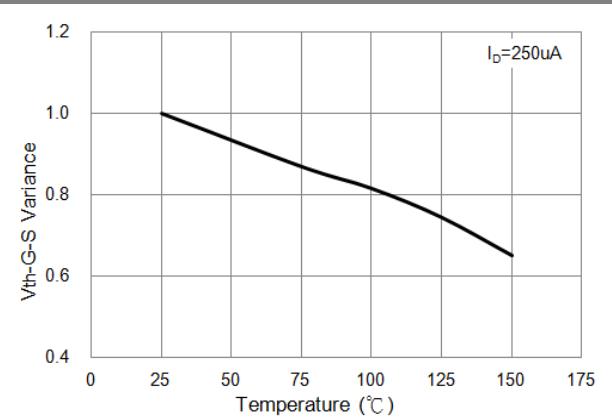


Fig.8 Threshold Voltage Variation with Temperature.

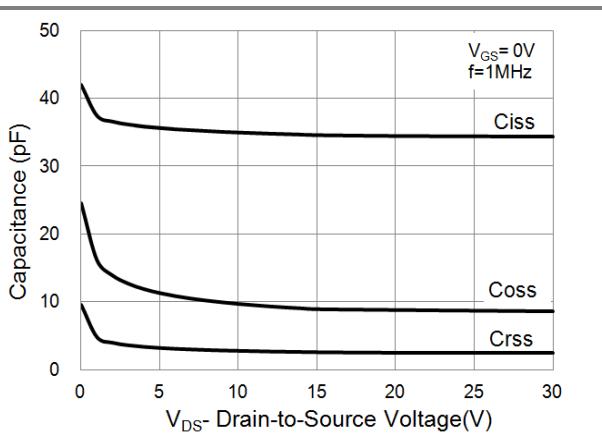


Fig.9 Capacitance vs. Drain-Source Voltage.

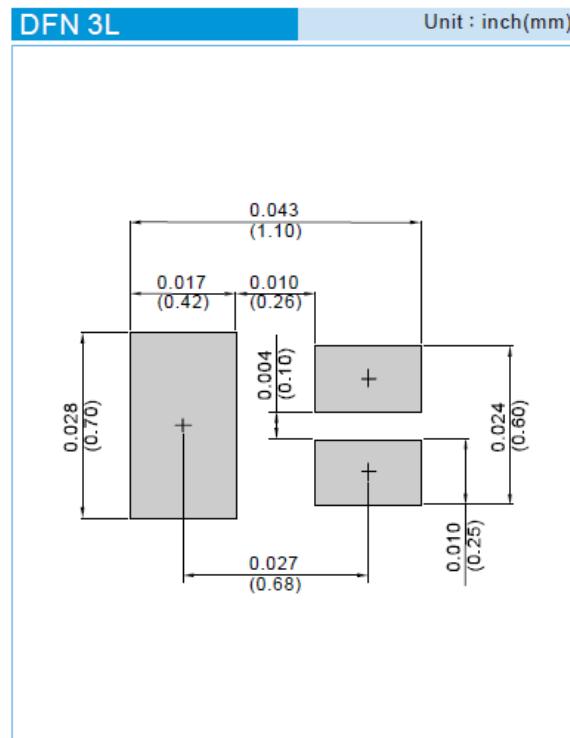


# PJQ1902

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJQ1902_R1_00001	DFN3L	8K pcs / 7" reel	2	Halogen free

## MOUNTING PAD LAYOUT





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